DA9080

PMIC Solution for Kneron KL730

This document describes all the default register settings of the DA9080, for supplying power to the Kneron KL730 system, and associated peripherals. It focuses primarily on DA9080's configuration with respect to the KL730 power on/off requirements.

The DA9080 is a high-performance, low cost, five channel PMIC designed for 32-bit and 64-bit MCU / MPU applications. The internally compensated regulators provide a highly integrated, small footprint power solution for System-On-Module (SOM) applications.

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1. Terms and Definitions

ADC	Analog to digital converter
CH<x>	Channel <x>, where x = 1 to 4
FCQFN	Flip chip quad flat-pack no-lead (package)
LDO	Low drop out (regulator)
OTP	One time programmable
PG	Power good
SOM	System-on-Module

2. References

[1] DA9080, Datasheet, Renesas Electronics.

[2] KL730, Datasheet, Kneron.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

The KL730 system requires the following supplies: [0.8, 1.1, 1.8, 3.3] V. To meet startup requirements the following timings should be met.

- The 0.8 V supply must ramp up to 80%, a minimum of 10 µs, before the 1.1 V supply ramps up to 80 %.
- The 1.8 V supply must ramp up to 80%, a minimum of 10 µs, before the 3.3 V supply ramps up to 80 %.
- The 1.8 V supply must **not** ramp up to 80% before 1.1 V reaches 80%. In other words**,** the 1.8 V supply must rise at the same time, or before, the 1.1 V supply.
- Following the 3.3 V supply reaching 80% of its target voltage, there should be a minimum delay of 1 ms before SYS_I_nRST goes high (> 2.0 V).

The ramp up time requirements of each individual supply are shown in Table 1.

Table 1. Individual Supply Ramp Up Requirements

Supply	Ramp Up Time
0.8 V	100 µs ~ 10 ms
1.1 V	140 µs ~ 10 ms
1.8 V	220 µs ~ 10 ms
3.3 V	0 µs ~ 10 ms

4. Power Supply Tree Diagram

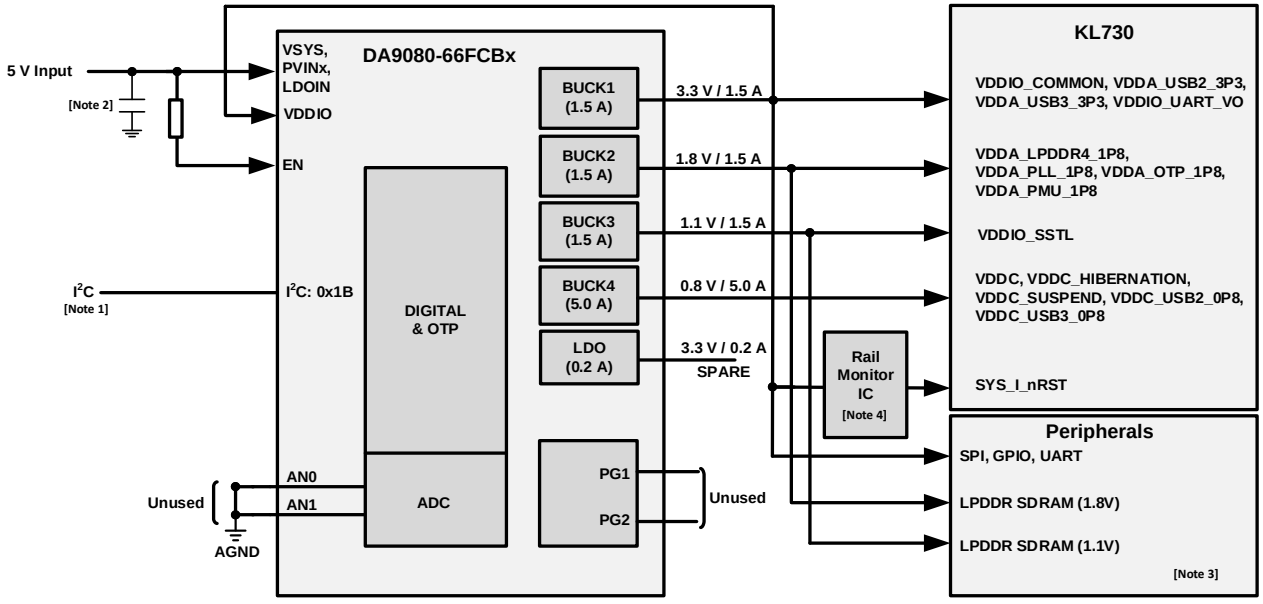

Figure 1. DA9080 to KL730 Tree Diagram

Note 1 The I²C (SCL and SDA) should be connected to the KL730.

Note 2 A large bulk capacitor (100 µF ~ 1000 µF) should be added to the 5 V input of DA9080.

Note 3 The peripherals included here are for example purposes; others may be able to be powered by the DA9080 device. Designers should ensure their power demands are appropriate.

Note 4 CH1 (3.3 V) can be passed into a rail monitoring IC (2.9 V threshold) to generate the reset signal.

5. Power On/Off Sequences

Table 2. Power Sequence

DA9080 Sequencer Slot	DA9080 Channel (Output Volage)
Slot 1	DA9080 CH4 (0.8 V)
Slot 2	DA9080 CH2 (1.8 V)
Slot 3	DA9080 CH3 (1.1 V)
Slot 4	DA9080 CH1 (3.3 V)

Channel 1: CH1 (3.3 V), Channel 2: CH2 (1.8 V), Channel 3: CH3 (1.1 V), Channel 4: CH4 (0.8 V)

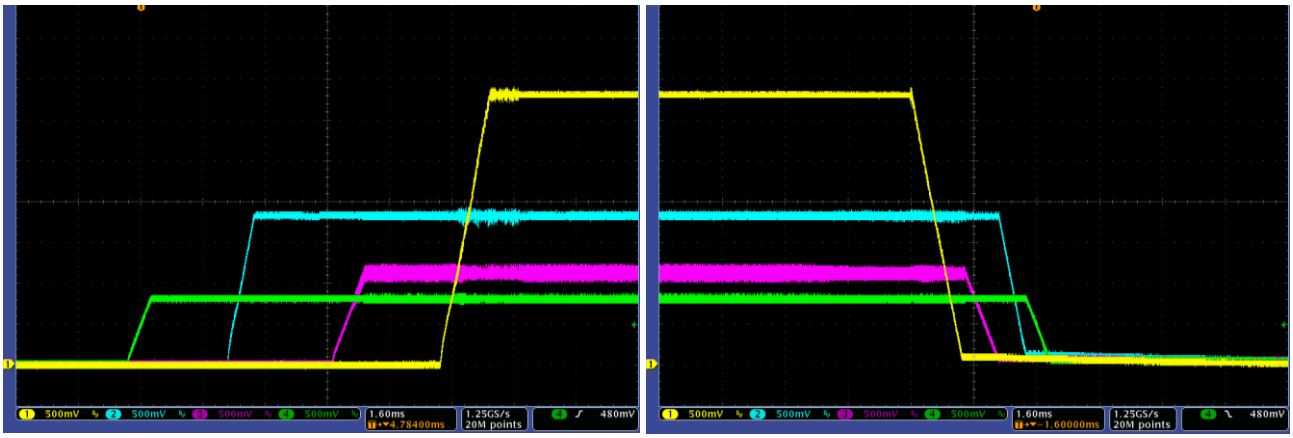

Figure 2. DA9080-66FCBx Power Up/Down

6. Detailed Description

Table 3. Register Settings DA9080-66FCBx (I2C slave address is 0x1B (7-bit))

Register Address	Register Name	Default Value	Description
0x04	PMC_ADC_ENABLE	0x00	ADC disabled
0x05	PMC_CH_EN	0x1F	CH1, CH2, CH3, CH4 and LDO enabled
0x06	PMC_VOUT_LDO	0x1F	VLDO = 3.30 V
0x07	PMC_VOUT_BUCK1	0x3C	VCH1 = 3.30 V
0x08	PMC_VOUT_BUCK2	0x0F	VCH2 = 1.80 V
0x09	PMC_VOUT_BUCK3	0x28	VCH3 = 1.10 V
0x0A	PMC_VOUT_BUCK4	0x00	VCH4 = 0.80 V
0x0B	PMC_PHASE_INTERLEAVING	0x88	BUCK1_PHASE = 0º BUCK2_PHASE = 180º BUCK3_PHASE = 0º BUCK4_PHASE = 180º
0x0C	PMC_BUCK_SEQ_GRP	0x27	CH1 = SLOT4, CH2 = SLOT2 CH3 = SLOT3, CH4 = SLOT1
0x0D	PMC_LDO_SEQ_GRP	0x03	LDO = SLOT4
0x0E	PMC_PG1	0x1C	CH2, CH3 and CH4 assigned to PG1
0x0F	PMC_PG2	0x03	CH1 and LDO assigned to PG1
0x10	PMC_DISCHARGE	0x1F	CH<x> and LDO discharge enabled
0x62	OTP_CONFIG_ID	0x66	OTP variant number: DA9080-66FCBx

7. Variant Table and Ordering Information

Table 4. Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9080-66FCB2	32 FCQFN	5.0 x 5.0 by 0.5 mm pitch	Reel	6000
DA9080-66FCBC				1000

8. Revision History

Revision	Date	Description
01.00	Mar 24, 2025	First version.

STATUS DEFINITIONS

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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