DA9083-26UUx Variant Overview

Register Settings Description

This document describes all the register default settings of the DA9083-26UUx variant (the x denotes the package option).

Contents

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1. Terms and Definitions

CH<x>	Channel <x>, where x = 1 to 4
DVC	Dynamic voltage control
LDO	Low drop out
OTP	One time programmable
WLCSP	Wafer Lever Chip Scale Package

2. References

[1] DA9083_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Variant Table and Ordering Information

Table 1. Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9083-26UUC	36 WLCSP	2.5 x 2.5	Tape & Reel	3000
DA9083-26UU6	36 WLCSP	2.5 x 2.5	Waffle Tray	500

4. Detailed Description

Key settings:

- VCH1 = 0.55 V, VCH2 = 0.55 V, VCH3 = 0.55 V, VCH4 = 0.55 V
- VLDO = 1.4 V
- LSW, CH1, CH2, CH3, CH4 and LDO are OFF by default
- CH1, CH2, CH3 and CH4 operate in AUTO mode, 2 MHz
- I^2C standard speed. I^2C slave address = 0x1B (7-bit)

Table 2. Register Settings DA9083-26UUx Variant

Register Address	Function	Default Value	Description
0x03	PMC_CH1_CFG_REG	0x6A	ILmax = 4 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x05	PMC_CH2_CFG_REG	0x6A	ILmax = 4 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x07	PMC_CH3_CFG_REG	0x6A	ILmax = 4 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x09	PMC_CH4_CFG_REG	0xAA	ILmax = 8.5 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x0B	PMC_LDO_SEL_REG	0x00	VLDO = 1.40 V
0x0F	PMC_DCDCCTRL0_REG0	0x00	LSW enable, CH<x> enables and LDO enable controlled by the Sequencer
0x10	PMC_SLEEP_REG0	0x00	SLEEP settings not configured
0x11	PMC_DCDCCTRL1_REG	0x00	CH<x> operating in AUTO mode
0x12	PMC_DISCHARGE_REG0	0xFC	LSW, CH<x> and LDO discharge enabled
0x13	PMC_DCDCCTRL2_REG	0x00	CH<x> and LDO operating in Higher Power mode
0x14	PMC_CH1CH2_WAKEUP_TIME	0x00	CH1, CH2 are OFF by default
0x15	PMC_CH3CH4_WAKEUP_TIME	0x00	CH3, CH3 are OFF by default
0x16	PMC_LDO_WAKEUP_TIME	0x00	LDO is OFF by default
0x1B	PMC_IRQ_MASK0	0x00	No IRQ events masked
0x1C	PMC_IRQ_MASK1	0x00	No IRQ events masked
0x1D	PMC_IRQ_MASK2	0x00	No IRQ events masked
0x1E	PMC_VOUT_CH1	0x37	VCH1 = 0.55 V
0x1F	PMC_VOUT_CH2	0x37	VCH2 = 0.55 V
0x20	PMC_VOUT_CH3	0x37	VCH3 = 0.55 V
0x21	PMC_VOUT_CH4	0x37	VCH4 = 0.55 V
0x4C	BUCK_BUCK_OPT_04	0x00	Divider mode disabled

Register Address	Function	Default Value	Description
			VCH1 range = 0.55 V to 1.9 V
0x4D	BUCK_BUCK_OPT_05	0x00	Divider mode enabled VCH2 range = 0.55 V to 1.9 V
0x4E	BUCK_BUCK_OPT_06	0x00	Divider mode disabled VCH3 range = 0.55 V to 1.9 V
0x4F	BUCK_BUCK_OPT_07	0x00	Divider mode enabled VCH4 range = 0.55 V to 1.9 V
0x62	OTP_CONFIG_ID	0x26	OTP variant number: DA9083-26UUx

Revision History

Revision	Date	Description
1.0	May 21, 2024	First version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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