Application Note

DA9083-28UUx Variant Overview

AN-PM-182

Abstract

This application note describes all the register default settings of the DA9083-28UUx variant (the x denotes the package option).

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1 Terms and Definitions

CH	Channel
DVC	Dynamic voltage control
LDO	Low Drop Out
OTP	One Time Programmable
WLCSP	Wafer Lever Chip Scale Package

2 References

[1] DA9083_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

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3 Variant Table and Ordering Information

Table 1: Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9083-28UUC	36 WLCSP	2.5 x 2.5	Tape & Reel	3000
DA9083-28UU6	36 WLCSP	2.5 x 2.5	Waffle Tray	500

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4 DA9083-28UUx Detailed Description - Production Release

Key settings:

- VCH1 = 0.55 V, VCH2 = 1.5 V, VCH3 = 0.55 V, VCH4 = 1.5 V
- VLDO = 1.8 V
- LSW, CH1, CH2, CH3, CH4 and LDO are OFF by default
- CH1, CH2, CH3 and CH4 operate in PWM mode, 2 MHz
- I^2C standard speed. I^2C slave address = 0x1B (7-bit)

Table 2: Register Settings DA9083-28UUx Variant

Register Address	Function	Default Value	Description
0x03	PMC_CH1_CFG_REG	0x6A	ILmax = 4 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x05	PMC_CH2_CFG_REG	0x6A	ILmax = 4 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x07	PMC_CH3_CFG_REG	0x6A	ILmax = 4 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x09	PMC_CH4_CFG_REG	0xAA	ILmax = 8.5 A DVC slew rate up/down= 10/5 mV/µs fSW = 2 MHz
0x0B	PMC_LDO_SEL_REG	0xA0	VLDO = 1.80 V
0x0F	PMC_DCDCCTRL0_REG0	0x00	LSW enable, CH<x> enables and LDO enable controlled by the Sequencer
0x10	PMC_SLEEP_REG0	0x00	SLEEP settings not configured
0x11	PMC_DCDCCTRL1_REG	0xF0	CH<x> operating in PWM mode
0x12	PMC_DISCHARGE_REG0	0xFC	LSW, CH<x> and LDO discharge enabled
0x13	PMC_DCDCCTRL2_REG	0x00	CH<x> and LDO operating in Higher Power mode
0x14	PMC_CH1CH2_WAKEUP_TIME	0x00	CH1, CH2 are OFF by default
0x15	PMC_CH3CH4_WAKEUP_TIME	0x00	CH3, CH3 are OFF by default
0x16	PMC_LDO_WAKEUP_TIME	0x00	LDO is OFF by default
0x1B	PMC_IRQ_MASK0	0x00	No IRQ events masked
0x1C	PMC_IRQ_MASK1	0x00	No IRQ events masked
0x1D	PMC_IRQ_MASK2	0x00	No IRQ events masked
0x1E	PMC_VOUT_CH1	0x37	VCH1 = 0.55 V
0x1F	PMC_VOUT_CH2	0x4B	VCH2 = 1.5 V
0x20	PMC_VOUT_CH3	0x37	VCH3 = 0.55 V
0x21	PMC_VOUT_CH4	0x4B	VCH4 = 1.5 V
0x4C	BUCK_BUCK_OPT_04	0x00	Divider mode disabled VCH1 range = 0.5 V to 1.9 V
0x4D	BUCK_BUCK_OPT_05	0x40	Divider mode enabled

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DA9083-28UUx Variant Overview

Register Address	Function	Default Value	Description
			VCH2 range = 1.5 V to 2.7 V
0x4E	BUCK_BUCK_OPT_06	0x00	Divider mode disabled VCH3 range = 0.5 V to 1.9 V
0x4F	BUCK_BUCK_OPT_07	0x40	Divider mode enabled VCH4 range = 1.5 V to 2.7 V
0x62	OTP_CONFIG_ID	0x28	OTP variant number: DA9083-28UUx

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5 DA9083-28UUx Variant Overview

Table 3: OTP Variant Overview

Reg Add	Function	Standard Variant DA9083-28UUx
0x03	PMC_CH1_CFG_REG	0x6A
0x05	PMC_CH2_CFG_REG	0x6A
0x07	PMC_CH3_CFG_REG	0x6A
0x09	PMC_CH4_CFG_REG	0xAA
0x0B	PMC_LDO_SEL_REG	0xA0
0x0F	PMC_DCDCCTRL0_REG0	0x00
0x10	PMC_SLEEP_REG0	0x00
0x11	PMC_DCDCCTRL1_REG	0xF0
0x12	PMC_DISCHARGE_REG0	0xFC
0x13	PMC_DCDCCTRL2_REG	0x00
0x14	PMC_CH1CH2_WAKEUP_TIME	0x00
0x15	PMC_CH3CH4_WAKEUP_TIME	0x00
0x16	PMC_LDO_WAKEUP_TIME	0x00
0x1B	PMC_IRQ_MASK0	0x00
0x1C	PMC_IRQ_MASK1	0x00
0x1D	PMC_IRQ_MASK2	0x00
0x1E	PMC_VOUT_CH1	0x37
0x1F	PMC_VOUT_CH2	0x4B
0x20	PMC_VOUT_CH3	0x37
0x21	PMC_VOUT_CH4	0x4B
0x4C	BUCK_BUCK_OPT_04	0x00
0x4D	BUCK_BUCK_OPT_05	0x40
0x4E	BUCK_BUCK_OPT_06	0x00
0x4F	BUCK_BUCK_OPT_07	0x40

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Revision History

Revision	Date	Description
1	30-Jan-2024	Initial version.

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DA9083-28UUx Variant Overview

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
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