Application Note

DA9083 PCB Layout Recommendations

AN-PM-178

Abstract

This application note provides recommendations on how to place and route DA9083 device. It also gives guidance on the passive components needed for proper functioning of the system. This document is a guideline only; target applications may have different requirements.

Contents

Figures

Tables

1 Terms and Definitions

CH	Channel
GND	Ground
GPIO	General purpose input or output
IC	Integrated circuit
LDO	Low drop out
LSW	Load switch
PCB	Printed circuit board
WLCSP	Wafer level chip scale packaging

2 References

[1] DA9083_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3 Introduction

Renesas Electronics' DA9083 device is a power management IC that integrates four buck converters, one LDO, and one load switch, see datasheet [1].

The input voltage range of 2.9 V to 5.5 V makes it suited for a wide range of low voltage systems, including all single cell battery powered systems. The CH output voltages are programmable from 0.55 V to 1.9 V in 10 mV steps or from 1.5 V to 2.7 V in 20 mV steps. The LDO output voltage is programmable from 1.4 V to 1.9 V in 20 mV steps. The load switch has a current limit of 4 A.

The recommended components and connections for DA9083 is shown in Figure 1.

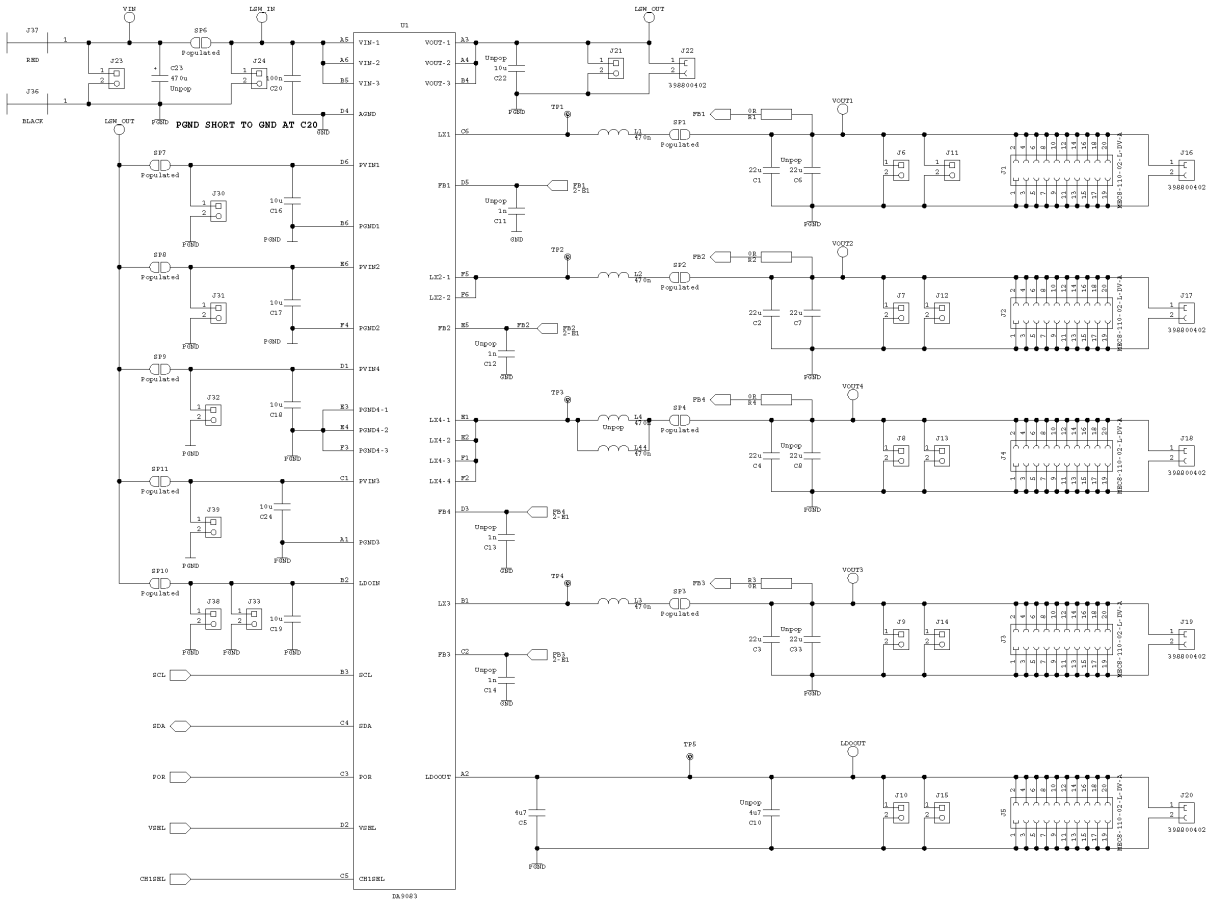


Figure 1: DA9083 Recommended Components and Connections

Table 1: DA9083 Recommended Components

Application	Part Reference	Value	Temp. Char.	Voltage Rating	ISAT and ITEMP
CVIN	C20	100 nF	X5R or better	6.3 V or above	N/A
CVOUT (Optional)	C22	10 µF	X5R or better	6.3 V or above	N/A
CPVIN1, CPVIN2, CPVIN3, CPVIN4	C16, C17, C18, C24	10 µF	X5R or better	6.3 V or above	N/A

DA9083 PCB Layout Recommendations

Application	Part Reference	Value	Temp. Char.	Voltage Rating	ISAT and ITEMP
CVOUT1, CVOUT2, CVOUT3, CVOUT4	C1, C2, C3, C4	22 µF	X6S or better	4V or above	N/A
CLDOIN	C19	10 µF	X5R or better	6.3 V or above	N/A
CLDOOUT	C5	4.7 µF	X5R or better	6.3 V or above	N/A
LOUT1, LOUT2, LOUT3,	L1, L2, L3	470 nH	N/A	N/A	5.8 A ISAT typical or above
LOUT4	L4	470 nH	N/A	N/A	7.2 A ISAT typical or above

4 Layout Recommendations

DA9083 is packaged in a 36-pin WLCSP package with a 0.4 mm pitch.

Although the PCB layout recommendations described in this application note is with reference to the Renesas Electronics' DA9083 Evaluation Board, a six-layer PCB, the required number of routing layers and other PCB parameters are also determined by the other devices in the system.

4.1 DA9083 Package Information

4.1.1 Ball Map

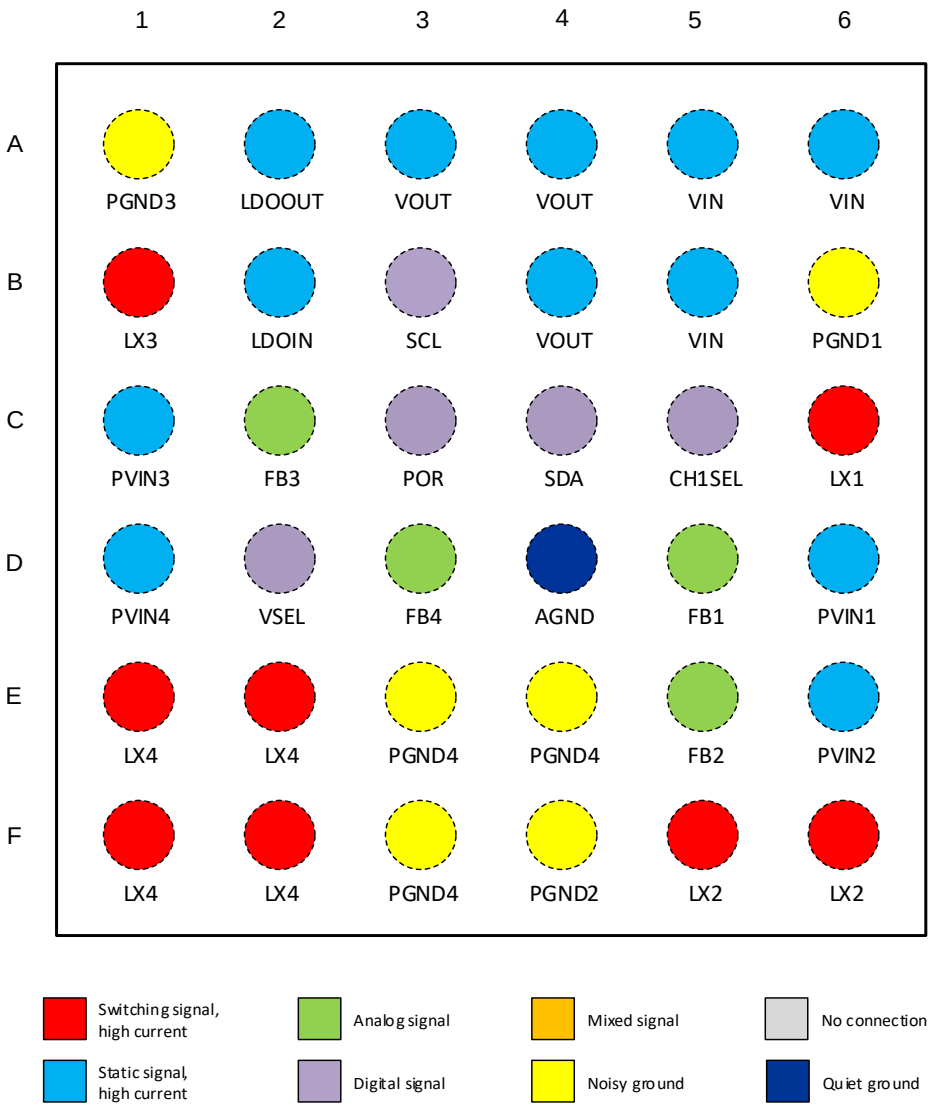


Figure 2: DA9083 Ball Map

4.1.2 Package Information

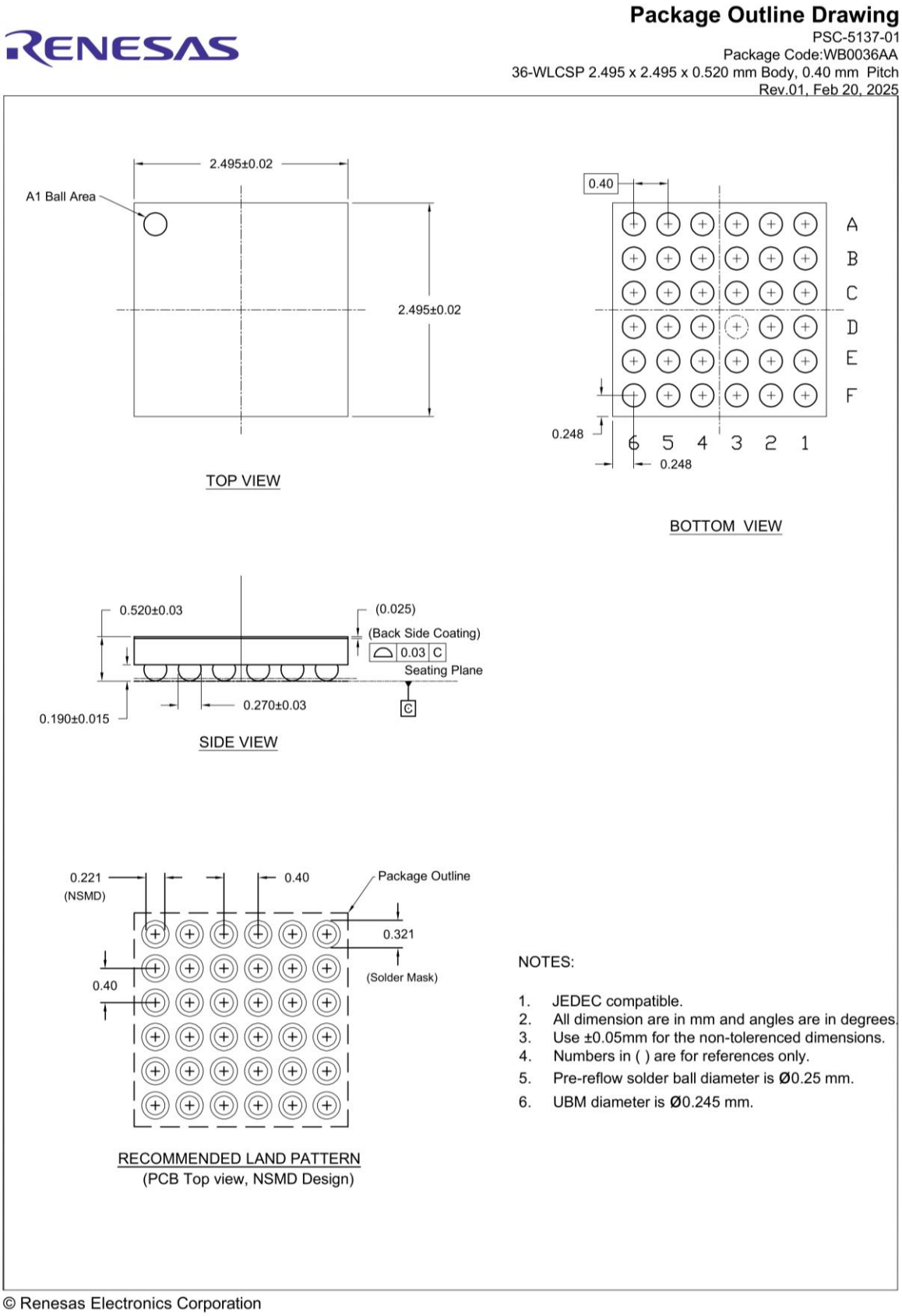


Figure 3: WLCSP6x6 Package Outline Drawing

4.2 Buck Converter, LDO and LSW

4.2.1 Input Decoupling

In a buck converter layout, the input capacitor location is critical. Locate the input capacitor as close as possible to the device's input and power GND pins to minimize the parasitic inductance.

In the DA9083 layout design, the input capacitor for each CH<x> should be placed as close as possible to the PVIN<x> and PGND<x> pins, and on the same layer as the DA9083 device.

If multiple layers are used, it is recommended to use as many as possible microvias (or through-hole vias) to minimize line resistance.

The load switch input capacitor should be placed near the VIN and AGND pins, and on the same layer as the DA9083 device.

Figure 4 shows the input capacitor placement and routing recommendation.

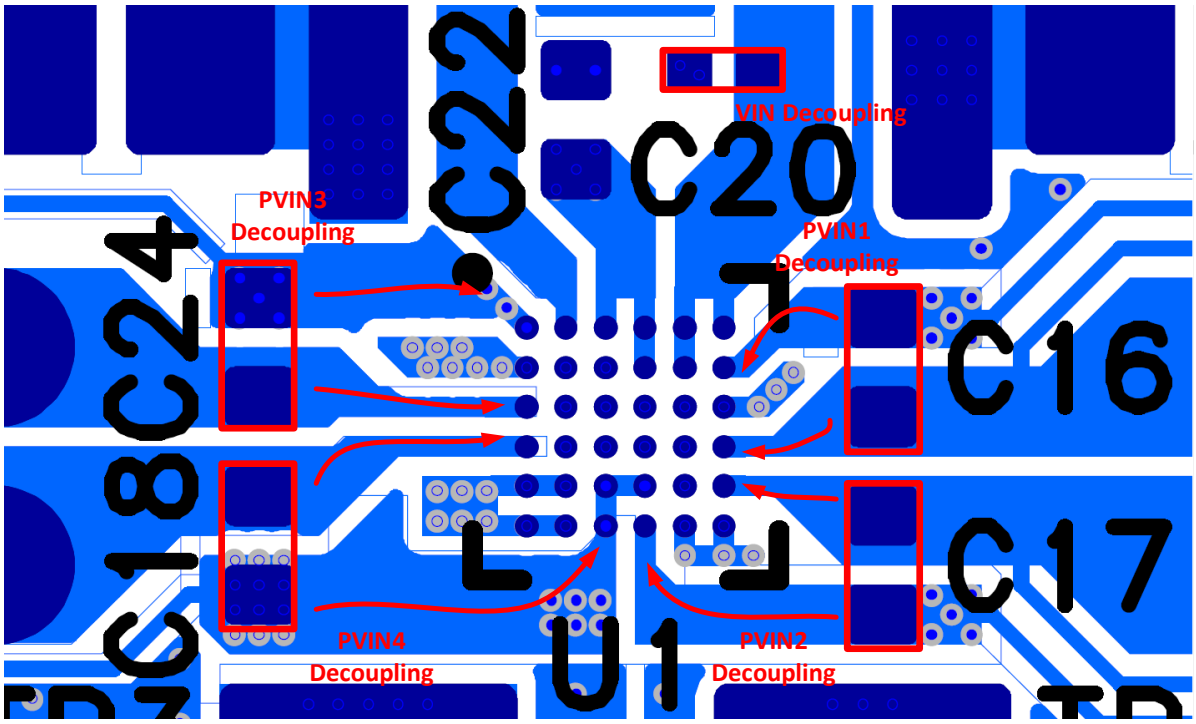


Figure 4: Recommended CH<x> and LSW Input Capacitors Placement and Routing

The LDO input capacitor should be placed as close as possible to the LDOIN and PGND pins, and in the DA9083 layout design it is placed on the bottom layer (opposite layer to DA9083).

Trace impedances to the LDO input connection should be minimized to reduce drop-out and effects on load regulation.

4.2.2 Ground Connections

Special care should be taken with ground connections because of the high current capability of DA9083 and because of the device's high-performance requirements.

The power PGND terminals (PGND<x>) of the DA9083 are placed conveniently to allow the placement of the PVIN decoupling capacitors as close as possible to the device.

It is best practice to isolate quiet analog GND (AGND) from noisy power GND terminals (PGND<x>).

On the Renesas Electronics' DA9083 Evaluation Board, AGND is isolated from the power GND terminals (PGND<x>) at the top layer (component layer) and connected at a single point (VIN bypass capacitor) on the bottom layer.

Layer 2 can be used as a return power GND plane, where the device's power GND pins (for CH<x>, LDO and LSW) and output capacitor GND can be connected. It is recommended to minimize the line impedance of the power GND pins and output capacitor GND connections by using as many vias as possible. This will also improve the heat dissipation.

NOTE
It is always recommended to use copper plugged vias to achieve the minimum parasitic via impedance and best thermal performance.

Example of GND terminals connection is illustrated in Figure 5.

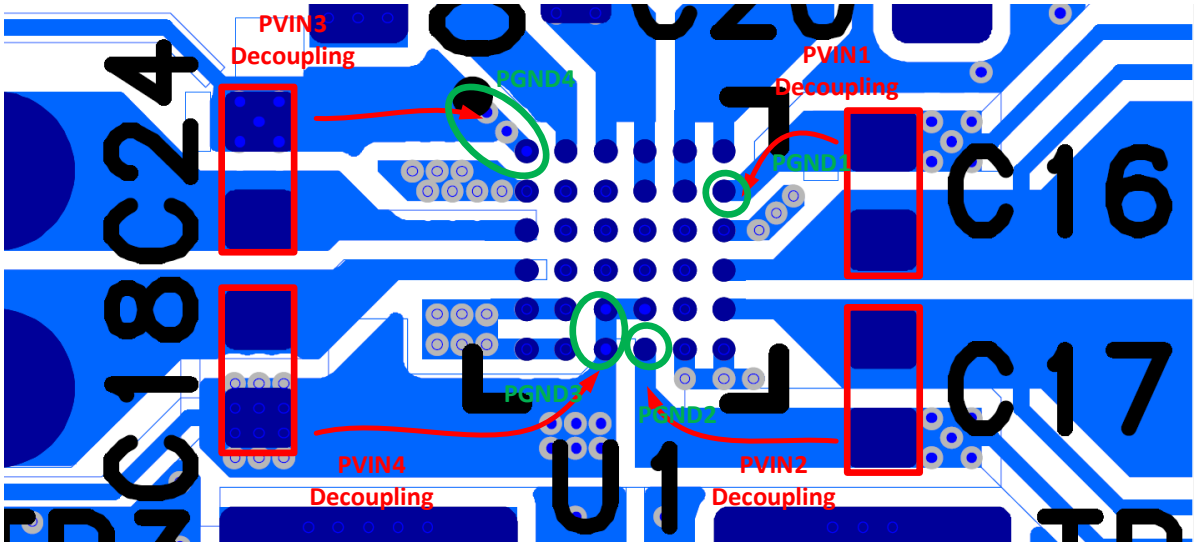


Figure 5: GND Terminals Connection

DA9083 PCB Layout Recommendations

To minimize ground-bounce effects from the bucks affecting the LDO or between bucks, it is recommended that GND 'cuts' are applied between each buck. Figure 6 illustrates the power ground with cuts (highlighted by red arrows) implemented on the Renesas Electronics' DA9083 Evaluation Board.

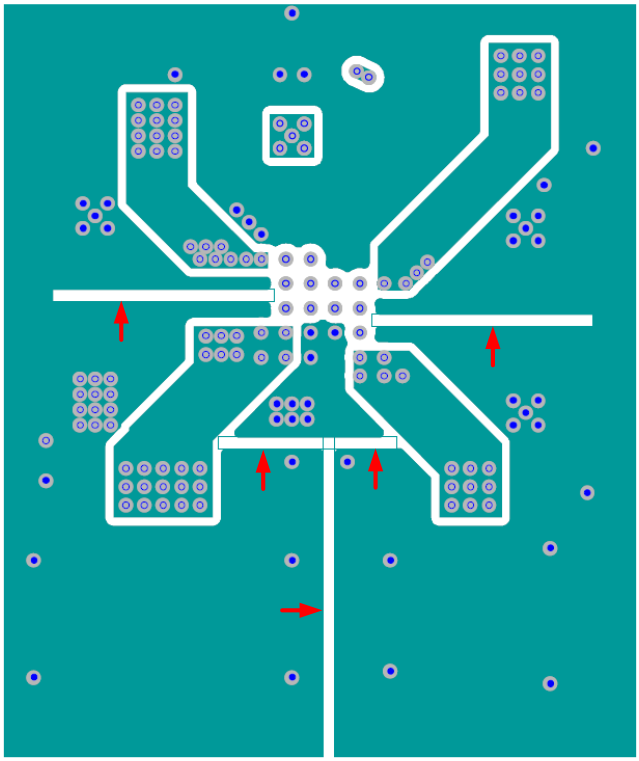


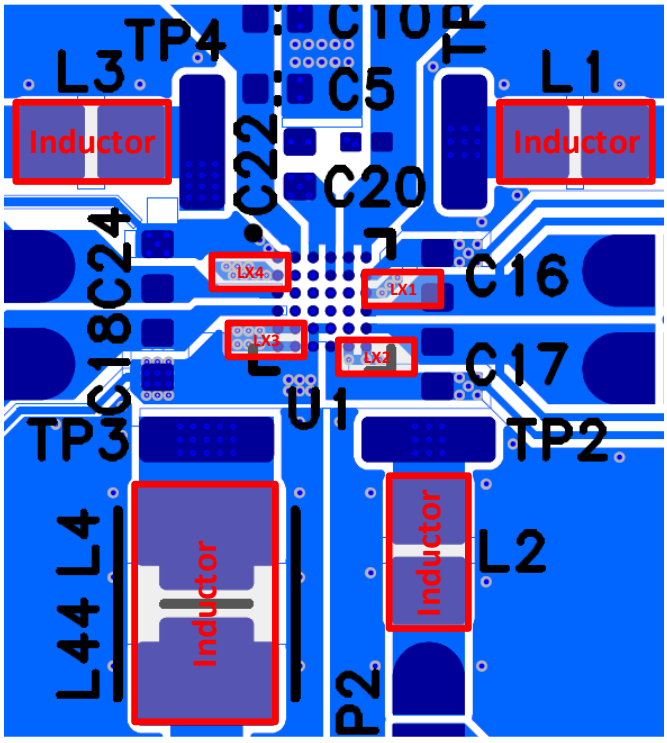
Figure 6: GND Cut on Layer 2

4.2.3 LX Routing

Switch node/LX node traces (traces between LX pins and output inductors) need to be kept as short as possible since this node generates switching noise, which can interfere with buck converters stability. Very high current will flow through these traces and so the minimum width of trace used for this LX node must be considered. Also, ensure that there are enough vias to deliver the current.

The LX node patterns on the Renesas Electronics' DA9083 Evaluation Board are shown in Figure 7. The LX nodes are routed out on layer 2 to allow the input capacitors to be placed as close as possible to the device.

Layer 1:



Layer 2:

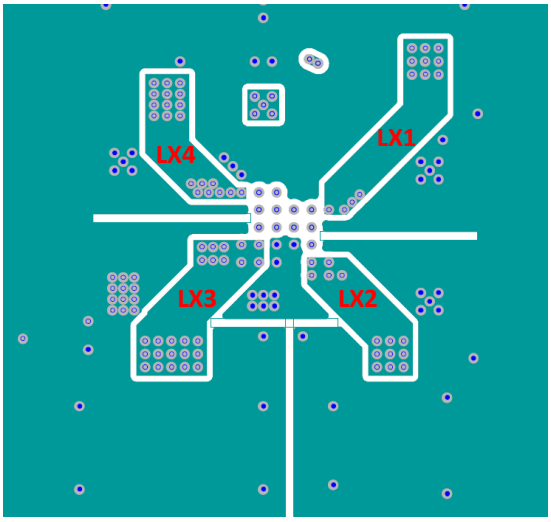


Figure 7: LX Node Pattern on DA9083 Evaluation Board

4.2.4 Buck, LDO and LSW Output

Output capacitors should be placed locally close to the output inductors to avoid any effects to the stability of the buck converters.

Minimizing the distance (which minimizes the line impedance) from the output inductors to the output capacitors is very important since it directly affects the efficiency and load transient response performance of the buck converter. Care must be taken with the size of the output traces to accommodate the high output current that DA9083 needs to support.

It is best practice to transfer the output current at the top layer directly without using any vias. This will give the best performance in terms of efficiency and load transient response performance.

The output capacitors for the LDO and LSW should be placed near the device. Trace impedances to the LDO output connection should be minimized to reduce drop-out and effects on load regulation.

4.2.5 Feedback Lines

Feedback lines must be routed far from any noise source (for example, output inductors, LX node, and so on). It is strongly recommended to place an UNPOP bypass capacitor (typically 1 nF) on the feedback. The bypass capacitor should be placed as close as possible to the IC. It is useful for filtering noise which may be injected to the feedback lines due to a layout limitation (for example, a long feedback pattern or noise from other devices in the system).

Also, ensure that the feedback lines are not overlapping any noisy node traces (for example, the LX node trace) without an insulation plane in between.

NOTE
The feedback lines must be routed directly from the load point in order to achieve the best voltage accuracy and stability.

Examples of output-voltage feedback-line routing, on the Renesas Electronics' DA9083 Evaluation Board, is shown in Figure 8.

Layer 6:

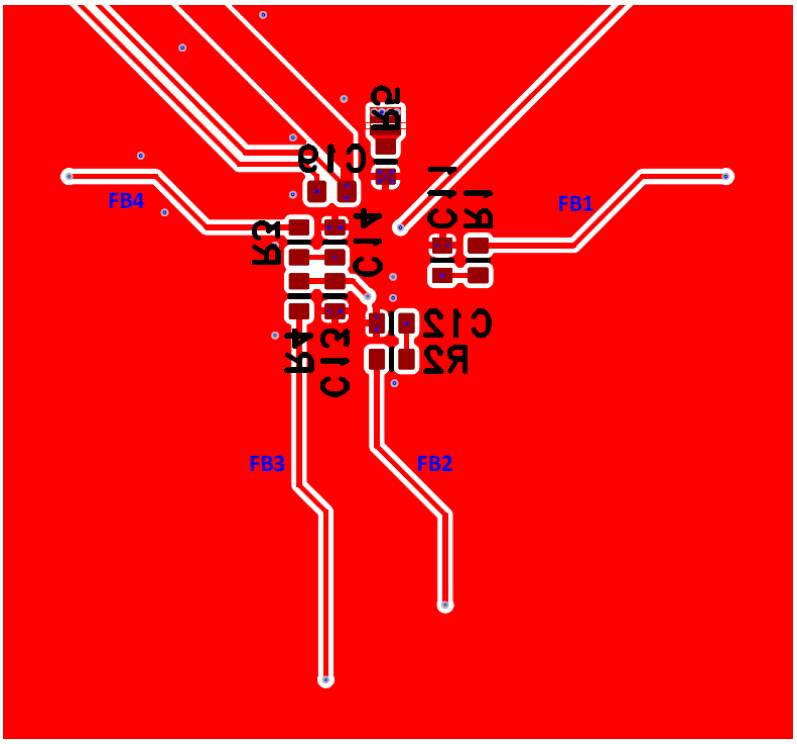


Figure 8: Output Voltage Feedback Line Routing on DA9083 Evaluation Board

4.3 Communication Interface (I^2C)

It is recommended to route the communication interface far from any noise source.

Care must also be taken regarding the noise produced by the interface signal in order to avoid coupling to the sensitive analog references and feedbacks. The routing layer is not critical, but it is recommended to use the bottom or top layer.

4.4 POR Signal

Generally, POR has the lowest routing priority. Any layer can be used for routing this signal.

However, care must be taken regarding the noise produced by the POR in order to avoid coupling to the sensitive analog references and feedbacks.

4.5 VSEL and CH1SEL Signals

VSEL and CH1SEL should be connected to GND.

Revision History

Revision	Date	Description
1	15-Sep-2023	Initial version.
1.1	11-Mar-2024	Section 3: Updated Figure 1 for better picture clarity
2.0	04-Apr-2025	Watermark removed and Figure 3 updated.

DA9083 PCB Layout Recommendations

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

DA9083 PCB Layout Recommendations

IMPORTANT NOTICE AND DISCLAIMER

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/

Trademarks