DA9083 Unused Pin Configuration

This application note describes the recommended configuration for unused pins in applications that use the DA9083 power management IC.

Contents

Tables

1. Terms and Definitions

CH<x>	Channel <x>
PGND	Power ground
IC	Integrated circuit
LDO	Low drop out
PMIC	Power management integrated circuit
SSD	Solid state drive

2. References

[1] DA9083_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

DA9083 is a six-channel, advanced, system power management IC (PMIC) that integrates four buck converters, one LDO, and one load switch. This high current integrated PMIC is ideal for Client and Enterprise SSD Modules, Hybrid Drives, and other memory management applications.

In some applications, certain functions or features may not be required and, to minimize any potential issues with these unused functions, the pins related to them need to be configured correctly. This document provides guidance on how to configure unused connections on DA9083.

4. DA9083 Functional Blocks

The following tables describe the recommended configurations for unused pins. **"**Mandator**y"** means that the pin is used in all applications.

Table 1: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AIO	Analog input/output
DIO	Digital input/output	PWR	Power
DIOD	Digital input/output open drain	GND	Ground

Table 2: Pin Description

Pin #	Pin Name	Type (Table 1)	Description	If Unused
A1	PGND3	GND	CH3 DCDC buck converter ground	Mandatory
A2	LDOOUT	AO	LDO output, bypass to ground with ceramic capacitor	Leave floating, cap not required
A3	VOUT	AO	Load Switch output	Leave floating, cap not required
A4	VOUT	AO	Load Switch output	Leave floating, cap not required
A5	VIN	PWR	Load Switch input	Mandatory
A6	VIN	PWR	Load Switch input	Mandatory
B1	LX3	AIO	CH3 DCDC buck converter switching node	Leave floating
B2	LDOIN	PWR	LDO input, bypass to ground with a ceramic capacitor	Connect to PGND<x>
B3	SCL	DI	I^2C interface data, connect SCL to the logic rail through a pull-up resistor	Mandatory - though can be connected to PGND<x> if no IOs are used

Pin #	Pin Name	Type (Table 1)	Description	If Unused
B4	VOUT	AO	Load Switch output	Leave floating
B5	VIN	PWR	Load Switch input	Mandatory
B6	PGND1	GND	CH1 Buck converter power ground	Mandatory
C1	PVIN3	PWR	CH3 Buck converter input	Connect to PGND<x>
C2	FB3	AI	CH3 Buck output voltage feedback connection	Connect to PGND<x>
C3	POR	DOD	Power-on-Reset release output signal (Power Good), output open-drain	Leave floating
C4	SDA	DIOD	I^2C interface data. Connect SDA to the logic rail through a pull-up resistor	Mandatory - though can be connected to PGND<x> if no IOs are used
C5	CH1SEL	DI	Reserved. Needs to be tied to ground	Mandatory
C6	LX1	AIO	CH1 Buck converter switching node	Leave floating
D1	PVIN4	PWR	CH4 Buck converter power	Connect to PGND<x>
D2	VSEL	DI	Reserved. Needs to be tied to ground	Mandatory
D3	FB4	AI	CH4 Buck output voltage feedback connection	Connect to PGND<x>
D4	AGND	GND	Quiet ground connection, Connect to a quiet ground area	Mandatory
D5	FB1	AI	CH1 Buck output voltage feedback connection	Connect to PGND<x>
D6	PVIN1	PWR	CH1 Buck converter input	Connect to PGND<x>
E1	LX4	AIO	CH4 Buck converter switching node	Leave floating
E2	LX4	AIO	CH4 Buck converter switching node	Leave floating
E3	PGND4	GND	CH4 Buck converter power ground	Mandatory
E4	PGND4	GND	CH4 Buck converter power ground	Mandatory
E5	FB2	AI	CH2 Buck output voltage feedback connection	Connect to PGND<x>
E6	PVIN2	PWR	CH2 Buck converter input	Connect to PGND<x>
F1	LX4	AIO	CH4 Buck converter switching node	Leave floating
F2	LX4	AIO	CH4 Buck converter switching node	Leave floating
F3	PGND4	GND	Power ground for the CH4 Buck converter	Mandatory
F4	PGND2	GND	Power ground for the CH2 Buck converter	Mandatory
F5	LX2	AIO	CH2 Buck converter switching node	Leave floating
F6	LX2	AIO	CH2 Buck converter switching node	Leave floating

5. Conclusion

Adherence to the recommendations of this document helps minimize spurious application issues, such as noise and increased current consumption, and may avoid device damage due to incorrectly biased pins. For further information please consult your Renesas Electronics local sales representative.

Revision History

Revision	Date	Description
1.0	Nov 26, 2024	First version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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