Application note

DA9155M PCB Layout Recommendations

AN-PM-074

Abstract

This application note provides recommendations on how to place and route the DA9155M device, and guidance on the passive components needed for proper functioning of the system. Application developers should treat this document as a guideline, not as a hard requirement, since the target application may have different requirements.

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1 Terms and definitions

GPIO	General Purpose Input/Output
PCB	Printed Circuit Board
TH	Through-Hole
WLCSP	Wafer level chip scale package
WLP	Wafer level packaging

2 References

1. DA9155M Datasheet, Dialog Semiconductor

3 Introduction

DA9155M is a slave charger that extends the current capability of an existing charging solution. It provides a regulated output current in the constant current phase of charging.

The DA9155M features a Buck converter capable of 2500 mA output current. The Buck regulates the output current with ±5 % accuracy. Current sensing is performed with a fully integrated circuit.

The input voltage range of 4.5 V to 13.5 V makes the DA9155M suitable to be powered from USB and high voltage travel adaptors. The output current limit is configurable in the range of 400 mA to 2500 mA in 10 mA steps.

The basic recommended components and connections for DA9155M are shown in Figure 1. DA9155M components and specifications for Capacitors are shown in Table 1 and for inductor in Table 2.

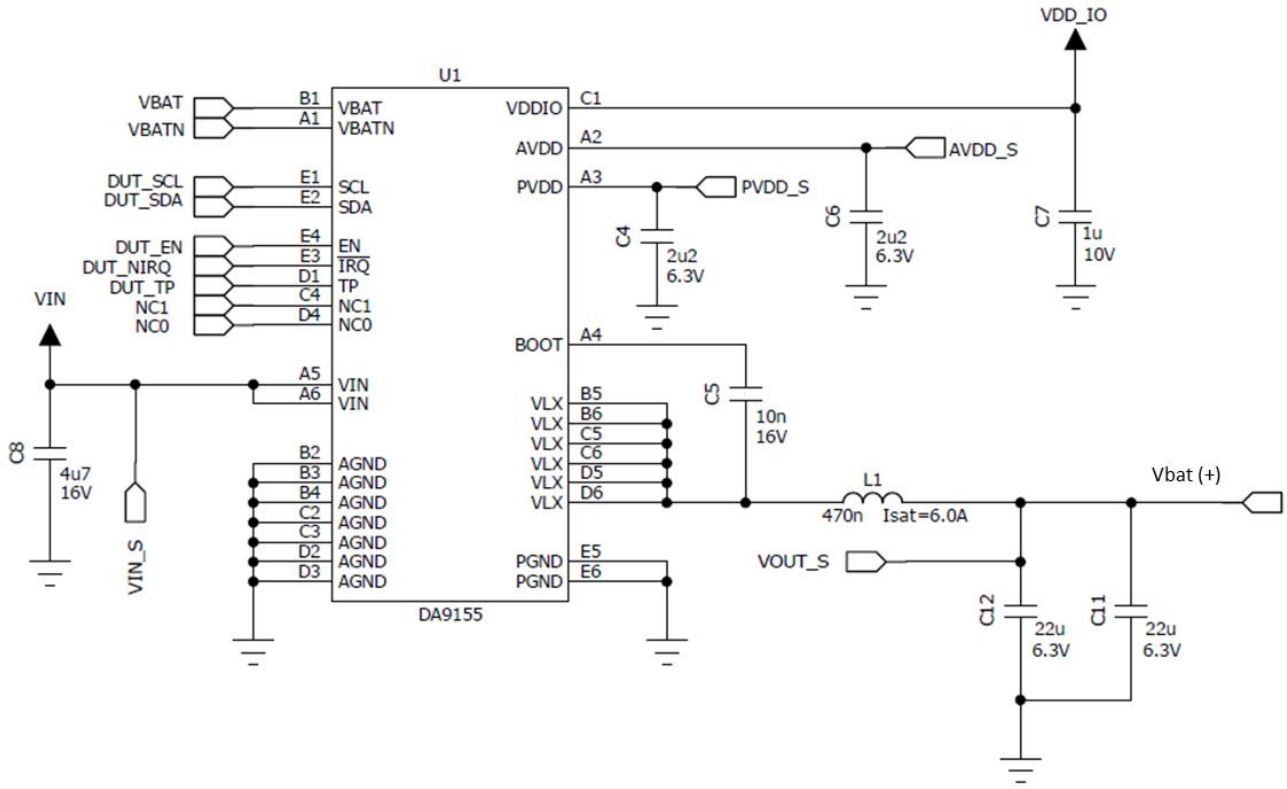


Figure 1: DA9155M schematic

Table 1: Capacitors

Reference	Quantity	Value	Size (mm)	Temp char.	Tol.	Voltage rating (V)
Buck input bypass cap	1	4.7 µF	1608	X5R	±20 %	16
Buck output bypass cap	2	22 µF	1608	X5R	±20 %	6.3
Buck bootstrap cap	1	10 nF	1005	X7R	±10 %	16 (min 6.3)
AVDD output bypass cap	1	2.2 µF	1005	X5R	±20 %	6.3
PVDD output bypass cap	1	2.2 µF	1005	X5R	± 20 %	6.3

Table 2: Inductor

Reference	Value (µH)	ISAT (A)	IRMS (A)	DCR (typ. [mΩ])	Size (L×W×H [mm])
Buck output inductor	0.47	6	4.5	24	2.5×2.0×1.0

4 Layout recommendations

DA9155M is packaged in a 30-pin WL-CSP device with a 0.4 mm pitch, 30 bumps WLP, 2.6 mm x 2.2 mm, 0.5 mm height.

At least a four-layer PCB stack-up should be used for best PCB layout design. However, the number of routing layers and other PCB parameters are also determined by the other devices in the system.

This document references Dialog's DA9155M Evaluation Board, which is a six-layer PCB stack-up, as an example to describe a recommended PCB layout design.

This document is divided into the following sections:

- Package information (section 4.1)
- Buck converter (section 4.2)
- Communication interfaces (section 4.3)
- GPIOs and control signals (section 4.4)

4.1 DA9155M package information

4.1.1 DA9155M pin description

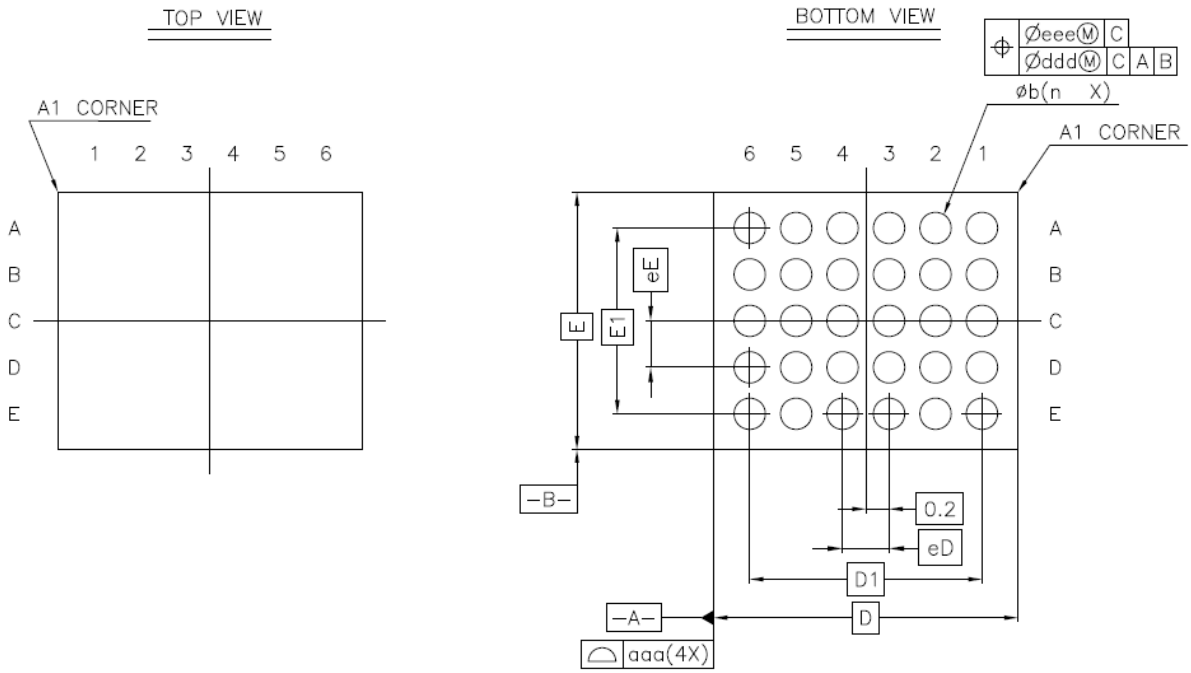
Table 3: Pin description

Pin	Name	Type	Description
C1	VDDIO	PS	IO supply
B2, B3, B4, C2, C3,D2, D3	AGND	GND	Analog ground
A2	AVDD	AIO	Internal supply
A3	PVDD	AIO	Internal supply
E2	SDA	DIO	Data signal of the 2-wire interface (GPIO)
E1	SCL	DI	Clock signal of the 2-wire interface (GPIO)
E4	EN	DI	Control signal for the output current/voltage (GPIO)
E3	nIRQ	DO	Interrupt signal to host processor (GPIO)
A5, A6	VIN	PS	Input supply
B5, B6, C5, C6, D5, D6	VLX	AO	Switching node of buck
A4	BOOT	AIO	Supply of the high-side driver
B1	VBAT	AI	Battery voltage sense, positive terminal
A1	VBATN	AI	Battery voltage sense, negative terminal
E5, E6	PGND	GND	Power grounds of the buck, digital ground
D1	TP	DIO	Test pin
C4, D4	NC		Not connected.

Table 4: Pin type definition

Pin type	Description	Pin type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
DIOD	Digital Input/Output open Drain	BP	Backdrive Protection
PU	Fixed pull-up resistor	SPU	Switchable pull-up resistor
PD	Fixed pull-down resistor	SPD	Switchable pull-down resistor

4.1.2 Package information



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.471	0.511	0.551
Stand Off	A1	0.178	–	0.206
Wafer Thickness	A2	0.279 ±0.025		
Body Size	D	2.620 BSC		
	E	2.220 BSC		
Ball Diameter (Size)		0.250		
Ball/Bump Width	b	0.255	0.270	0.285
Ball/Bump Pitch	eD	0.4		
	eE	0.4		
Ball/Bump Count	n	30		
Edge Ball Center to Center	D1	2.0 BSC		
	E1	1.6 BSC		
Package Edge Tolerance	aaa	0.03		
Coplanarity (whole wafer)	ccc	0.03		
Ball/Bump Offset (Package)	ddd	0.05		
Ball/Bump Offset (Ball)	eee	0.015		

Figure 2: DA9155M WLCSP package outline drawing

4.2 Buck converter

Figure 3 provides a guideline for component placement. The reference designators used in this section match the schematic shown in Figure 1.

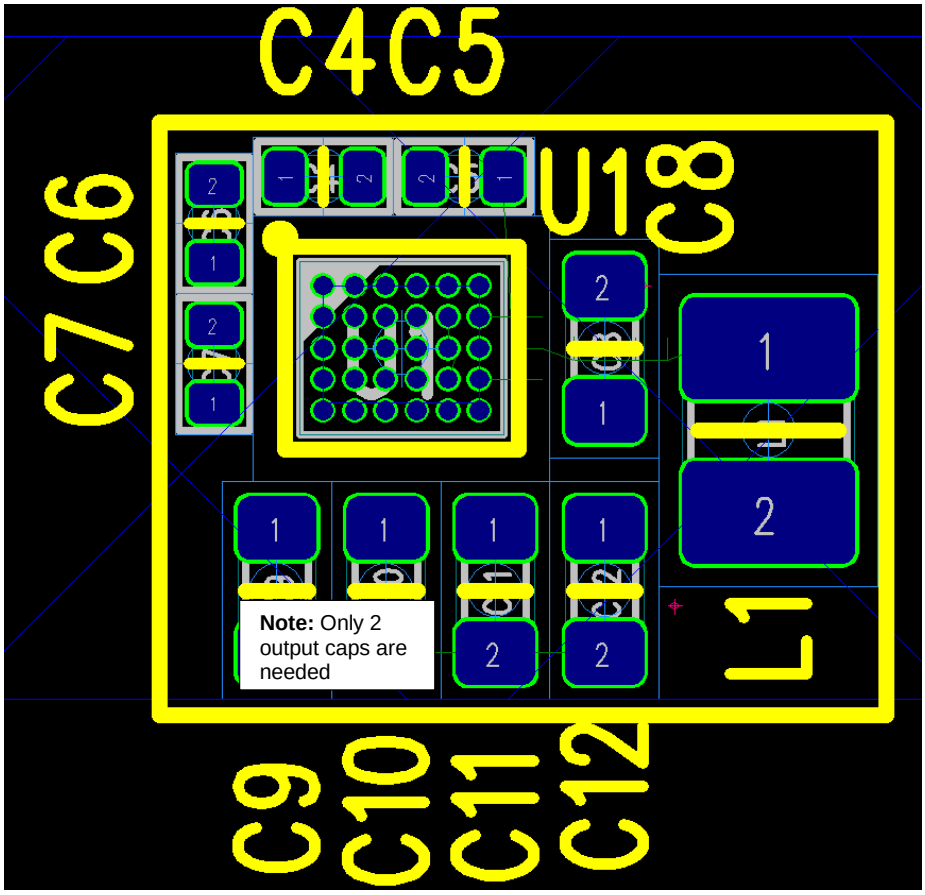


Figure 3: Components placement on Dialog's DA9155M Evaluation Board

4.2.1 DA9155M input

In a Buck converter layout, input capacitor location is critical. The input capacitor needs to be located as close as possible to the device's input and power GND pins. The step-down input bypass capacitors are the most critical components because they carry discontinuous currents with a high rate of change (di/dt). For the DA9155M layout design, the input capacitor for the Buck converter should be placed as close as possible to the VIN and PGND pins**,** and **on the same layer as the DA9155M device**. The traces between the input capacitor pads and device balls need to be as short as possible to minimise parasitic inductance. Placing the input capacitor on the opposite side of the PCB is not ideal because the vias that are necessary to connect the two halves of the PCB add inductance to this critical path.

If multiple layers are used, Dialog recommends using at least four TH vias (or eight micro-vias) to connect the input voltage (VIN) between layers and to minimise trace impedance. Also ensure that there is a sufficient number of vias to connect the input capacitor GND to the inner layer GND plane.

It is also recommended to place a 1 µF decoupling capacitor on VDD_IO line close to the DA9155M.

Figure 4 shows the input capacitor placement and routing recommendation.

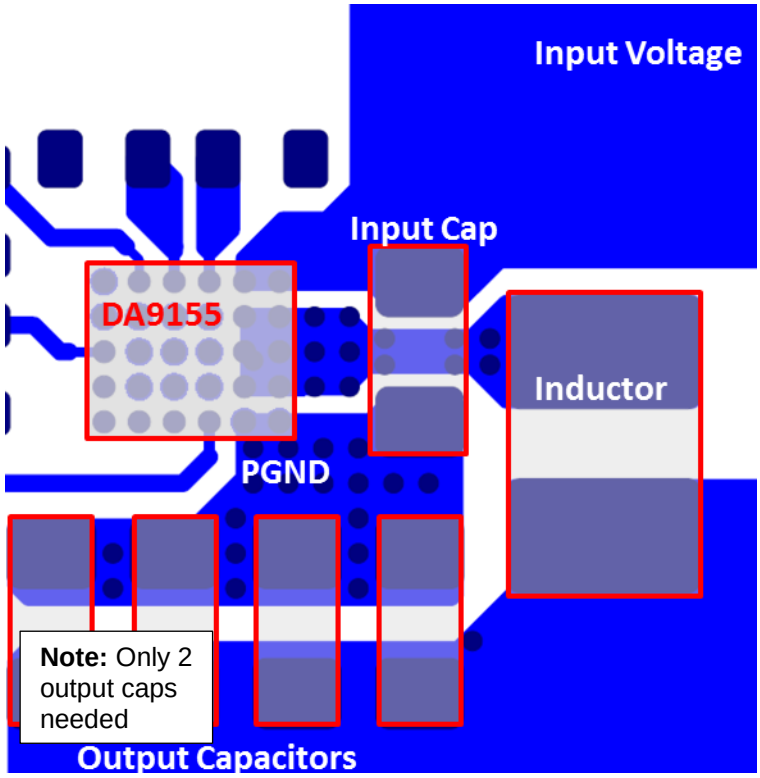


Figure 4: Recommended input capacitor placement and routing

4.2.2 Ground connections

Special care should be taken with ground connections because of the high performance requirements of the DA9155M.

The Buck converter PGND terminals should be connected together on the same layer as these are noisy power GNDs, and they should not be connected directly to any analog GND (for example, AGND) on the same layer.

It is recommended to connect power GND and analog GND together at a solid internal GND plane. It is best practice to isolate the power GND (noisy GND) from the analog GND (quiet GND) and to connect them at a single point close to the device. In addition, the PCB layout should minimise the line impedance of PGND pins and output capacitors GND connections by using as many vias as possible. This will also improve the heat dissipation.

NOTE
It is always recommended to use copper plugged vias in order to achieve the minimum parasitic via impedance, and best thermal performance.

Layer 3 can be used as a common GND plane. The common GND plane on Layer 3 also acts as a shield to protect noise-sensitive signal lines (for example, feedback lines) on Layer 4 and below from switching-noise interference. Also, connecting the less noisy output capacitor GND (instead of input capacitor GND) to common GND is preferable.

Examples of how to connect the GND terminals on Dialog's DA9155M Evaluation Board is illustrated in Figure 5, Figure 6, and Figure 7.

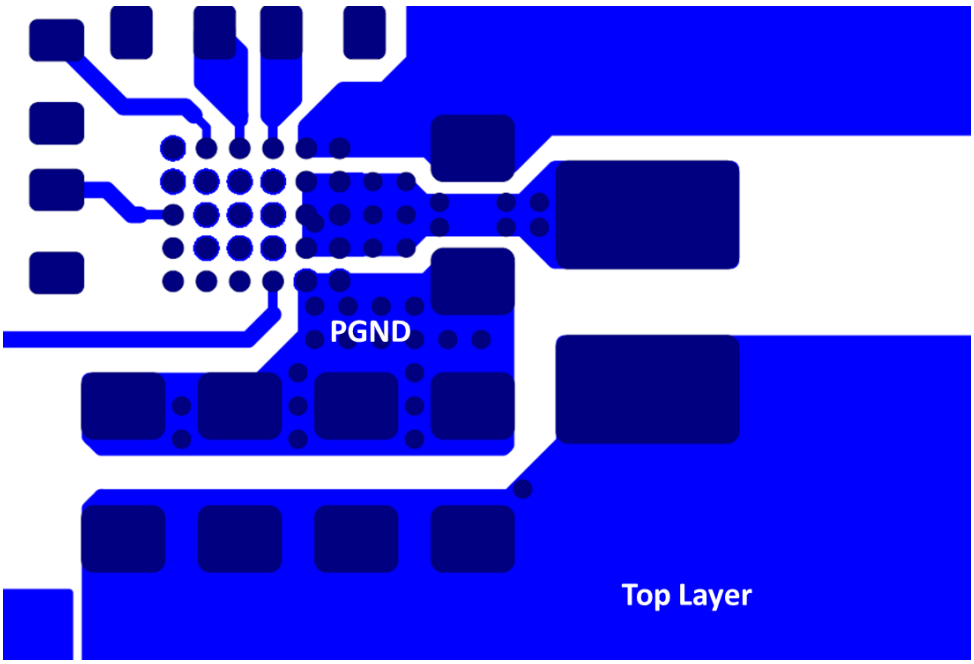


Figure 5: Top layer power ground

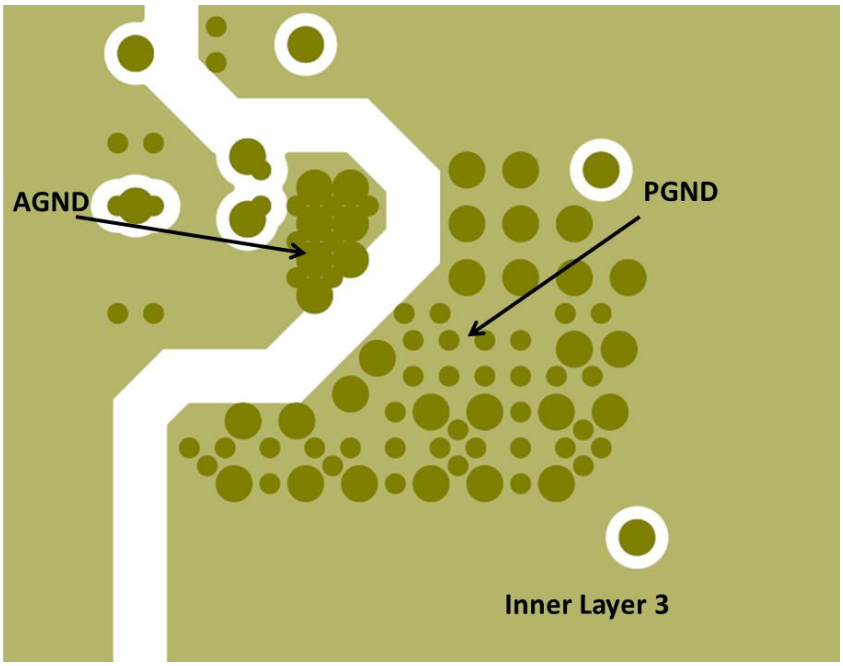


Figure 6: Inner layer 3 showing PGND and AGND

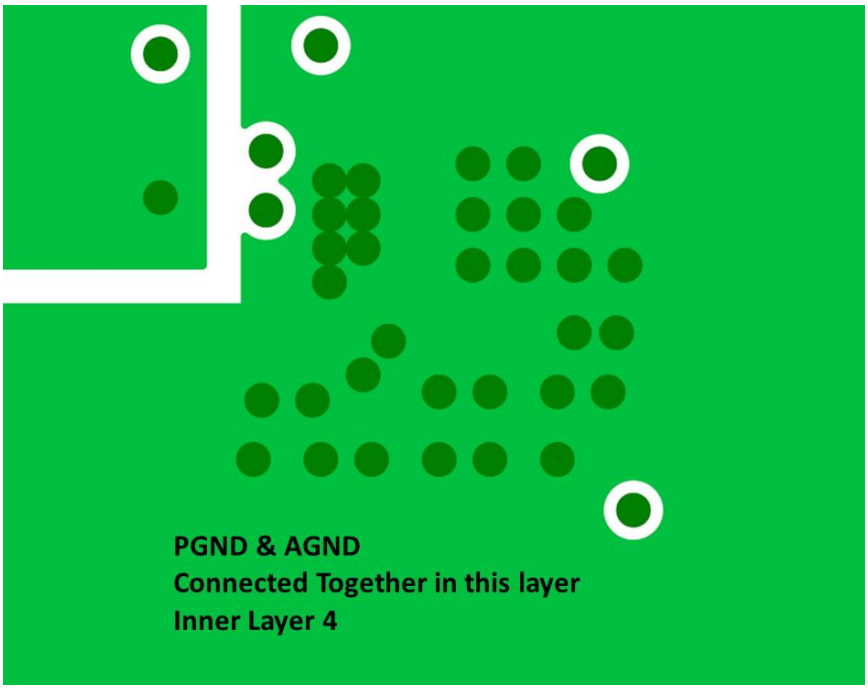


Figure 7: Inner layer 4 showing PGND and AGND

4.2.3 VLX routing

Switch node/VLX node traces (traces between VLX pin and the output inductor) need to be kept as short as possible since this node generates switching noise, and this can interfere with Buck converter stability. High current will flow through this trace and the minimum trace width for this VLX node must be considered.

Multiple layers may be preferable for VLX node traces. Also, ensure that there are enough vias (0.5 A per micro-via) to deliver the current.

Figure 8 and Figure 9 show the VLX node pattern on Dialog's DA9155M Evaluation Board.

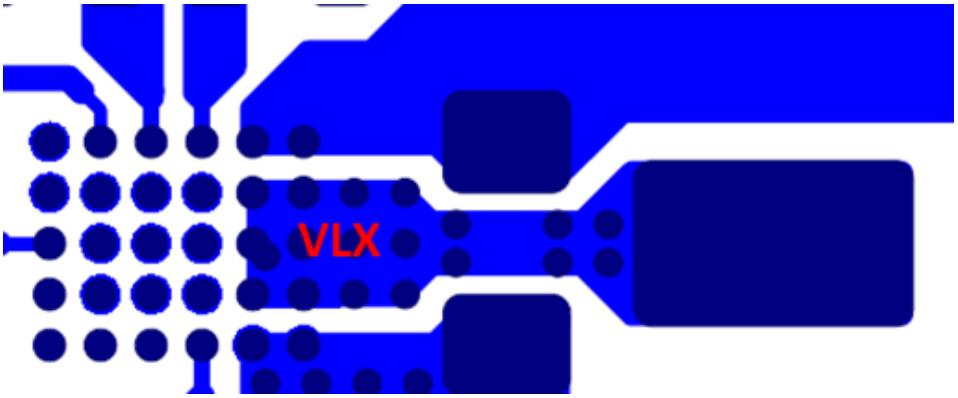


Figure 8: VLX pattern at top layer

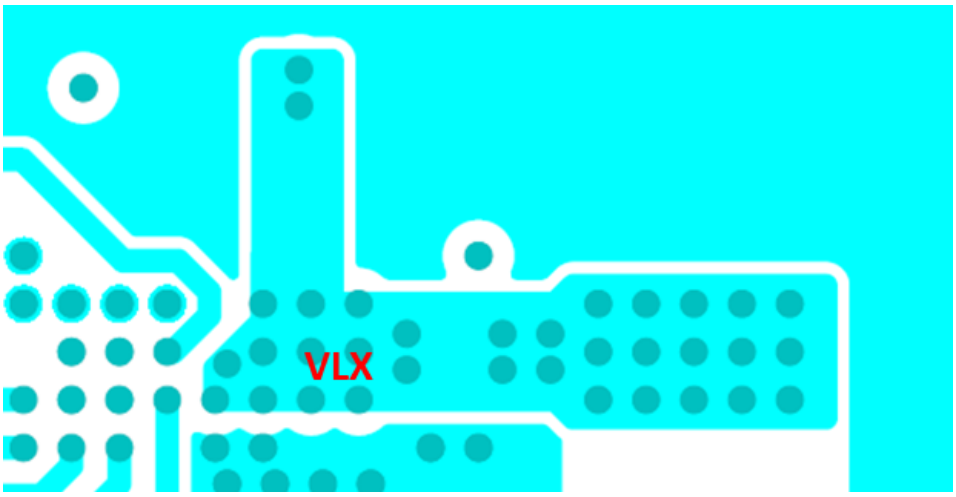


Figure 9: VLX pattern at layer 2

4.2.4 Buck output

Output capacitors should be placed as close as possible to the load. Do not split the output capacitors into local capacitors (close to the output inductor) and remote capacitors (close to the load) as this may affect the stability of the Buck converter.

However, minimising the distance (thus minimising the line impedance) from the output inductors to the output capacitors (the load) is also important since it directly affects the efficiency and load transient response performance of the Buck converter. Care must be taken regarding the size of the output traces since the output peak current can be up to 2500 mA for DA9155M.

It is best practice to transfer the output current at the top layer directly without using any vias. This will give the best performance in terms of efficiency and load transient response performance.

Figure 10 shows an example of inductor and capacitor placement based on Dialog's DA9155M Evaluation Board.

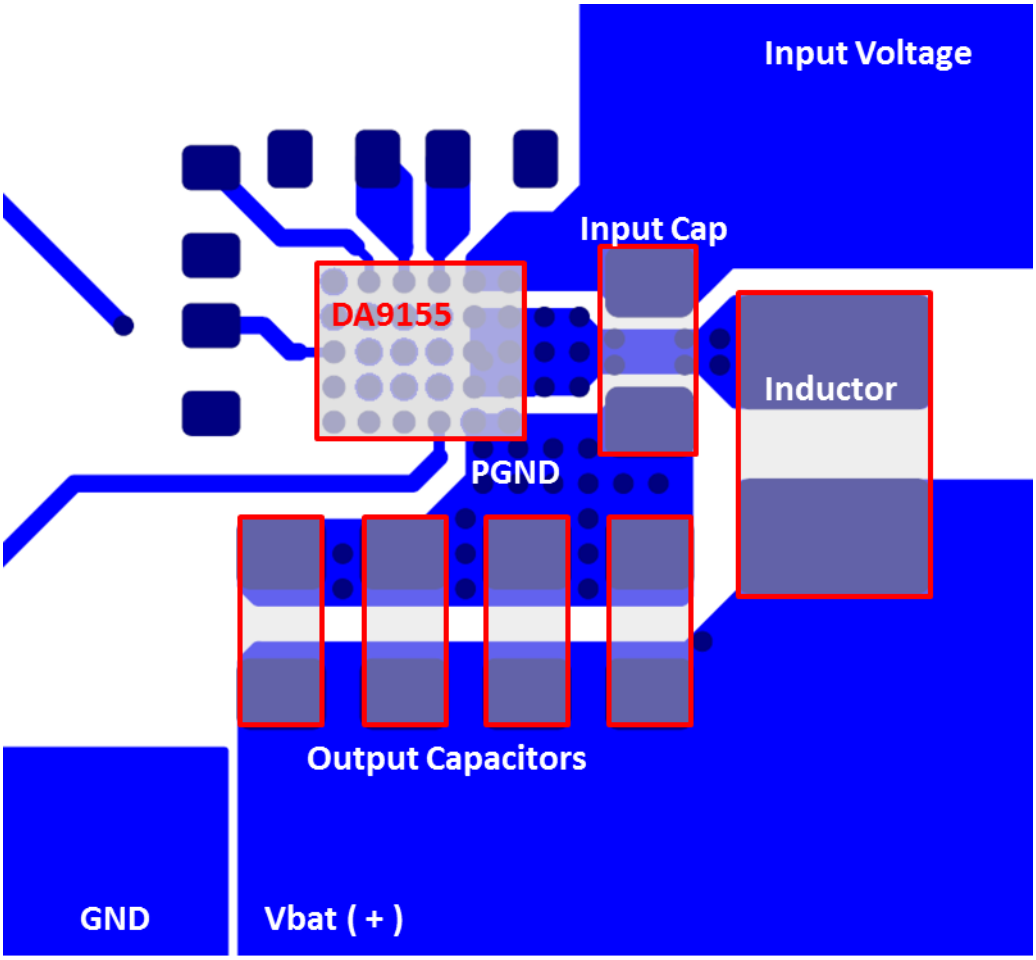


Figure 10: Output LC filter placement

4.2.5 Battery voltage sense

It is recommended to route the positive battery voltage sense (VBAT) and negative battery voltage sense (VBATN) as a differential pair to the battery connecting terminals, far from any noise source (for example, output inductors, VLX node, and such). This will help achieve the best voltage accuracy.

Also, ensure that the voltage sense lines are not overlapping any noisy node traces (for example, the VLX node trace) without an isolation plane layer in between. Assuming that DA9155M is assembled on the top layer, it is recommended to route the sense lines on layer 4 or below when the traces are near to the IC and/or the switch node areas.

NOTE
The negative battery voltage sense trace is at ground potential and care should be taken not to connect any part of the trace to the ground plane.

Figure 11 and Figure 12 show an example of the battery voltage sense routing on Dialog's DA9155M Evaluation Board.

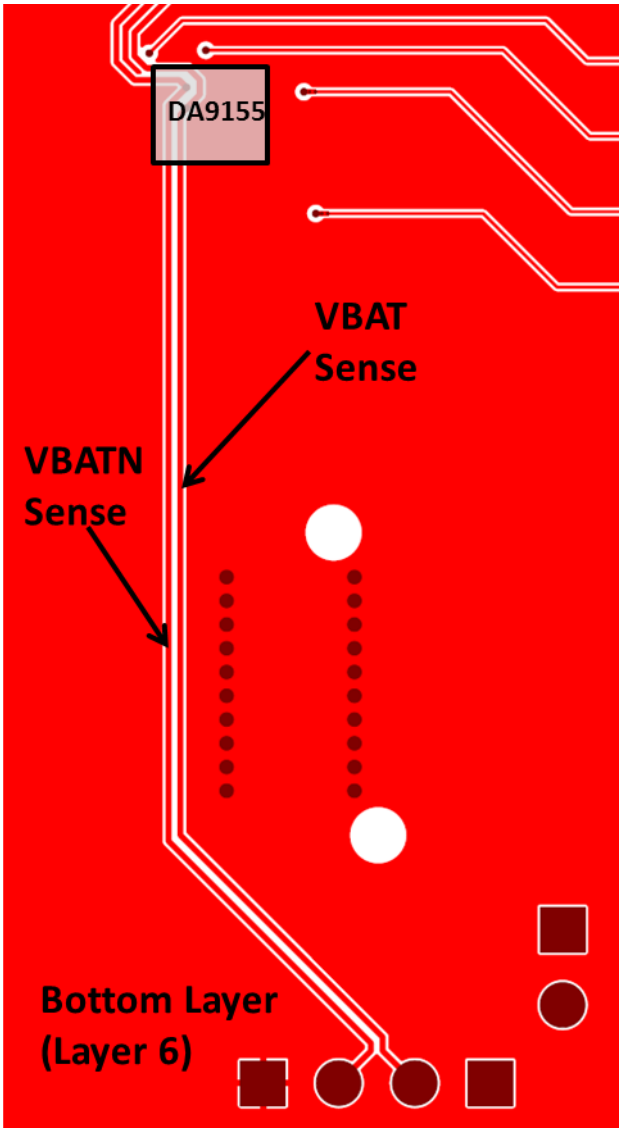


Figure 11: Battery voltage sense line routing

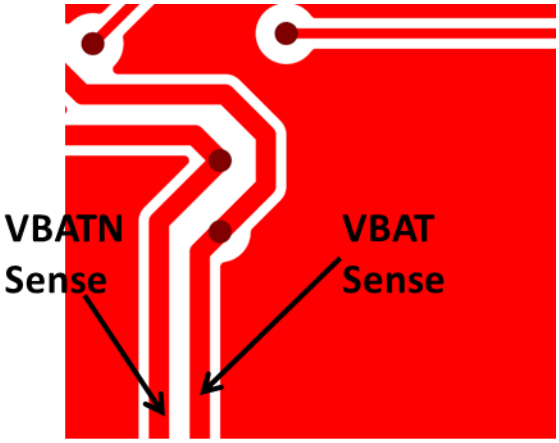


Figure 12: Battery voltage sense routing

4.3 Communication interfaces (I^2C)

There are no firm rules regarding the interface routing strategy. All of the signals are digital and are immune to various kinds of noise.

Care must be taken regarding the noise produced by the interface signal in order to avoid coupling to the sensitive analog references and feedbacks. The routing layer is not critical, but using the bottom or top layer is recommended.

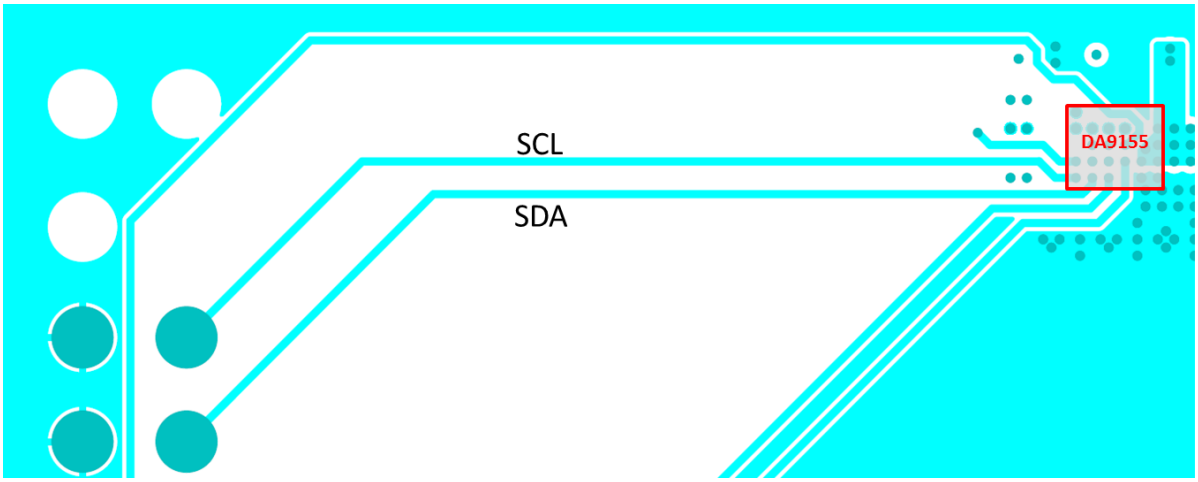


Figure 13: I^2C (SDA, SCL) interface lines

4.4 GPIO signals

Generally GPIOs have the lowest routing priority. Any layer can be used for routing these signals.

5 Revision history

Revision	Date	Description
1.0	12/08/2015	Initial version

Status definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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