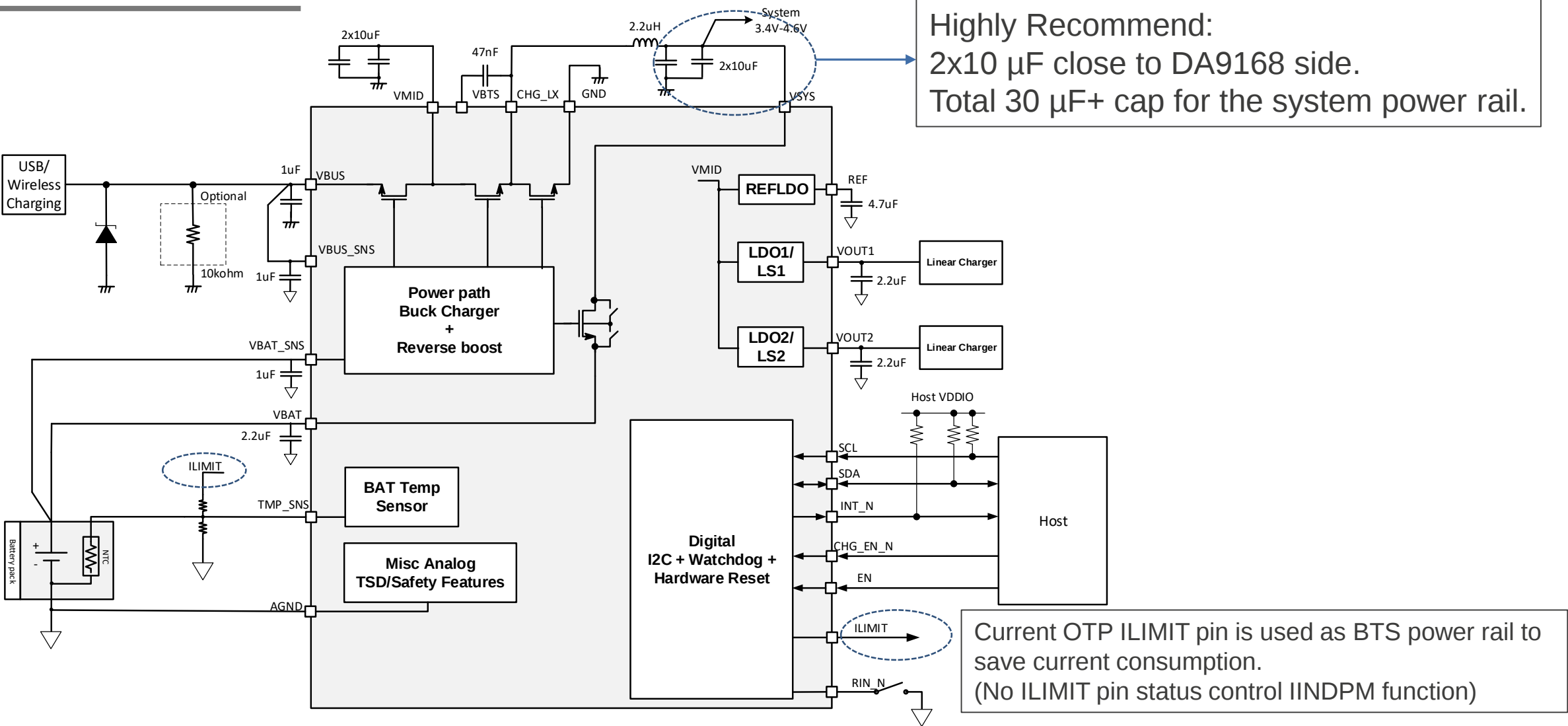


DA9168BC APPLICATION NOTE

FEB 2022

RENESAS ELECTRONICS CORPORATION

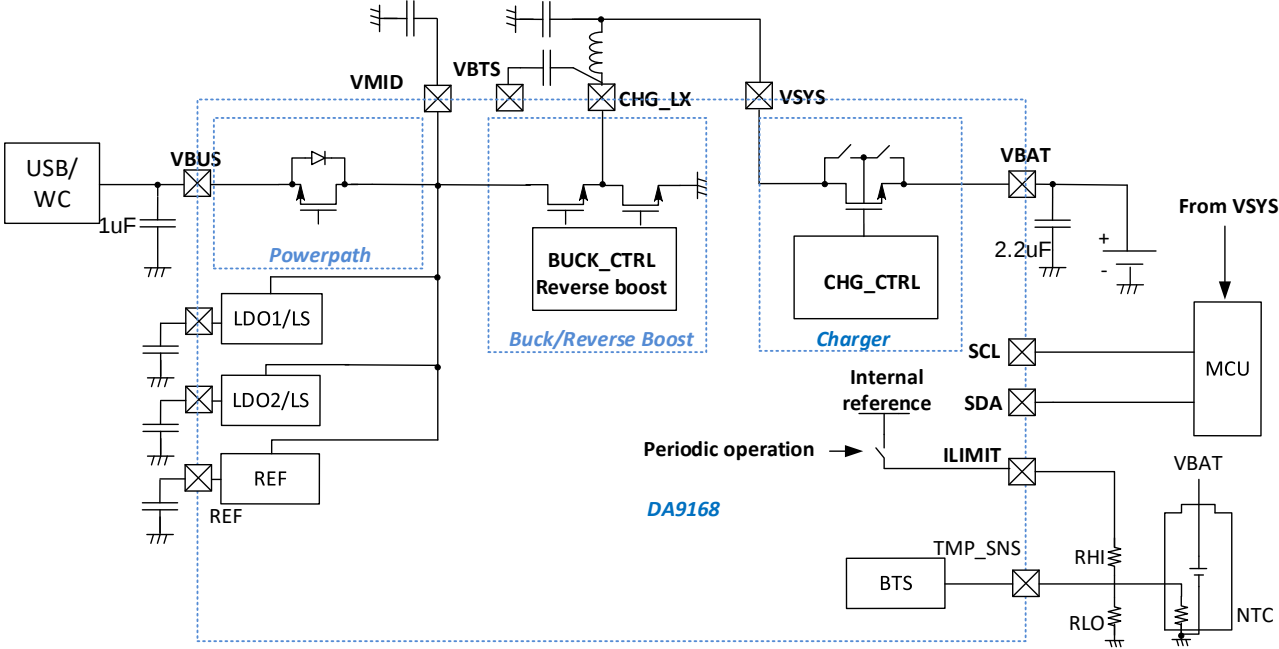
TYPICAL TWS APPLICATION WITH CURRENT OTP



DA9168 BTS WITH ILIMIT PIN

BTS WITH ILIMIT - VBUS IQ

Using ILIMIT pin (instead of REF)
for BTS has large I_Q savings

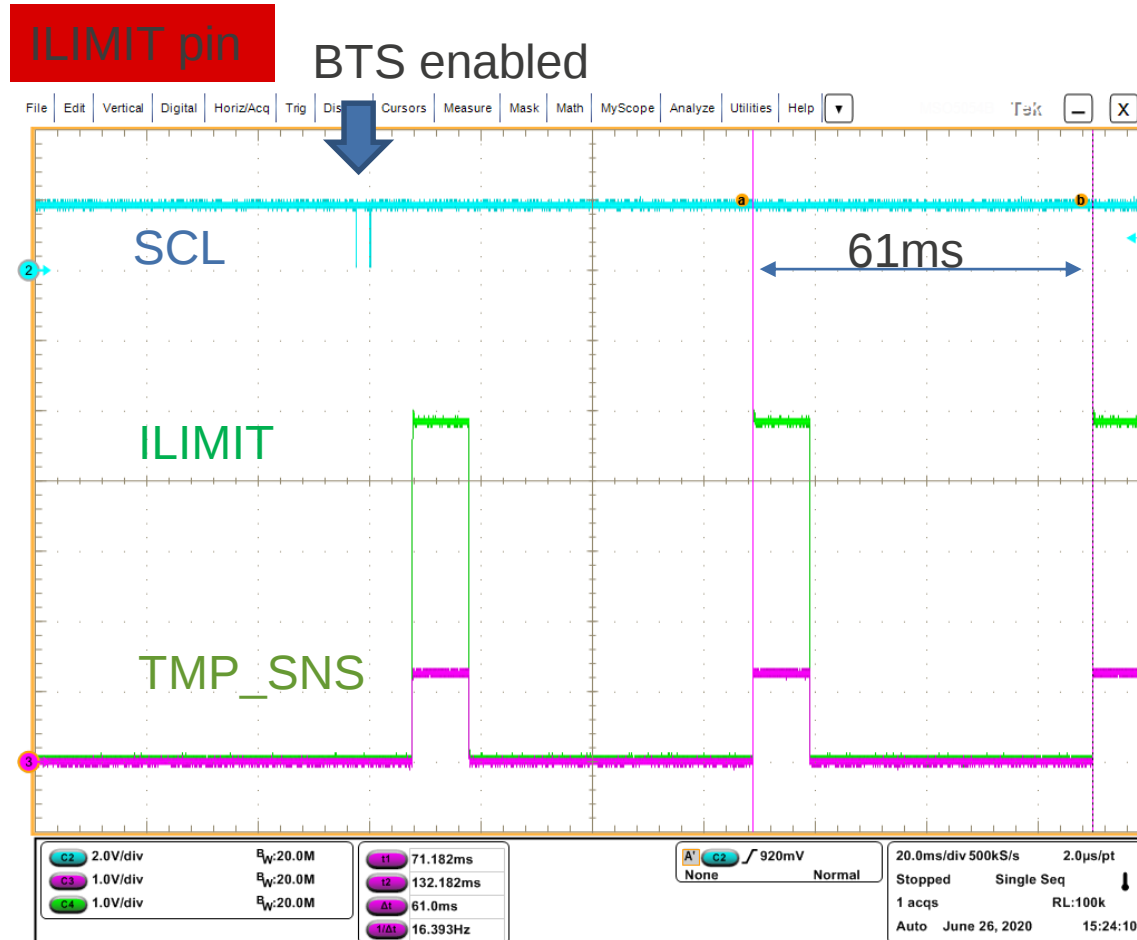


BTS Reference	BTS	Condition	I _Q from VBAT (μA)	Savings (μA)
REF	Disabled	Reverse boost + REFLDO	377	-
REF	Enabled	Reverse boost + REFLDO + BTS (50msec)	380	-
REF	Enabled	Reverse boost + REFLDO + BTS (2 sec)	377	-
ILIMIT	Disabled	Standby (boost disable)	10	367
ILIMIT	Enabled	Standby (boost disable) + BTS (50 msec)	41	339
ILIMIT	Enabled	Standby (boost disable) + BTS (2 sec)	11	366

I_Q increase
from BTS
just ~1 μA

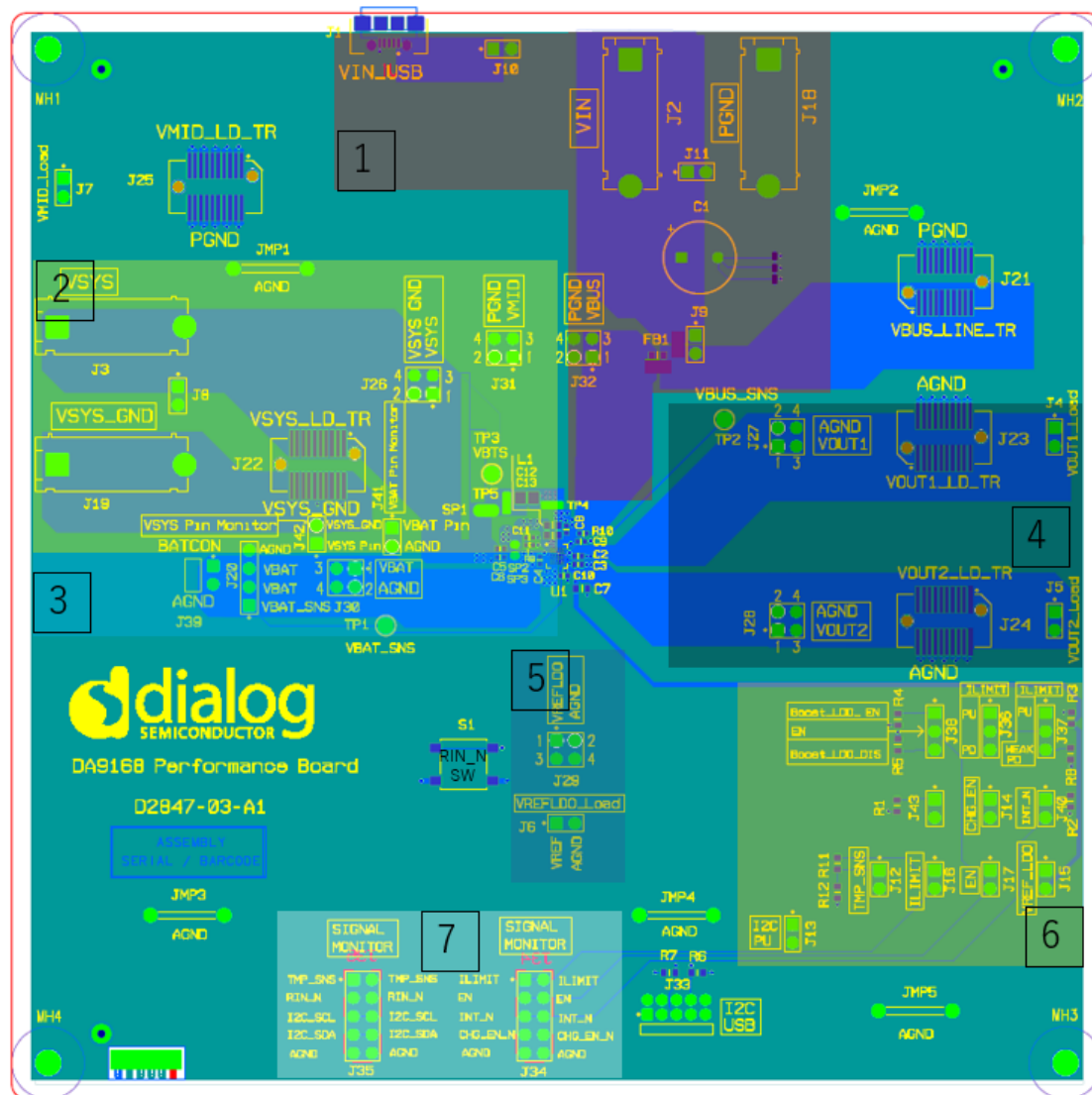
BTS WITH ILIMIT - PERIODIC OPERATION

- ✓ BTS periodic operation working as expected



DA9168 PERFORMANCE BOARD

PERFORMANCE BOARD OVERVIEW

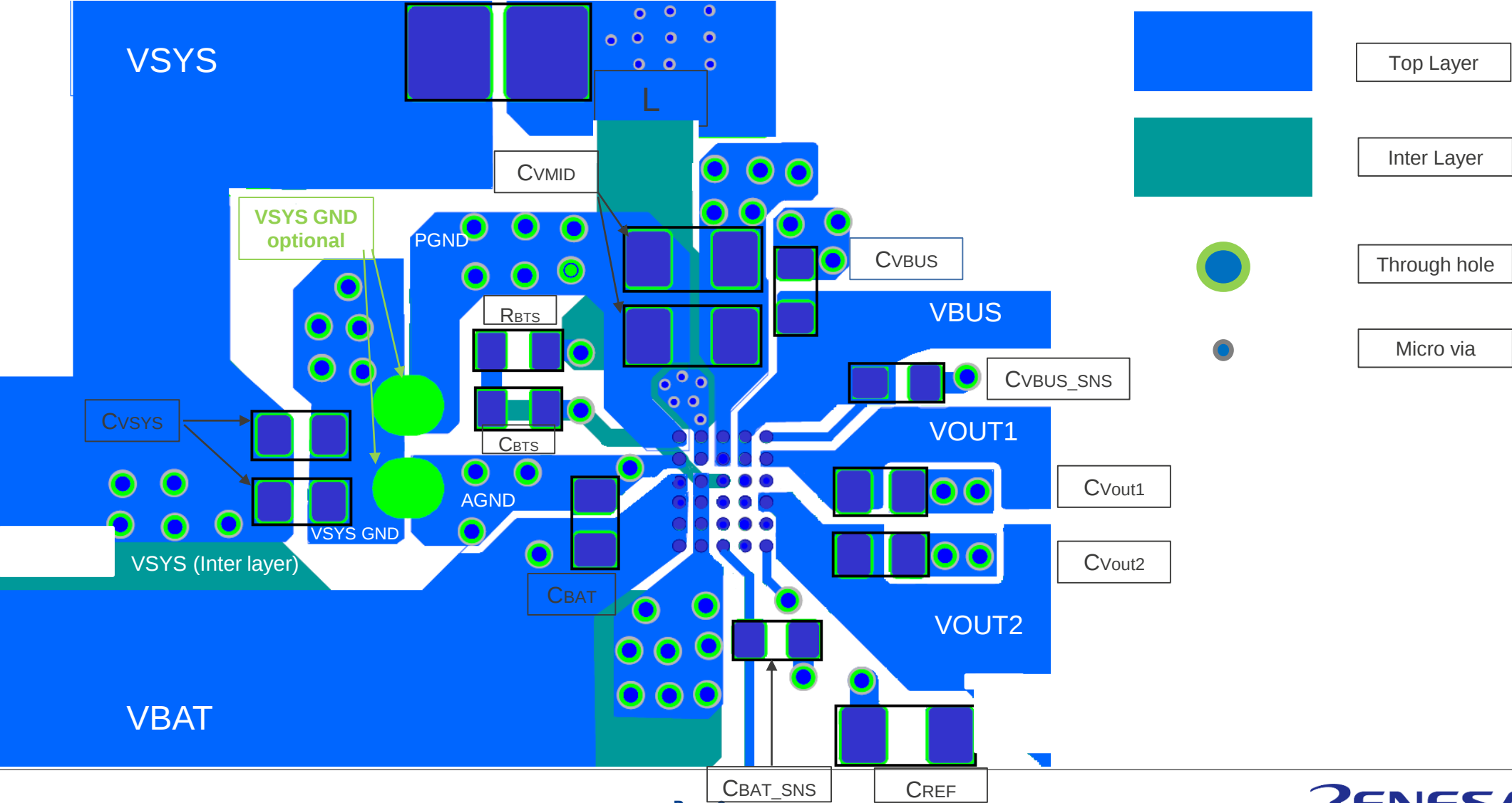


CAUTION

Apply high current to J26, J27, J28, J29, J30, J31, J32, J41 and J42 headers pin 1 and 2 may causes the voltage sensing traces burn out.

1. VBUS input section: Power supply and USB power supply connectors.
2. VSYS output section.
3. VBAT input/output section.
4. VOUT1 and VOUT2 outputs section.
5. REFLDO output section.
6. GPIOs network section.
7. GPIOs signal monitors section.

DA9168 PERFORMANCE BOARD LAYOUT CONCEPT



LAYOUT GUIDELINES

1. Minimize high frequency current path loop (VMID – CHG_LX – VSYS – GND and CHG_LX – VSYS - GND) to reduce EMI.
2. The two VMID capacitors (2x10 μ F) need to be placed as close as possible to the device DA9168.
3. The inductor input pin connected to GHG_LX pin should be as short as possible to reduce switching noise.
4. Make sure decoupling capacitors trace to the device pins as short as possible.
5. Split AGND (analog ground) and GND (power ground), and tie the analog ground and power ground with single ground connection.
6. For high current paths, ensure that the vias number and copper area is enough to support the operation current.

Note:

1. *Currently, there are two options for VSYS GND connection. Based on device evaluation results, recommend VSYS GND connect to AGND.*
2. *VBAT_SNS Capacitor can be removed if the battery connection is short enough.*

PERFORMANCE BOARD EXTERNAL COMPONENTS LIST

■ Inductors

Manufacturers	Part #	Size (mm)	Inductance (μ H)	Rdc (m Ω)		Heat Rating Current (A)		Saturation Current (A)	
				Typ	Max	Typ	Max	Typ	Max
Cyntec	HTEH20160H-1R0MSR	L = 2.0; W = 1.6 T = 0.8 (max)	1.0	29	35	4.4	4.0	4.0	3.6
Cyntec	HTEH20160H-2R2MSR	L = 2.0; W = 1.6 T = 0.8 (max)	2.2	75	90	2.6	2.3	2.9	2.7

PERFORMANCE BOARD EXTERNAL COMPONENTS LIST

■ MLCC

Manufacturers	Part #	Size (mm)	Height (mm)	Capacitance (μF)	Rated voltage	Temp characteristics	ESR @1 MHz (Ω)	Position
Murata	GRM155R6YA105KE11	1005	0.5 ±0.1	1.0 ±10%	35 V	X5R	0.01	VBUS VBUS_SNS (*VBAT_SNS)
Murata	GRM155R61A106ME11	1005	0.5 ±0.2	10.0 ±20%	10 V	X5R	-	VSYS(2x)
Murata	GRM188R61E106MA73D	1608	0.8 ±0.2	10.0 ±20%	25 V	X5R	-	VMID (2x)
Taiyo Yuden	TMK105BJ473KV-F	1005	0.55 (Max)	0.047±10%	25 V	X5R	0.1	VBTS
Murata	GRM155R61C225KE11	1005	0.5 ±0.2	2.2 ±10%	16 V	X5R	0.008	VBAT VOUT1 VOUT2
Murata	GRM155R61C105KA12	1005	0.5 ±0.05	1.0 ±10%	16 V	X5R	0.02	VBAT_SNS
Murata	GRM185R61C475KE11	1608	0.5 ±0.05	4.7 ±10%	16 V	X5R	0.006	VREF

DA9168 GUI

For GUI Install and Setup, please refer to document:
“UM_PM_051_DA9168_Performance_Board_User_Manual”

SYSTEM STATUS REGISTERS

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

System Status

System Events

Interrupt mask

System Status

PMC_STATUS_00

PMC_STATUS_01

PMC_STATUS_02

PMC_STATUS_03

PMC_STATUS_04

S_VBUS_VINDPM

S_VBUS_IINDPM

S_VMID_OC

S_VBAT_OC

S_VBUS_OK

S_VMID_OK

S_VSYS_OK

S_VBAT_OK

0x0000

0x07

S_VBUS_OV

S_VMID_OV

S_VSYS_OV

S_VBAT_OV

S_VBUS_UV

S_VMID_UV

S_VSYS_UV

S_VBAT_UV

0x0001

0x08

S_TSD_CRIT

S_TSD_WARN

S_WD_TIMER

S_TS_HOT

S_TS_WARM

S_TS_COOL

S_TS_COLD

S_TS_OFF

0x0002

0x00

S_CHG_SLEEP

S_CHG_SPLMT

S_CHG_TIMER

S_CHG_TRICKLE

S_CHG_PRE

S_CHG_CC

S_CHG_CV

S_CHG_DONE

0x0003

0x00

S_VSYS_SHUTDOWN

S_REF_OC

S_LDO2_IMON1

S_LDO2_IMON2

S_LDO2_OC

S_LDO1_IMON1

S_LDO1_IMON2

S_LDO1_OC

0x0004

0x00

VBUS not in VINDPM

VBUS not in IINDPM

VMID not in OC

VBAT not in OC

VBUS_OK

VMID_OK

VSYS_OK

VBAT_OK

VBUS not in OV

VMID not in OV

VSYS not in OV

VBAT not in OV

VBUS in UV

VMID not in UV

VSYS not in UV

VBAT not in UV

Below

Below

Watch-dog timer not

Battery temp sens...

Battery temp sens...

Battery temp sens...

Battery temp sens...

Battery temp sens...

Battery temp sens...

VBUS higher

VBAT fet not

Charge timer not

Charger not in trickle

Charger not

Charger not

Charger not

Charge termination...

VSYS not in SHUTDOWN

REF not in OC

LDO2 not in IMON1

LDO2 not in IMON2

LDO2 not in OC

LDO1 not in IMON1

LDO1 not in IMON2

LDO1 not in OC

Example: Rev-boost operation status

Read-only registers indicate device current status

Console Log

Clear Mark Save to file

Filter (reg expr):

Log level: Info

2021-12-14, 10:52:32 [INFO] poller stopped

2021-12-14, 10:53:08 [INFO] starting poller

2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0000, value: 0x0b <--

2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0001, value: 0x00 <--

2021-12-14, 10:53:13 [INFO] poller stopped

2021-12-14, 10:53:30 [INFO] DA9168 addr: 0x0013, value: 0x39 -->

2021-12-14, 10:53:35 [INFO] starting poller

2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0000, value: 0x07 <--

2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0001, value: 0x08 <--

2021-12-14, 10:53:37 [INFO] poller stopped

Bitfield Info

Bitfield: S_VSYS_UV

Register: PMC_STATUS_01 (0x1)

Bit: [1]

Access: R

POR: 0

Current Value: 0

Enumerated Value: VSYS not in UV

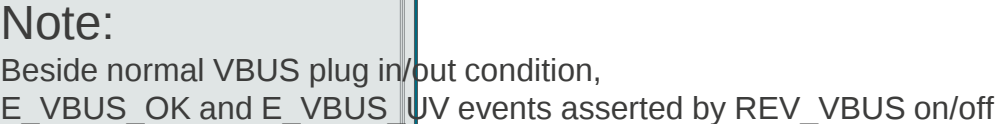
Chipmodel Blocks:

PMC: S_VSYS_UV

Description:

VSYS UV Status

Note:
Beside normal VBUS plug in/out condition,
S_VBUS_OK and S_VBUS_UV status flags by REV_VBUS on/off



INTERRUPT MASK REGISTERS

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

Interrupt mask bits

PMC_MASK_00	PMC_MASK_01	PMC_MASK_02	PMC_MASK_03
M_VBUS_VINDPM	M_VBUS_OV	M_TSD_CRIT	M_CHG_SLEEP
M_VBUS_IINDPM	M_VMID_OV	M_TSD_WARN	M_CHG_SPLMT
M_VMID_OC	M_VSYS_OV	M_WD_TIMER	M_CHG_TIMER
M_VBAT_OC	M_VBAT_OV	M_TS_HOT	M_CHG_TRICKLE
M_VBUS_OK	M_VBUS_UV	M_TS_WARM	M_CHG_PRE
M_VMID_OK	M_VMID_UV	M_TS_COOL	M_CHG_CC
M_VSYS_OK	M_VSYS_UV	M_TS_COLD	M_CHG_CV
M_VBAT_OK	M_VBAT_UV	M_TS_OFF	M_CHG_DONE
0x000A	0x000B	0x000C	0x000D

PMC_MASK_04

M_VSYS_SHUTDOWN
M_REF_OC
M_LDO2_IMON1
M_LDO2_IMON2
M_LDO2_OC
M_LDO1_IMON1
M_LDO1_IMON2
M_LDO1_OC
0x000E

INT_N signal masked for all events (Default) which means INT_N no react while these events triggered.

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

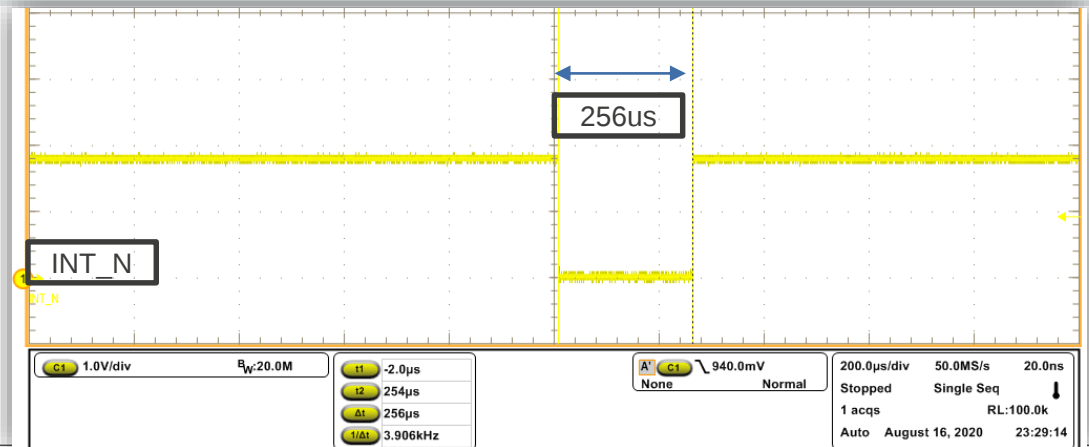
Interrupt mask bits

PMC_MASK_00	PMC_MASK_01	PMC_MASK_02	PMC_MASK_03
M_VBUS_VINDPM	M_VBUS_OV	M_TSD_CRIT	M_CHG_SLEEP
M_VBUS_IINDPM	M_VMID_OV	M_TSD_WARN	M_CHG_SPLMT
M_VMID_OC	M_VSYS_OV	M_WD_TIMER	M_CHG_TIMER
M_VBAT_OC	M_VBAT_OV	M_TS_HOT	M_CHG_TRICKLE
M_VBUS_OK	M_VBUS_UV	M_TS_WARM	M_CHG_PRE
M_VMID_OK	M_VMID_UV	M_TS_COOL	M_CHG_CC
M_VSYS_OK	M_VSYS_UV	M_TS_COLD	M_CHG_CV
M_VBAT_OK	M_VBAT_UV	M_TS_OFF	M_CHG_DONE
0x000A	0x000B	0x000C	0x000D

PMC_MASK_04

M_VSYS_SHUTDOWN
M_REF_OC
M_LDO2_IMON1
M_LDO2_IMON2
M_LDO2_OC
M_LDO1_IMON1
M_LDO1_IMON2
M_LDO1_OC
0x000E

Example: M_CHG_DONE register is set as "Not masked"



SYSTEM REGISTERS

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

System

Chip ID

OTP_DEVICE_ID
DEV_ID: 215
0x0042 0xD7

OTP_VARIANT_ID
MRC: 1
VRC: 0
0x0043 0x10

OTP_CONFIG_ID
CONFIG_REV: 0
0x0044 0x00

VSYS_OV_SHUTDOWN_DIS: Disable VSYS shutdown once VSYS_OV triggered
VSYS_UV_SHUTDOWN_DIS: Disable VSYS shutdown once VSYS_UV triggered
IINDPM_EN: IINDPM setting by ILIMIT pin option (Not support this function)
IINDPM_setting: 0.1 A to 2.5 A with 0.1 A/step

BTS_VBAT_RATE: BAT temp sense interval @ battery operation
BTS_VBAT_EN: Enable BAT temp sense @ battery operation
BTS_VBUS_RATE: BAT temp sense interval @ VBUS supply present
BTS_VBUS_EN: Enable BAT temp sense @ VBUS supply present
VBAT_DEB: VBAT detection debounce time (ms)
VBUS_DEB: VBUS detection debounce time (ms)

Read-on-clear event register function enable/disable

VSYS minimum voltage setting: 3.4 V to 3.7 V with 0.1 V/step

VINDPM setting: 3.8 V to 4.8 V with 0.1 V/step

System settings

PMC_SYS_00

E_RD_CLR_DIS: Low
VSYS_MIN: 3.7
VINDPM: 4.2
0x000F 0x38

PMC_SYS_01

VSYS_OV_SHUTDOWN...: System
VSYS_UV_SHUTDOWN...: System
ILIMIT_EN: No IINDPM update
IINDPM: 0.1
0x0010 0x00

PMC_SYS_02

BTS_VBAT_RATE: 50 ms
BTS_VBAT_EN: Disable
BTS_VBUS_RATE: 50 ms
BTS_VBUS_EN: Disable
VBAT_DEB: 100
VBUS_DEB: 100
0x0011 0x0A

PMC_SYS_03

SYS_WAIT: 1
WD_TMR: 160
WD_EN: No action
RST_TMR: 12
RST_REG: No action
0x0012 0x34

SYS_WAIT: VSYS power-off time for system power recovery cycle (s)
WD_TMR: watch-dog timer expire time (s)
WD_EN: watch-dog timer enable/disable
RST_TMR: RIN_N button press time (s) to reset the system
RST_REG: Triggers registers initialization

Boost operation mode option

Boost enable by EN pin option

VMID dummy-load setting (mA)

VMID dummy-load enable/disable

Reverse VBUS (OTG) enable/disable

Reverse boost enable/disable

PMC_SYS_04

BOOST_PWM: Auto-mode
SEQ_BOOST: BOOST_EN is set w...
DLOAD_VMID_SEL: 30
DLOAD_VMID_EN: Disable
REV_VBUS_EN: Disable
BOOST_EN: Disable
0x0013 0x38

PMC_SYS_05

REV_VBUS_ILIM: 1.0
BOOST_VOUT: 5.0
0x0014 0x9A

Reverse boost VOUT setting: 4.0 V to 5.5 V with 0.1 V/step

Reverse VBUS (OTG) current limit setting: 0.1 A to 1 A with 0.1 A/step

PMC_SYS_06

RST_SYS: No action
RIN_N_SHIP_EXIT_TMR: 20 ms
VBUS_OVSEL: 5.6
HIZ_MODE: VBUS when available
SHIP_DLY: 10
SHIP_MODE: No action
0x0015 0x06

System reset while set to high

RIN_N debounce time to exit from ship mode: 2 s/20 ms

VBUS over voltage threshold setting

HIZ mode option

Ship mode enter delay (s)

Ship mode enter/exit

Status

Console Log

Clear Mark Save to file Filter (reg expr): Log level: Info

2020-12-18, 10:43:42 [INFO] USB connected: U
2020-12-18, 10:43:42 [INFO] ready...
2020-12-18, 10:43:42 [INFO] Startup took: 0.90 sec
2020-12-18, 10:43:44 [INFO] no callables left to run...

Bitfield Info

Bitfield: WD_TMR
Register: PMC_SYS_03 (0x12)
Bits: [5:4]
Access: R/W
POR: 3
Current Value: 3
Enumerated Value: 160

CHARGER REGISTERS

BC Silicon New option at charging mode:

Recharge voltage threshold offset setting
0: 100 mV; 1: 200 mV

Charger safety timer rate reduced to half while relevant events triggered.

Charger safety timer enable/disable

Charger termination enable/disable

Charger enable/disable
(CHG_EN_N pin pulldown at the same time to enable charger)

CHG_TMR_SAFE: charger safty timer setting (h)

CHG_TMR_PRE: Pre-charge safty timer setting (min)

CHG_TOPOFF: Topoff timer setting (min) or disable

CHG_IPRE_MSB: Adds offset to pre-charge current setting (mA) while set to 1

CHG_RANGE_TERM: Charging current range settings for CHG_ITERM. For Higher range, CHG_RANGE need set to 1

CHG_RANGE_PRE: Charging current range settings for CHG_IPRE. For Higher range, CHG_RANGE need set to 1

CHG_ITERM: Termination charge current setting (mA)

CHG_IPRE: Pre-charge current setting(mA)

CHG_RANGE: Fast charge current range
0: 20 mA to 500 mA
1: 80 mA to 2000 mA

CHG_ICHG: Fast charge current setting

Fast charge current setting during TS event@ CHG_TS_COOL_I =1
CHG_RANGE = 0: TS_ICHG 20 mA to 500 mA
CHG_RANGE = 1: TS_ICHG 80 mA to 2000 mA

Battery regulation voltage setting: 4.0V to 4.5V with 10mV/step

- IO_INT_N_PD: INT_N pin internal pull-up
- IO_EN_PD: EN pin internal pull-down
- IO_CHG_EN_N_PD: CHG_EN_N pin internal pull-down
- TS_VBATREG_SHIFT: Battery regulation voltage shift down 100 mV/200 mV during temp sense warm event triggered @ CHG_TS_WARN_V=1

LDOS/LSWS REGISTERS

DA9168BC

File Tools Search View Help

DA9168

FUNCTIONAL REGISTERS SYSTEM CHARGER LDO Table View

LDO settings

PMC_LDO_00

LDO2_OCP: Disable
LDO2_PD: Enable
LDO2_LSW: LDO mode
LDO2_EN: Disable
LDO1_OCP: Disable
LDO1_PD: Enable
LDO1_LSW: LDO mode
LDO1_EN: Disable
0x001D: 0x44

PMC_LDO_01

SEQ_LDO1: LDO1 not enabled
LDO1_VOUT: 3.0
0x001E: 0x22

PMC_LDO_02

SEQ_LDO2: LDO2 not enabled
LDO2_VOUT: 3.0
0x001F: 0x22

PMC_LDO_04

SYS_WAIT_CFG: Default setting
RST_OPT_PWRCYC: Triggers power-cycle
SHIP_DLY_DIS: After SHIP_DLY
RST_OPT: On RIN_N rise
VBAT_OV_CFG: Shut-down
CHG_TRICKLE_CYC: Cyclic mode enabled
CHG_TRICKLE: 14 / 7
0x0021: 0x55

PMC_LDO_05

LDO2_ILIM: 487
LDO1_ILIM: 487
0x0022: 0xAA

LDOx sequence option:
0: LDOx not enabled by EN pin
1: Enable LDOx ASAP after EN pin rise
2: Enable LDOx 0.25 ms after EN pin rise
3: Enable LDOx 0.5 ms after EN pin rise

LDOx OCP option:
0: LDOx disable while trigger OCP
1: LDOx hiccup while trigger OCP

LDOx PD SW option:
0: LDOx PD switch disable
1: LDOx PD switch enable

LDOx_LSW mode option:
0: LDO mode
1: Load SW mode

LDOx_EN:
0: LDOx disable
1: LDOx enable

LDOx VOUT setting:
1.6 V to 5.2 V with 0.1 V/step

LDOx current limit setting

New options for BC silicon

Console Log

Clear Mark Save to file Filter (reg expr): Log level: Info

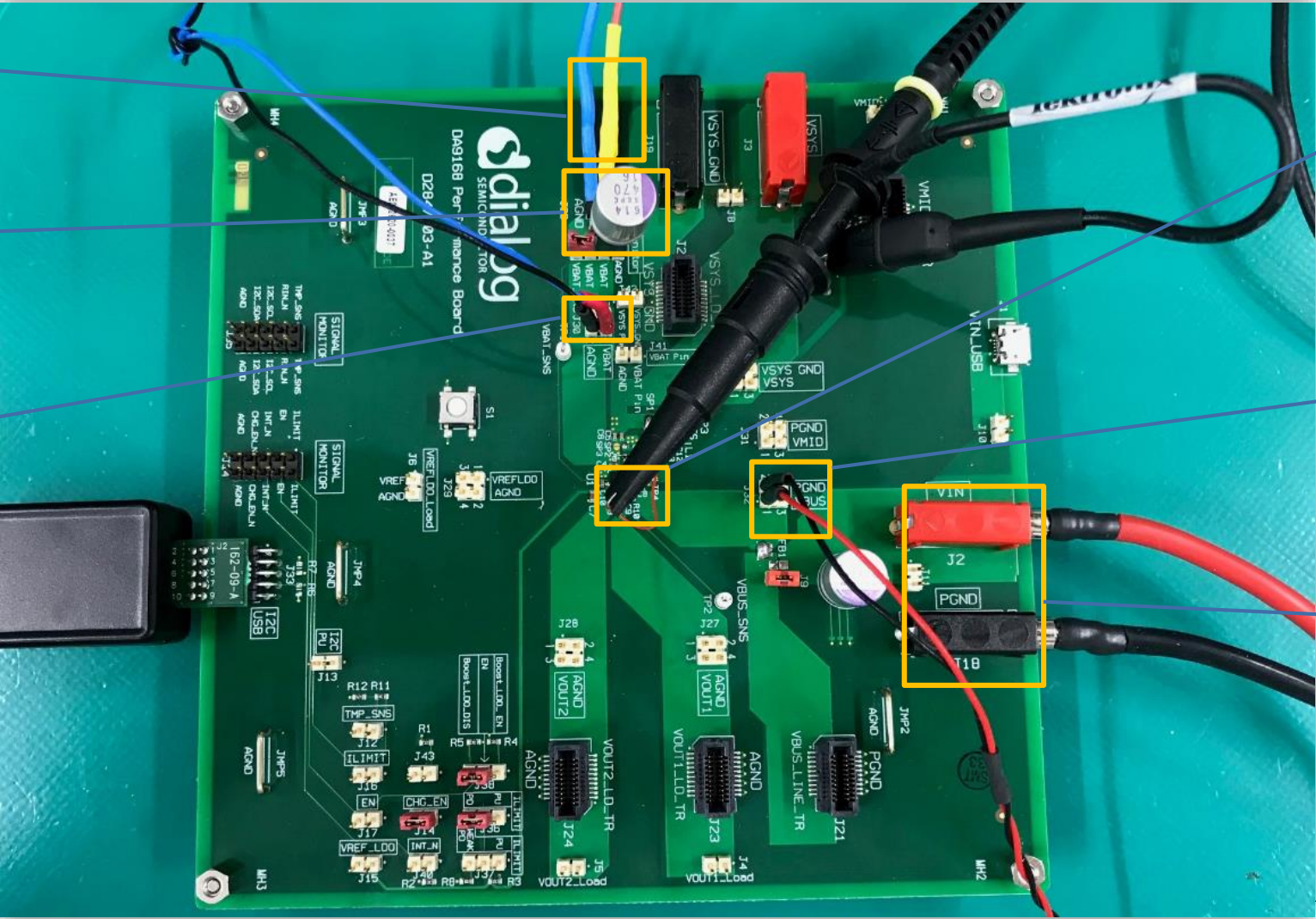
2021-12-14, 10:52:32 [INFO] poller stopped
2021-12-14, 10:53:08 [INFO] starting poller
2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0000, value: 0x0b <--
2021-12-14, 10:53:08 [INFO] DA9168 addr: 0x0001, value: 0x00 <--
2021-12-14, 10:53:13 [INFO] poller stopped
2021-12-14, 10:53:30 [INFO] DA9168 addr: 0x0013, value: 0x39 -->
2021-12-14, 10:53:35 [INFO] starting poller
2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0000, value: 0x07 <--
2021-12-14, 10:53:35 [INFO] DA9168 addr: 0x0001, value: 0x08 <--
2021-12-14, 10:53:37 [INFO] poller stopped

Bitfield Info

Bitfield: LDO1_ILIM
Register: PMC_LDO_05 (0x22)
Bits: [3:0]
Access: R/W
POR: 13
Current Value: 10
Enumerated Value: 487
Chipmodel Blocks:
PMC: LDO1_ILIM
Description:
VOUT1 current limit (mA)

TEST BENCH SETUP

CHARGE MODE BOARD SETUP



VBAT Connection

VLX Signal

VBUS Sense

VBUS Connection

Highly recommend:
Bulk electrolytic cap for
VBAT connector to prevent
VBAT voltage oscillation due
to the long cable

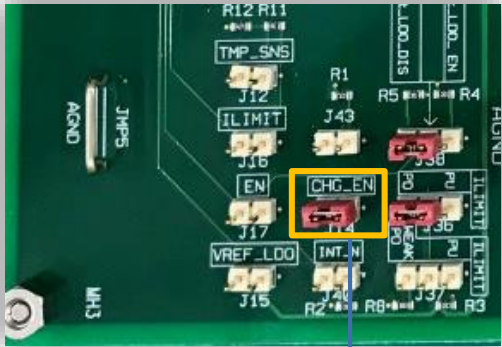
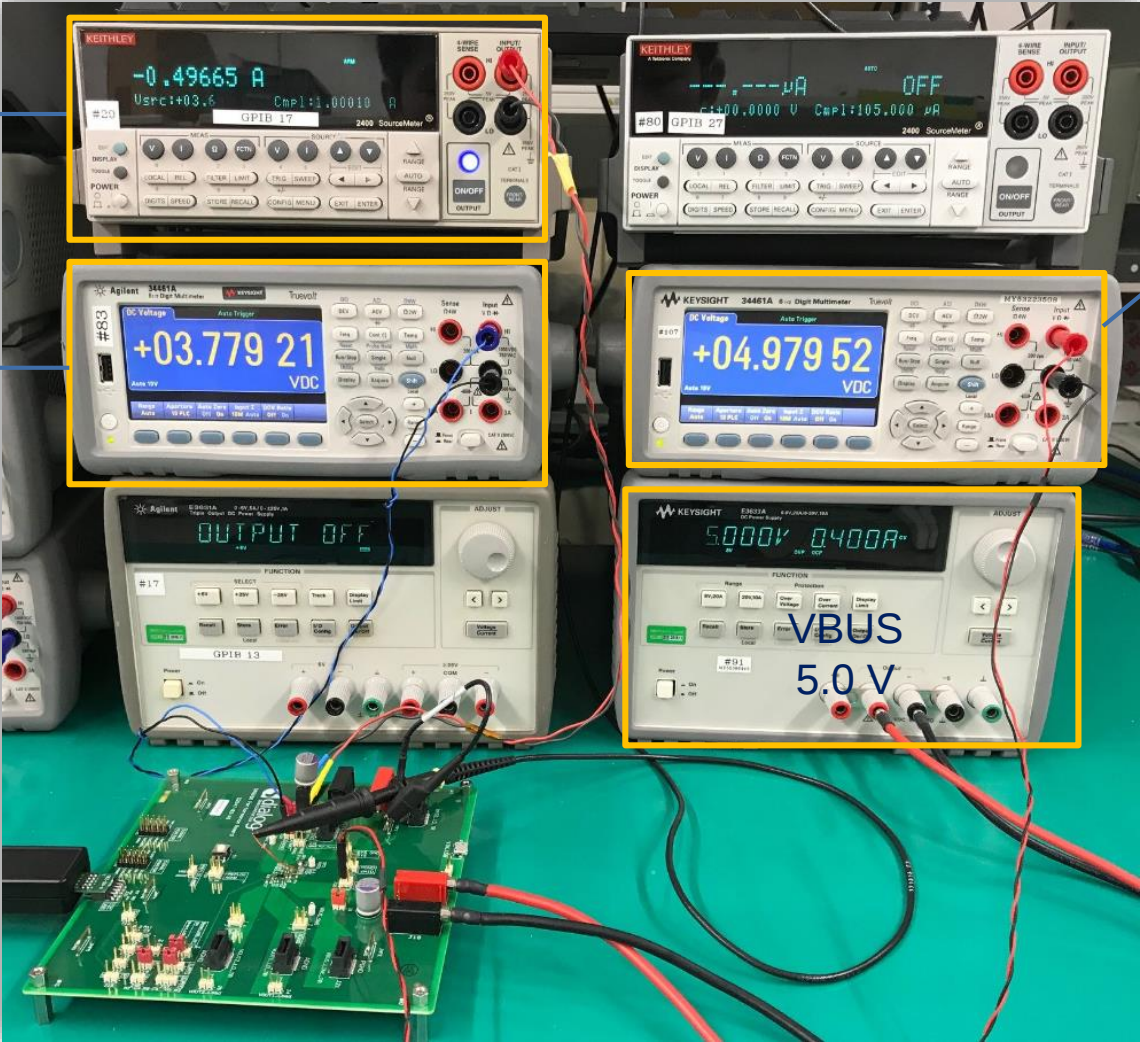
VBAT Sense

CHARGE MODE TEST BENCH SETUP

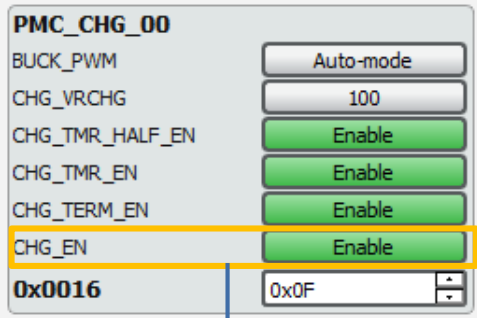
VBAT charging current

VBAT Sense
3.779 V

VBUS Sense
4.979 V

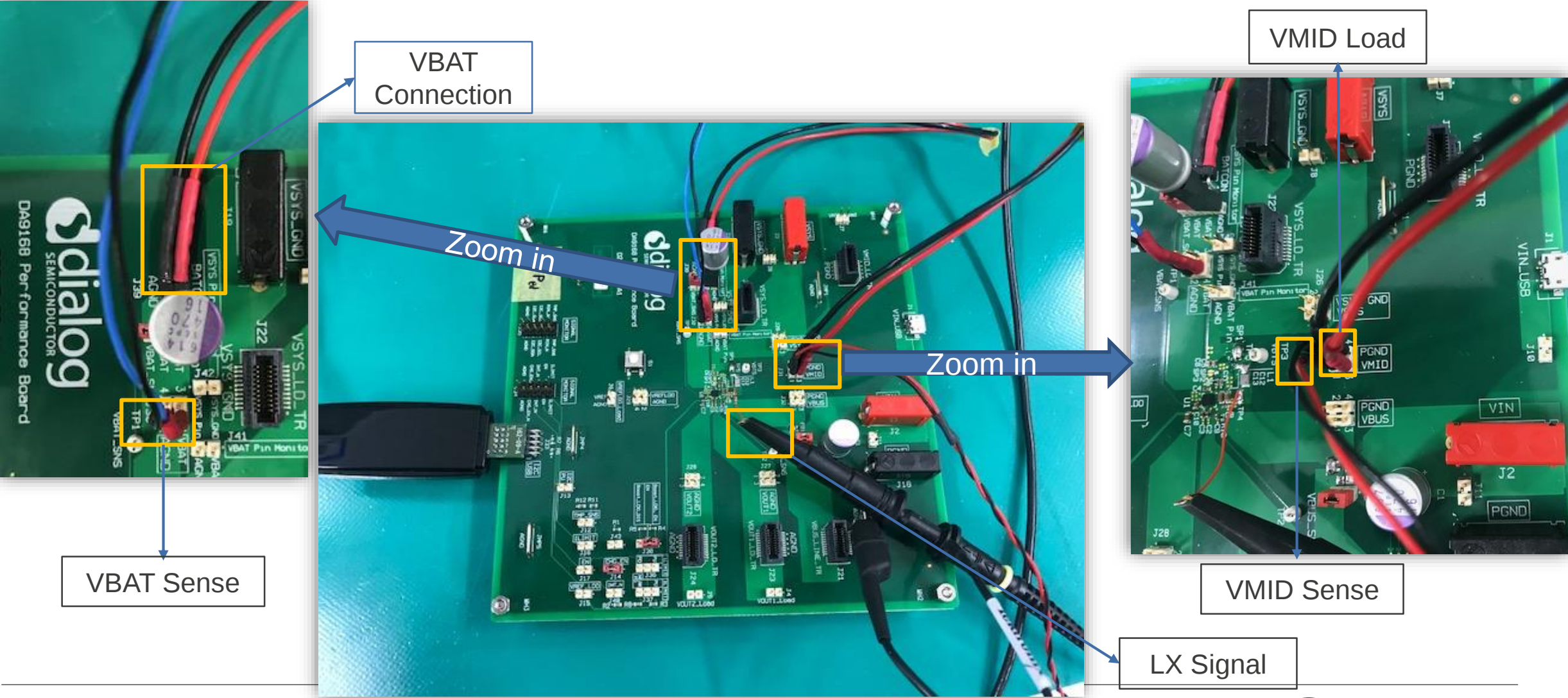


CHG_EN_N pin pulldown



CHG_EN set to High

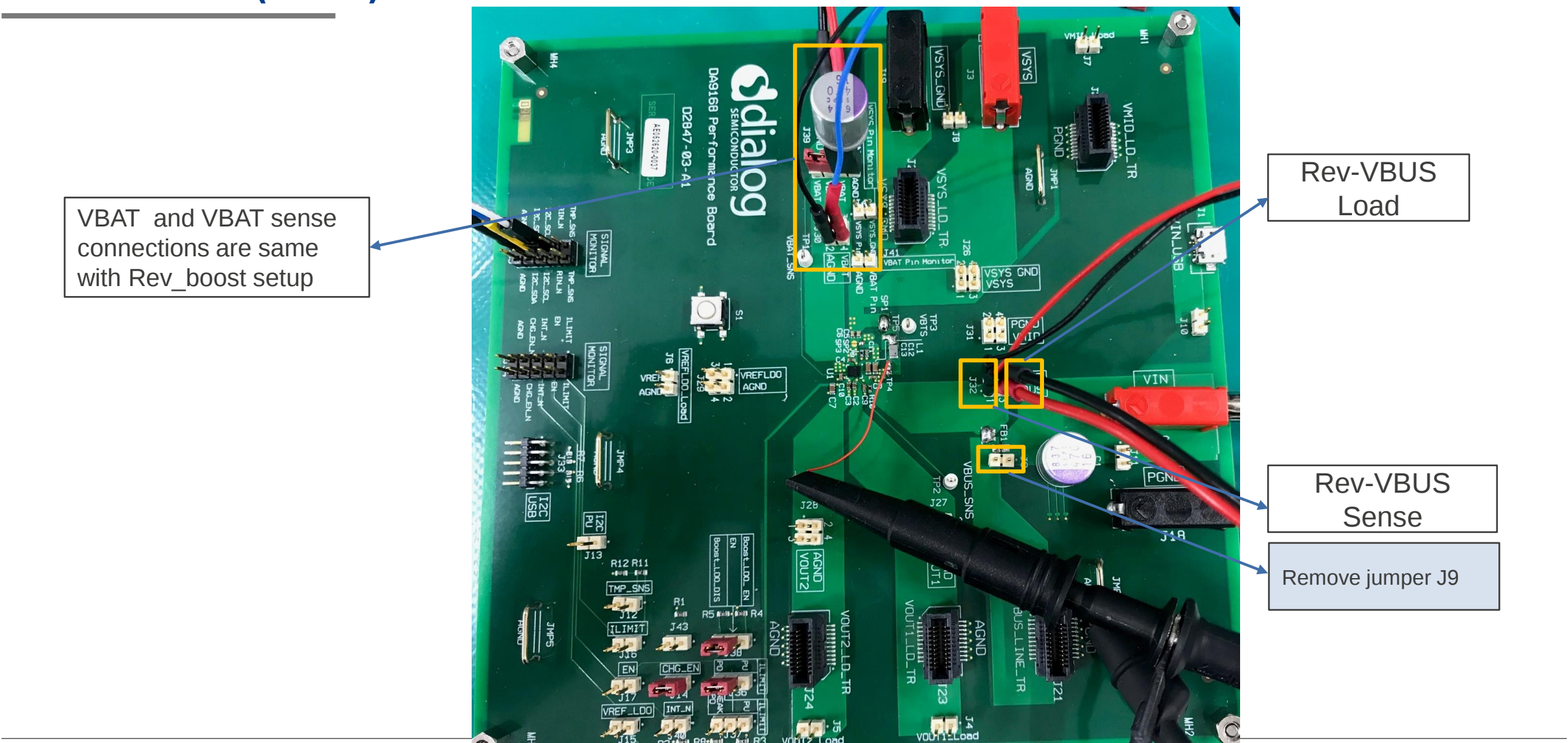
REV-BOOST MODE BOARD SETUP



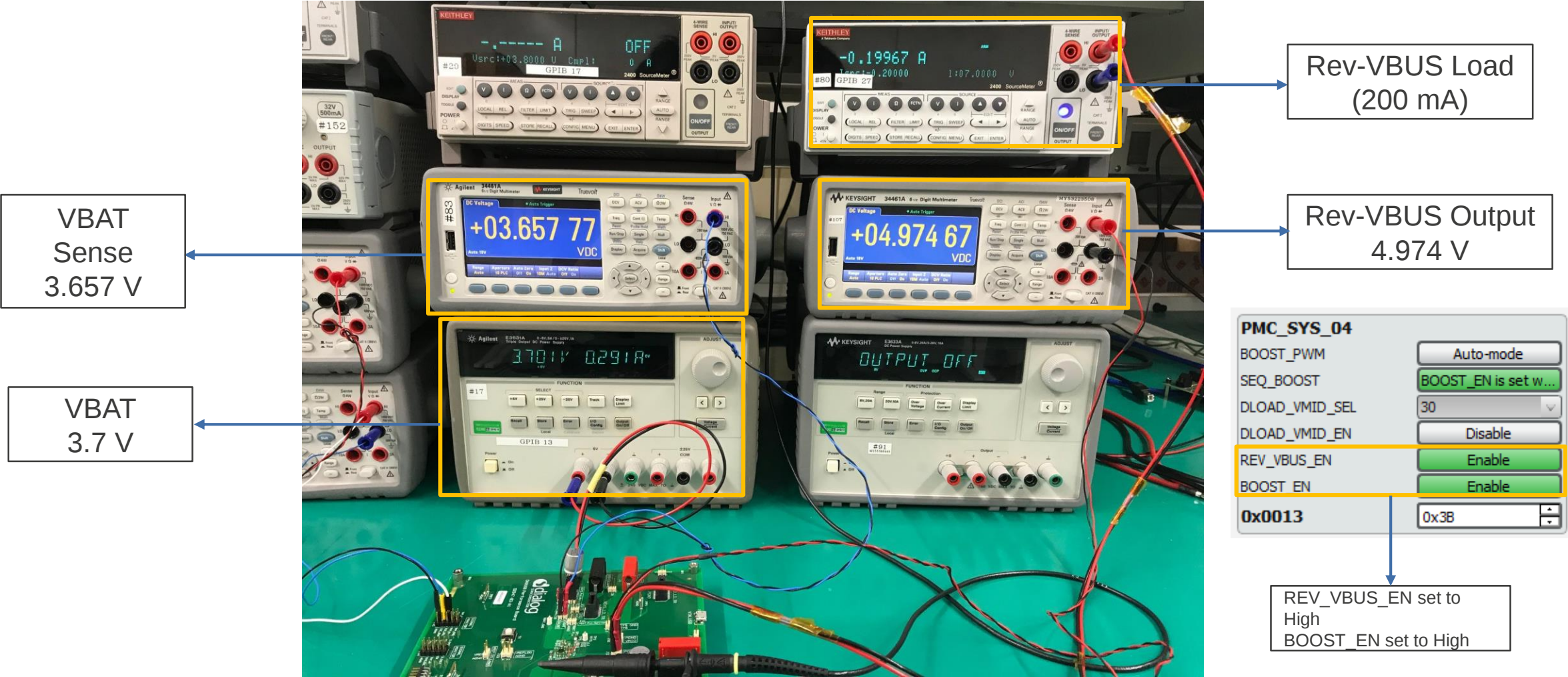
REV-BOOST MODE TEST BENCH SETUP



REV-VBUS (OTG) BOARD SETUP



REV-VBUS (OTG) TEST BENCH SETUP



[Renesas.com](https://www.renesas.com)