Schematic Checklist - DA9213/14/15, DA9213-A/14-A/15-A, DA9223-A/24-A

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1. Terms and Definitions

BGA	Ball grid array
CPU	Central processing unit
GUI	Graphical user interface
IC	Integrated circuit
OTP	One-time programmable memory
PCB	Printed circuit board
PMIC	Power management integrated circuit
WLCSP	Wafer level chip scale packaging

2. References

[1] DA9213_14_15 Datasheet, Renesas Electronics

[2] DA9213_14_15 Auto Datasheet, Renesas Electronics

[3] DA9223_24 Auto Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

DA9213, DA9214, DA9215, DA9223-A, and DA9224-A are PMUs optimized for the supply of CPUs, GPUs, and DDR memory rails in smartphones, tablets and other portable applications. The fast transient response (10 A/µs) and load regulation are optimized for the latest generation of multi core application processors.

DA9213 operates as a single four-phase buck converter delivering up to 20 A output current.

DA9214 integrates two dual-phase buck converters, capable of delivering 2 x10 A output current.

DA9215 integrates a three-phase buck converter capable of delivering 15 A and a single-phase buck converter delivering 5 A output current.

DA9223 operates as a single four-phase buck converter delivering up to 16 A output current.

DA9224 integrates two dual-phase buck converters, capable of delivering 2 x 8 A output current.

This checklist is intended to help a hardware engineer identify common errors that can arise in schematics containing DA9213_14_15_23_24. The checklist is only a reference to common errors, and is not a substitute for rigorous system development and an understanding of the PMUs behaviour as described in the DA9213/4/5 datasheet.

This checklist can also be used for DA9213-A, DA9214-A, and DA9215-A PMUs.

4. Schematic Checklist

Table 1. Checklist

General	Comments				
Design Name					
Schematic Version					
Review Date					
Circle sub PMIC being used	DA9213	DA9214	DA9215	DA9223	DA9224

OTP Variant	Notes	Checked (Y/N)	Comments
Which OTP variant is being used			
OTP Version Number			

Core Operation	Notes	Checked (Y/N)	Comments
V_{SYS}	2.8 V to 5.5 V		
V_{DDIO}	1.2 V to 3.6 V Note 1		
V_{DDCORE} capacitor	150 nF		
V_{DDIO} capacitor	100 nF		
V_{SYS} capacitor	1 µF		
V_{DD_BUCKx} capacitor	10 µF per phase		
V_{OUT_BUCKx} capacitor	47 µF per phase		
BUCKx indcutor	0.22 µH		
Phase connection	DA9213: BuckA: all phases Pins B1-B4, B8-B11, E1-E4, E8-E11		
	DA9214: BuckA: Phases A1/A2 Pins B1-B4, E1-E4 BuckB: Phases B1/B2 Pins B8-B11, E8-E11		
	DA9215: BuckA: Phases A1/A2/B2 Pins B1-B4, E1-E4, E8-E11 BuckB: Phase B1 Pins B8-B11		
FBAP/FBAN remote sense	Connect to output capacitor Pins C5, D5		
FBBP/FBBN remote sense	For DA9214/5 only. Pins C7, D7 Leave floating for DA9213		
FBAP/FBAN glitch capacitor	2.2 nF		

Core Operation	Notes	Checked (Y/N)	Comments
FBBP/FBBN glitch capacitor	2.2 nF (for DA9214/5 only) Leave floating for DA9213		
V_{SS} to V_{SS_ANA} resistor	1 k between pin E5 to E6		
Q_{GND} separate from P_{GND}	Connect V_{SYS}, V_{DDIO} and V_{SS_ANA} capacitors to Q_{GND} Pin E6, E7 and F6		
Resisitive Divider	Total resistance < 30 k from FBxP to FBxN and 1 nF capacitor across upper resistor if used.		
I^2C pull up resistors	Pin A5 and A6. Each signal has < 4k7 pull-up if used.		
nIRQ pull up resistor	Pin F5. Required if used and Open Drain output in OTP		
IC_EN	Pin F7. Needs to be pulled high to enable device operation		
GPIO0	Pin A7. Do OTP settings match GPIO connections		
GPIO1	Pin B7. Do OTP settings match GPIO connections		
GPIO2	Pin B6. Do OTP settings match GPIO connections		
GPIO3	Pin C6. Do OTP settings match GPIO connections		
GPIO4	Pin D6. Do OTP settings match GPIO connections		

Note 1 V_{DDIO} is not allowed to be higher than V_{SYS}

5. Further Assistance

For further assistance on debugging and for a detailed schematic and OTP check, please refer to the combined DA9213/4/5 or DA9223/4 datasheets found on the Renesas website (https:\\www.renesas.com) or contact your local FAE.

6. Revision History

Revision	Date	Description
01.00	Nov 21, 2025	First version.

STATUS DEFINITIONS

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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