Application Note

DA9281 PCB Layout Recommendations

AN-PM-180

Abstract

This application note provides recommendations on how to place and route DA9281 device. It also gives guidance on the passive components needed for proper functioning of the system. This document is a guideline only; target applications may have different requirements.

Contents

Figures

Tables

© 2025 Renesas Electronics

1 Terms and Definitions

CH<x>	Channel <x>, where x = 1 to 8
DDR	Double data rate (memory)
GND	Ground
IC	Integrated circuit
LDO	Low drop out
PCB	Printed circuit board
QFN	Quad Flat-pack No-lead (package)
VTT	Termination voltage (memory)

2 References

[1] DA9281_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

© 2025 Renesas Electronics

3 Introduction

Renesas Electronics' DA9281 is an 8-channel power management integrated circuit (PMIC) with 4 buck regulators, 3 LDOs, and 1 voltage buffer to support DDR VTT termination. All 8 channels have an output discharge function and protection features such as over-current protection (OCP), over voltage protection (OVP), and under voltage protection (UVP).

The input voltage range of 4.5 V to 5.5 V makes it suited for a wide range of low voltage systems. The Buck channel output voltages are programmable as follows; CH1 from 0.8 V to 3.0 V, CH3 from 0.8 V to 3.6 V, and CH2/CH4 from 0.8 V to 3.3 V. The Termination Voltage Regulator's output can be set to 1.2 V or 1.35 V. For more information, please see DA9281's datasheet [1].

The recommended components and connections for DA9281 is shown in Figure 1.

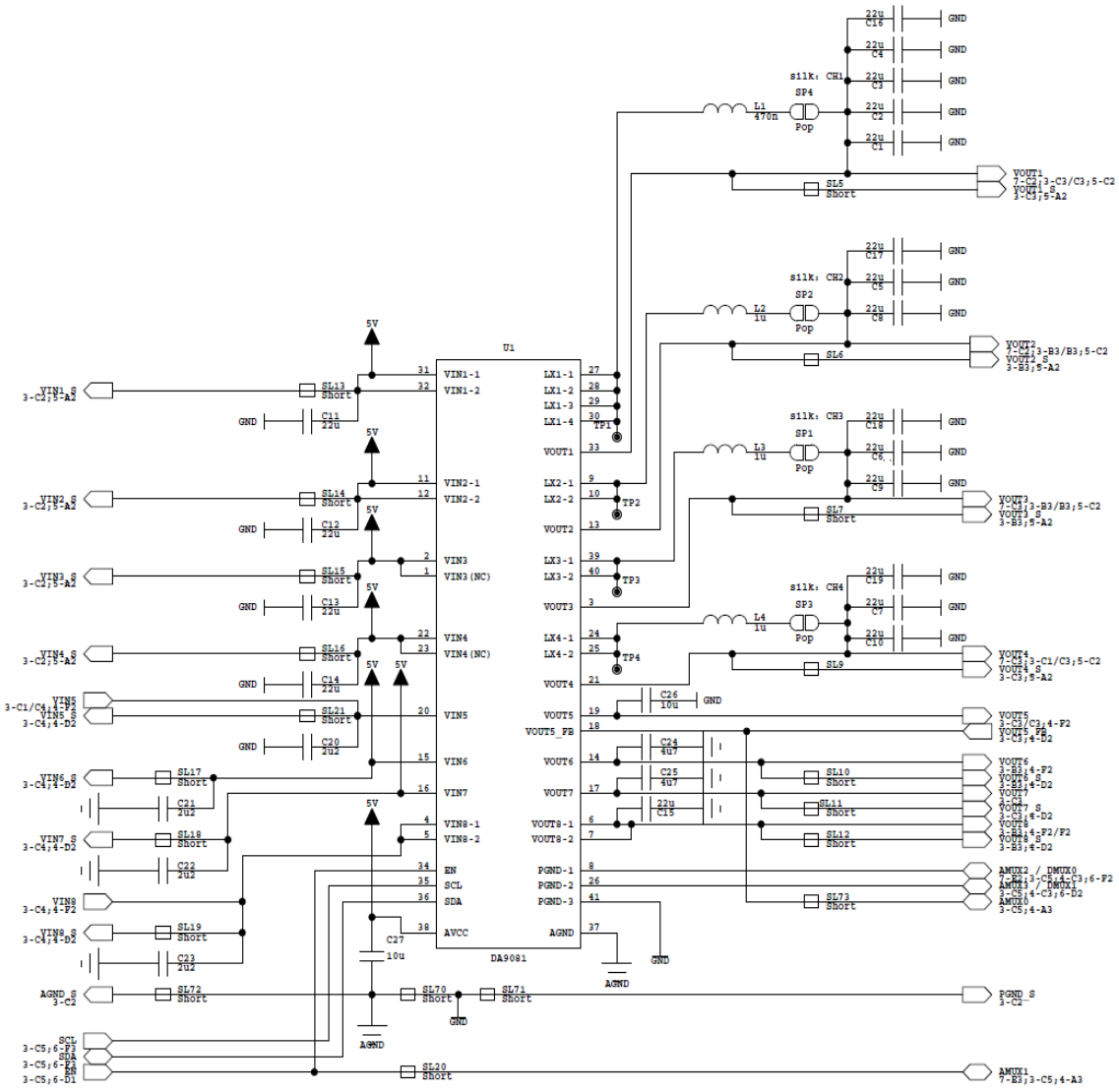


Figure 1: DA9281 Recommended Components and Connections

© 2025 Renesas Electronics

DA9281 PCB Layout Recommendations

Table 1: DA9281 Recommended Components

Application	Part Reference	Value	Temp. Char.	Voltage Rating	ISAT and ITEMP
CAVCC	C27	10 µF	X5R or better	10 V or above	N/A
CVIN1, CVIN2, CVIN3, CVIN4	C11, C12, C13, C14	22 µF	X5R or better	16 V or above	N/A
CVIN5, CVIN6, CVIN7, CVIN8	C20, C21, C22, C23	2.2 µF	X7R or better	10 V or above	N/A
CVOUT1, CVOUT2, CVOUT3, CVOUT4	C1, C2, C3, C16, C5, C8, C17, C6, C9, C18, C7, C10, C19	22 µF	X5R or better	16 V or above	N/A
CVOUT5	C26	10 µF	X5R or better	6.3 V or above	N/A
CVOUT6, CVOUT7	C24, C25	4.7 µF	X5R or better	16 V or above	N/A
CVOUT8	C15	22 µF	X5R or better	16 V or above	N/A
LOUT1	L1	470 nH	N/A	N/A	7.4 A ISAT typical or above
LOUT2, LOUT3, LOUT4	L2, L3, L4	1 µF	N/A	N/A	5.3 A ISAT typical or above

© 2025 Renesas Electronics

4 Layout Recommendations

DA9281 comes in a 5.0 x 5.0 mm 40-pin QFN package with a 0.4 mm pitch.

Although the PCB layout recommendations described in this application note is with reference to the Renesas Electronics' DA9281 Evaluation Board, a six-layer PCB, the required number of routing layers and other PCB parameters are also determined by the other devices in the system.

4.1 DA9281 Package Information

4.1.1 Pinout

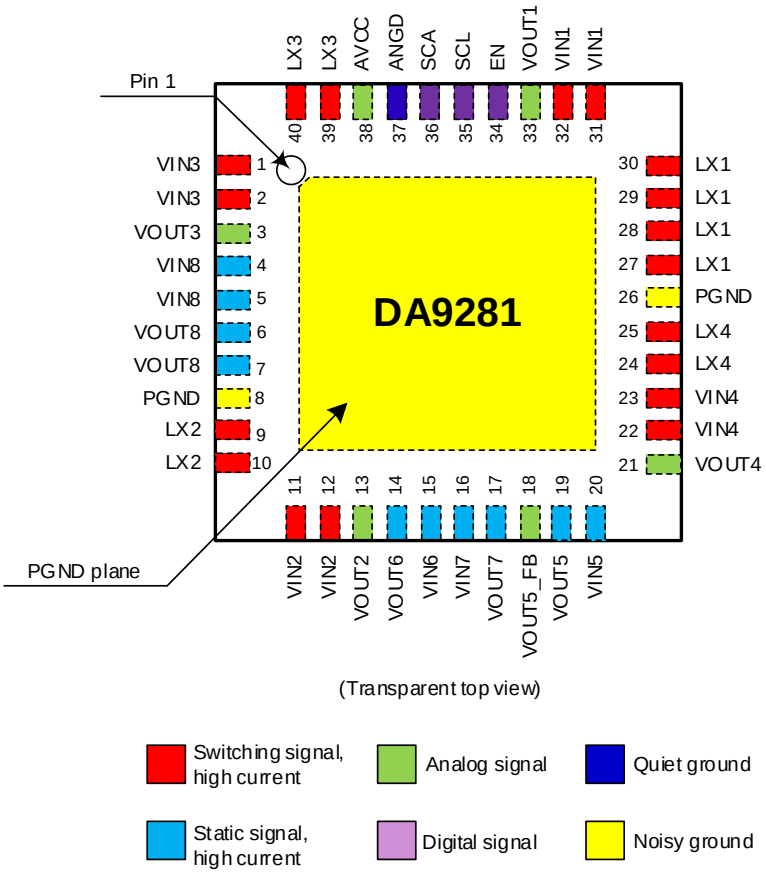
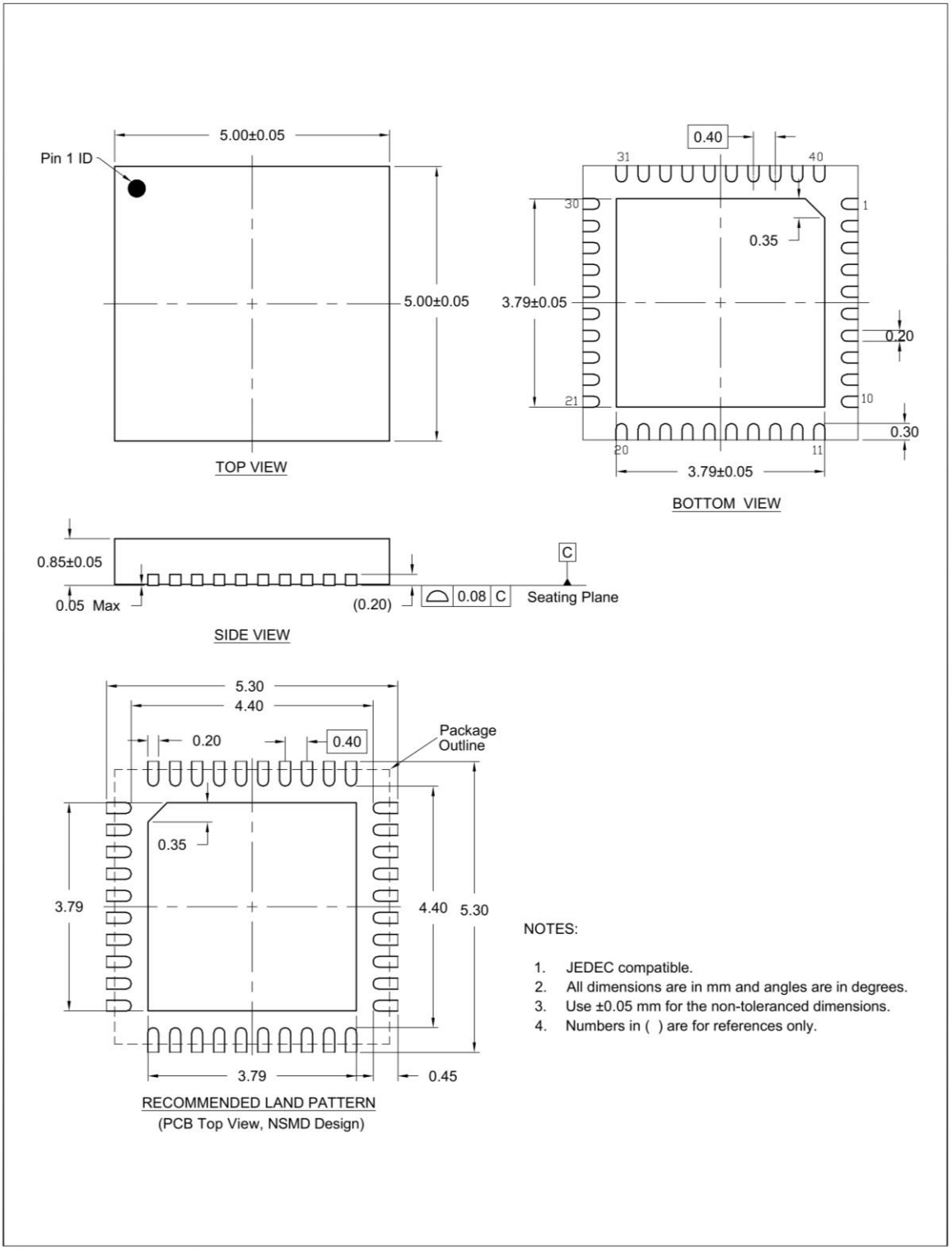


Figure 2: DA9281 QFN Pinout Diagram (Top View)

© 2025 Renesas Electronics

Package Outline Drawing

PSC-5138-01
QW0040AB
40-QFN 5.0 x 5.0 x 0.85 mm Body, 0.40 mm Pitch
Rev00, Feb 19, 2025



© Renesas Electronics Corporation

Figure 3: QFN 40L Package Outline Drawing

4.2 Buck Converter, VTT and LDO

4.2.1 Input Decoupling

In a buck converter layout, the input capacitor location is critical. Locate the input capacitor as close as possible to the device's input and power GND pins to minimize the parasitic inductance.

In the DA9281 layout design, the input capacitor for each CH<x> should be placed as close as possible to the VIN<x> and PGND<x> pins, and on the same layer as the DA9281 device.

If multiple layers are used, it is recommended to use as many as possible microvias (or through-hole vias) to minimize line resistance.

Figure 4 shows the input capacitor placement and routing recommendation.

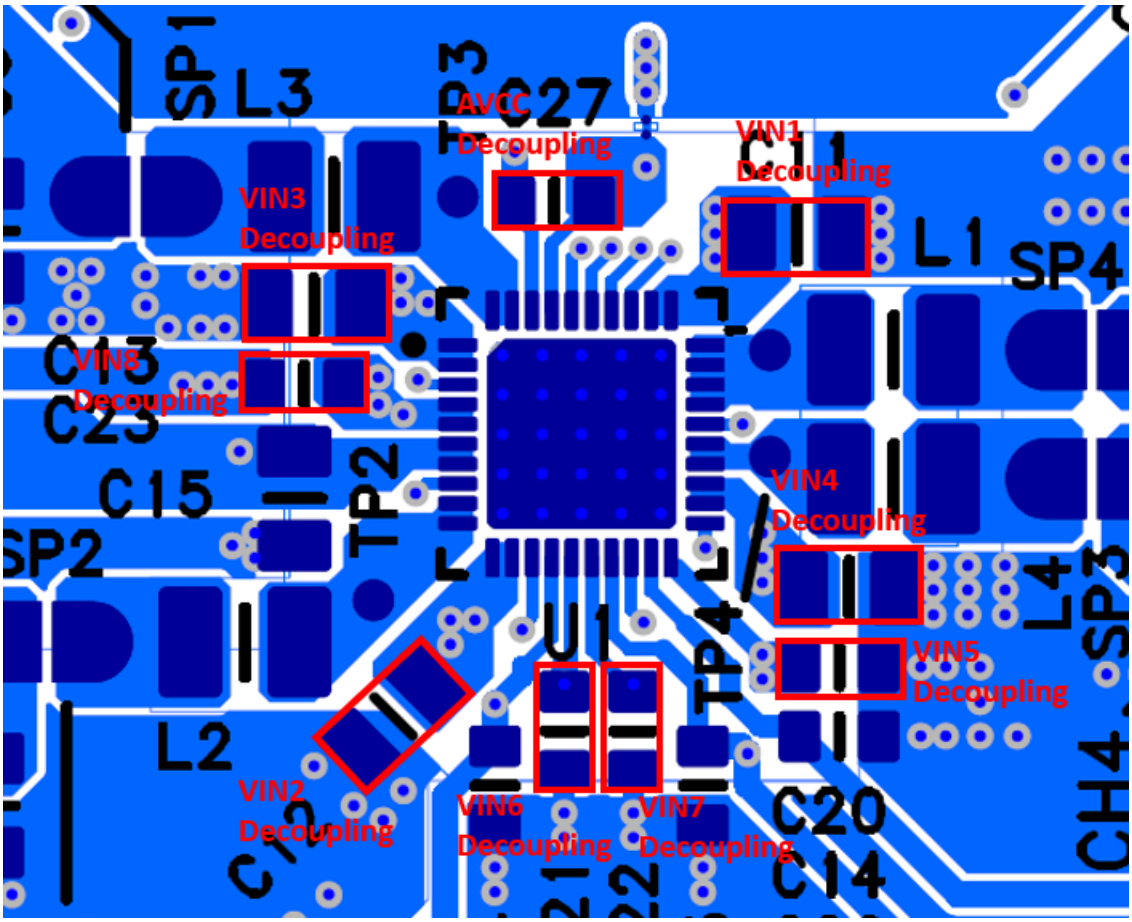


Figure 4: Recommended CH<x> and AVCC Input Capacitors Placement and Routing

Trace impedances for the VTT (CH5) and LDOs (CH6, CH7 and CH8) input connections should be minimized to reduce drop-out and effects on load regulation.

© 2025 Renesas Electronics

4.2.2 Ground Connections

Particular care should be taken with ground connections because of the high current capability of DA9281 and because of the device's high-performance requirements.

The power PGND terminals (PGND<x>) of the DA9281 are placed conveniently to allow the placement of the VIN<x> decoupling capacitors as close as possible to the device.

It is best practice to isolate quiet analog GND (AGND) from noisy power GND terminals (PGND<x>).

On the Renesas Electronics' DA9281 Evaluation Board, AGND is isolated from the power GND terminals (PGND<x>) on the top layer (component layer) and connected to GND on layer 2.

Layer 2 can be used as a return power GND plane, where the device's power GND pins (for CH<x>) and output capacitor GND can be connected. It is recommended to minimize the line impedance of the power GND pins and output capacitor GND connections by using as many vias as possible. This will also improve the heat dissipation.

NOTE
It is always recommended to use copper plugged vias to achieve the minimum parasitic via impedance and best thermal performance.

Example of GND terminals connection is illustrated in Figure 5.

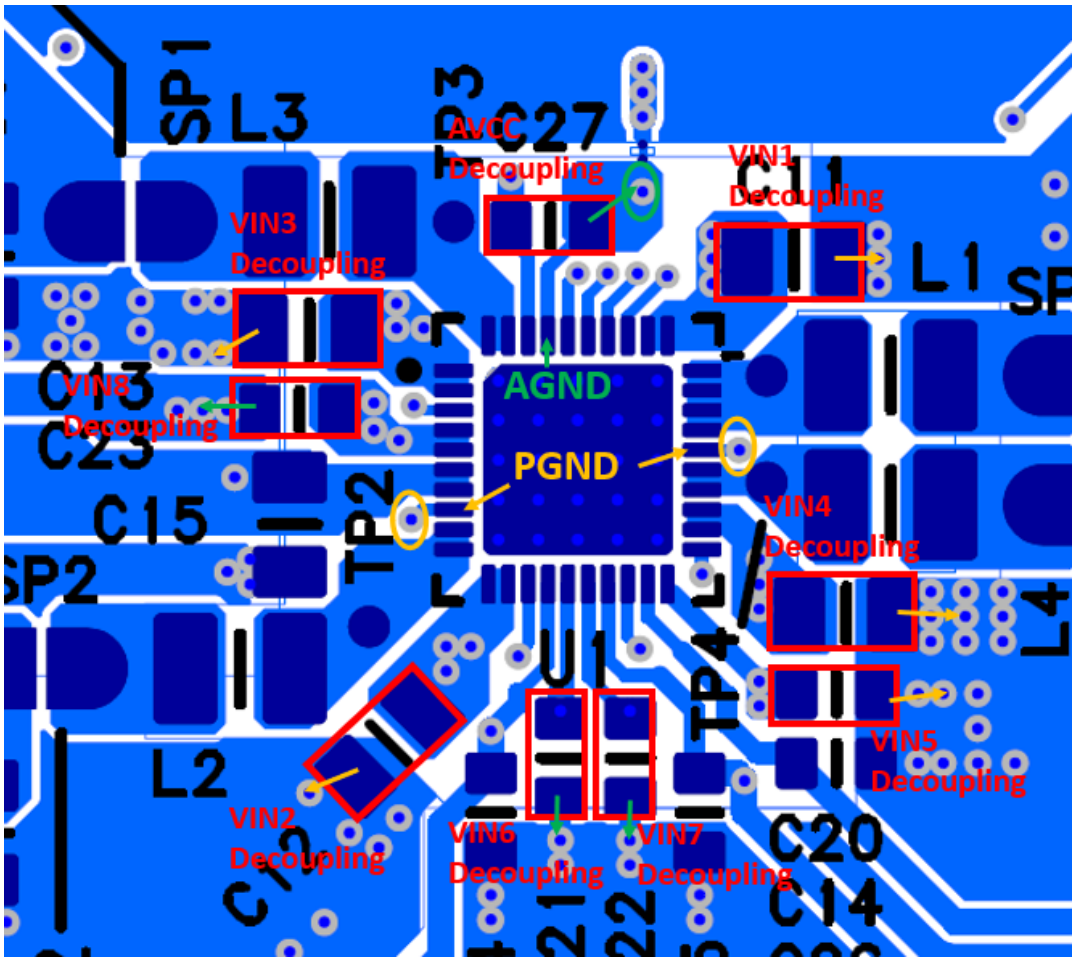


Figure 5: GND Terminals Connection

© 2025 Renesas Electronics

4.2.3 LX Routing

Switch node/LX node traces (traces between LX pins and output inductors) need to be kept as short as possible since this node generates switching noise, which can interfere with buck converters stability. Extremely high current will flow through these traces and so the minimum width of trace used for this LX node must be considered. Also, if used, ensure that there are enough vias to deliver the current.

The LX node patterns on the Renesas Electronics' DA9281 Evaluation Board are shown in Figure 6. The LX nodes are routed out on layer 1.

Layer 1:

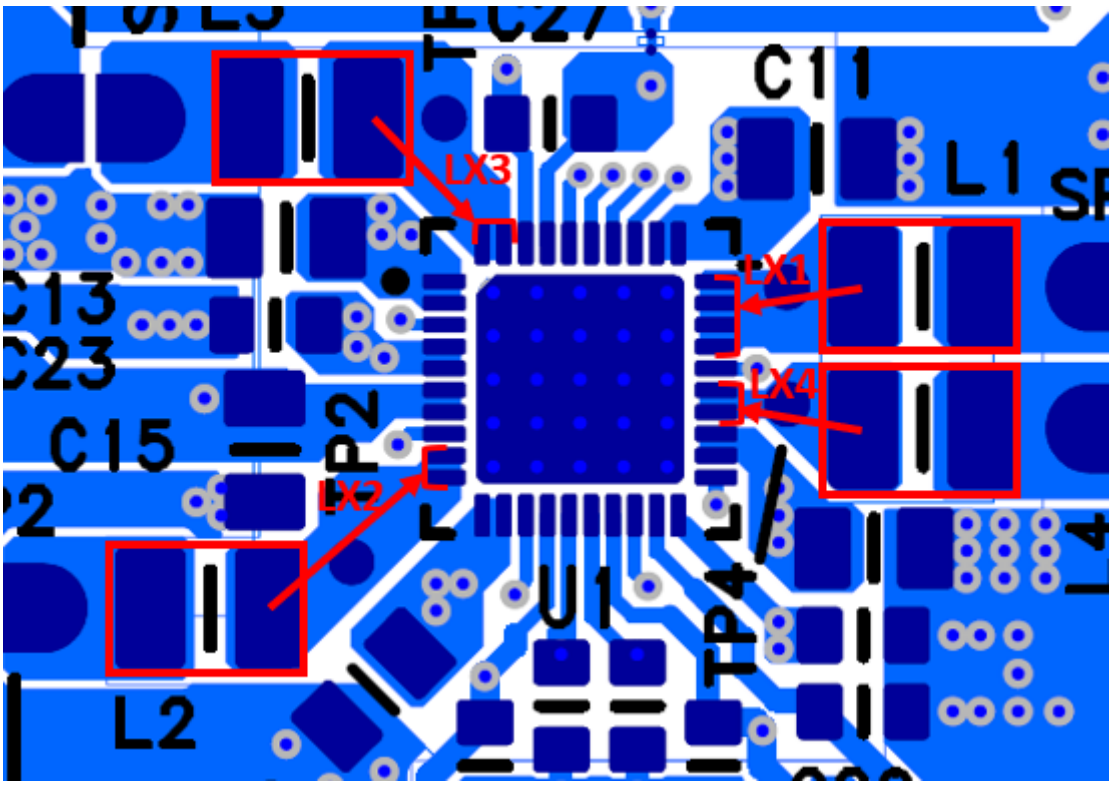


Figure 6: LX Node Pattern on DA9281 Evaluation Board

4.2.4 Buck Regulator, VTT and LDO Output

Output capacitors should be placed locally close to the output inductors to avoid any effects to the stability of the buck converters.

Minimizing the distance (which minimizes the line impedance) from the output inductors to the output capacitors is especially important since it directly affects the efficiency and load transient response performance of the buck converter. Care must be taken with the size of the output traces to accommodate the high output current that DA9281 needs to support.

It is best practice to transfer the output current at the top layer directly without using any vias. This will give the best performance in terms of efficiency and load transient response performance.

The output capacitors for the VTT (CH5) and LDOs (CH6, CH7 and CH8) should be placed near the device. Trace impedances to the VTT and LDO output connection should be minimized to reduce drop-out and effects on load regulation.

4.2.5 Feedback Lines

Feedback lines must be routed far from any noise source (for example, output inductors, LX node, and so on).

© 2025 Renesas Electronics

Also, ensure that the feedback lines are not overlapping with any noisy node traces (for example, the LX node trace) without an insulation plane in between.

NOTE
The feedback lines must be routed directly from the load point to achieve the best voltage accuracy and stability.

Examples of output-voltage feedback-line routing, on the Renesas Electronics' DA9281 Evaluation Board, is shown in Figure 7.

Layer 6 (bottom layer):

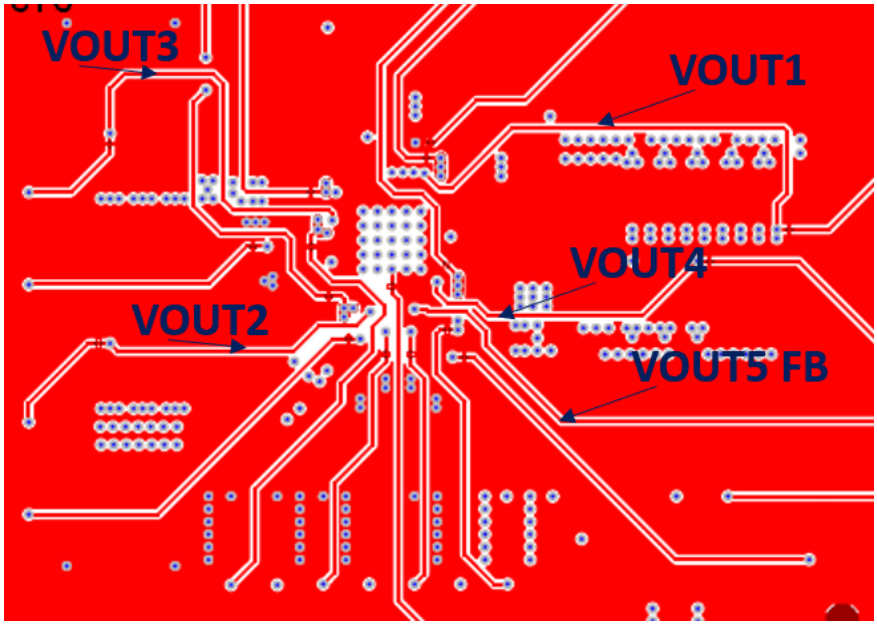


Figure 7: Output Voltage Feedback Line Routing on DA9281 Evaluation Board

4.3 Communication Interface (I^2C)

It is recommended to route the communication interface far from any noise source.

Care must also be taken regarding the noise produced by the interface signal to avoid coupling to the sensitive analog references and feedbacks. The routing layer is not critical, but it is recommended to use the bottom or top layer.

© 2025 Renesas Electronics

Revision History

Revision	Date	Description
1	14-Dec-2023	Initial version.
2	03-Apr-2025	Watermark removed and Figure 3 updated.

© 2025 Renesas Electronics

DA9281 PCB Layout Recommendations

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

© 2025 Renesas Electronics

Important Notice and Disclaimer

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

© 2025 Renesas Electronics Corporation. All rights reserved.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu

Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

https://www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.