DA9281 Unused Pin Configuration

This application note describes the recommended configuration for unused pins in applications that use the DA9281 power management IC.

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Tables

1. Terms and Definitions

CH<x>	Channel <x>
DDR	Double data rate
LDO	Low drop out (regulator)
OCP	Over-current protection
OVP	Over-voltage protection
PGND	Power ground
PMIC	Power management integrated circuit
SW	Switching
UVP	Under-voltage protection
VTT	Termination voltage regulator

2. References

[1] DA9281_Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

DA9281 is an eight-channel power management integrated circuit (PMIC) with four buck regulators, three LDOs and one voltage buffer to support DDR VTT termination
.
Key functions for power applications, such as soft-start, selectable preset output voltage, flexible power-up and power-down sequences are provided on chip and are programmable via the I^2C interface with non-volatile memory defaults.

All eight channels have an output discharge function and protections features such as over-current protection (OCP), over voltage protection (OVP), and under voltage protection (UVP).

4. DA9281 Functional Blocks

The following tables describe the recommended configurations for unused pins. **"**Mandatory**"** means that the pin is used in all applications.

Table 1: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AIO	Analog input/output
DIO	Digital input/output	PWR	Power
DIOD	Digital input/output open drain	GND	Ground

Table 2: Pin Description

Pin #	Pin Name	Type (Table 1)	Description	If Unused
1,2	VIN3	PWR	Input voltage for CH3 buck converter	Connect to GND (cap not required)
3	VOUT3	AI	Output voltage feedback of CH3 buck converter	Connect to GND
4,5	VIN8	PWR	Input voltage for CH8 LDO	Connect to GND (cap not required)
6,7	VOUT8	AO	Output voltage of CH8 LDO	Leave floating (cap not required)
8	PGND	GND	Power ground	Mandatory

Pin #	Pin Name	Type (Table 1)	Description	If Unused
9,10	LX2	AO	SW node of CH2 buck converter	Leave floating (L and Cout not required)
11,12	VIN2	PWR	Input voltage for CH2 buck converter	Connect to GND (cap not required)
13	VOUT2	AI	Output voltage feedback of CH2 buck converter	Connect to GND
14	VOUT6	AO	Output voltage of CH6 LDO	Leave floating (cap not required)
15	VIN6	PWR	Input voltage for CH6 LDO	Connect to GND (cap not required)
16	VIN7	PWR	Input voltage for CH7 LDO	Connect to GND (cap not required)
17	VOUT7	AO	Output voltage of CH7 LDO	Leave floating (cap not required)
18	VOUT5_FB	AI	Output voltage feedback of CH5 regulator	Connect to GND
19	VOUT5	AO	Output voltage of CH5 regulator	Leave floating (cap not required)
20	VIN5	PWR	Input voltage for CH5 regulator	Connect to GND (cap not required)
21	VOUT4	AI	Output voltage feedback of CH4 buck converter	Connect to GND
22,23	VIN4	PWR	Input voltage for CH4 buck converter	Connect to GND (cap not required)
24,25	LX4	AO	SW node of CH4 buck converter	Leave floating (L and Cout not required)
26	PGND	GND	Power ground	Mandatory
27-30	LX1	AO	SW node of CH1 buck converter	Leave floating (L and Cout not required)
31,32	VIN1	PWR	Input voltage for CH1 buck converter	Connect to GND (cap not required)
33	VOUT1	AI	Output voltage feedback of CH1 buck converter	Connect to GND
34	EN	DI	Enable pin	Mandatory
35	SCL	DI	Two-wire I^2C clock	Mandatory - though can be connected to GND if I^2C control/monitoring is not required
36	SDA	DIO	Two-wire I^2C data input/output	Mandatory - though can be connected to GND if I^2C control/monitoring is not required
37	AGND	GND	Quiet analog ground	Mandatory
38	AVCC	PWR	Quiet analog supply	Mandatory
39,40	LX3	AO	SW node of CH3 buck converter	Leave floating (L and Cout not required)
Paddle	PGND	GND	Common ground for all channels	Mandatory

5. Conclusion

Adherence to the recommendations of this document helps minimize spurious application issues such as noise and increased current consumption and may avoid device damage due to incorrectly biased pins. For further information please consult your Renesas Electronics local sales representative.

Revision History

Revision	Date	Description
1.0	Nov 26, 2024	First version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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