RZ/A3M Power Requirements

Design of Power Supply Circuits for RZ/A3M using DA9080

This document describes all the register default settings of the DA9080 for supplying power to the RZ/A3M systems.

The DA9080 is a high-performance, low cost 5 channel PMIC designed for 32-bit and 64-bit MCU / MPU applications. The internally compensated regulators provide a highly integrated, small footprint power solution for System-On-Module (SOM) applications.

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1. Terms and Definitions

ADC	Analog to digital converter
CH<x>	Channel <x>, where x = 1 to 4
FCQFN	Flit Chip quad flat-pack no-lead (package)
LDO	Low drop out (regulator)
OTP	One time programmable
PG	Power good

2. References

[1] DA9080_Datasheet, Renesas Electronics.

[2] RZ/A3M Group Datasheet, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Power Requirements

For power-up, 1.1 V and 1.8 V power (i.e., VDD, VDD18, JTAG_PVDD and OTP_VDD18) must be supplied first; then, 3.3 V power (i.e., PVDD) must be supplied.

Note 1 About SD0_PVDD, especially in the case of switching between 1.8 V and 3.3 V at same power rail, 1.8 V power-on/off timing can also follow 3.3 V power rail sequence as shown in the Figure 1.

Turn on the DDR IO power supply at the same time as or after the 1.1 V power supply.

From first power rising start to last power rising end must be within 100 ms.

The power-off sequence is the reverse of the power-on sequence: (PRST# → Low → 3.3 V = OFF → Other = OFF).

PRST# should be changed from Low to High after the 3.3 V power supply is turned on, after 1 µs, and after the input clock from the oscillator stabilizes.

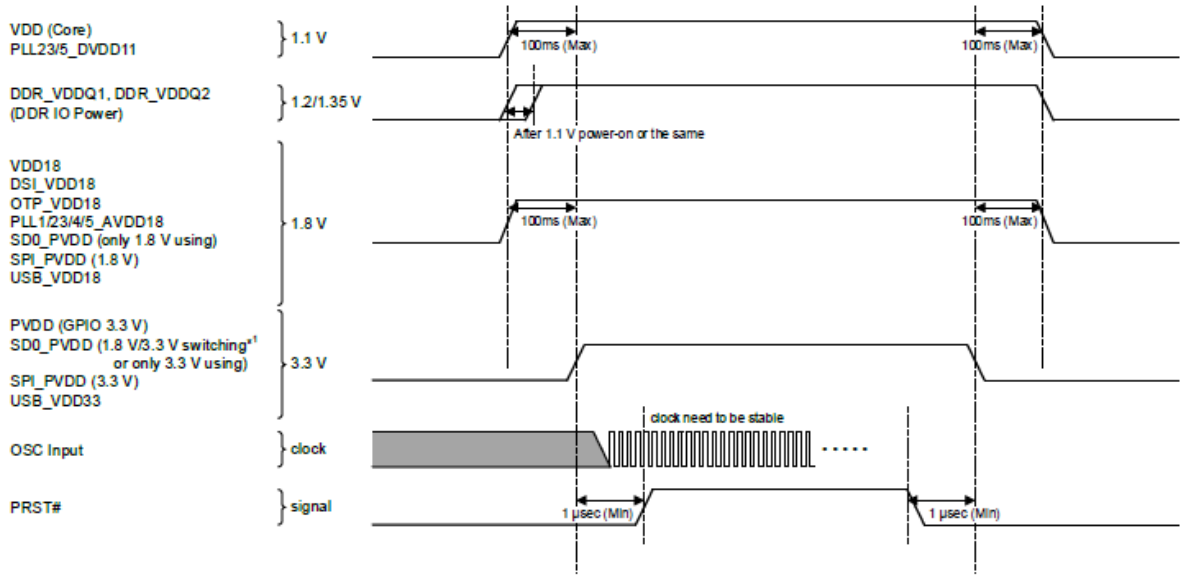

Figure 1. RZ/A3MPower On/Off Sequence

4. Power Supply Tree Diagram

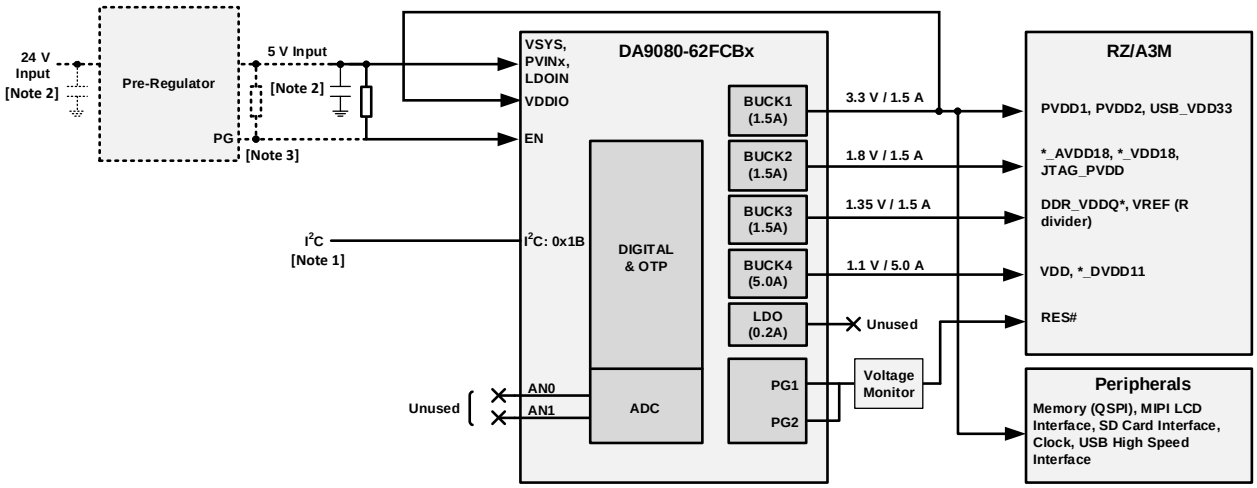

Figure 2. DA9080-62FCBx – RZ/A3M Power Tree

Note 1 The I2C (SCL and SDA) should be connected to the RZ/A3M MPU.

Note 2 A large bulk capacitor (100 µF ~ 1000 µF) should be added to the 5 V input of DA9080 or to the input of the pre-regulator.

Note 3 If a pre-regulator is used to supply DA9080, it is recommended to connect the pre-regulator's PG to the DA9080's EN.

5. Power On/Off Sequences

Channel 1: CH1 (3.3 V), Channel 2: CH2 (1.8 V), Channel 3: CH3 (1.35 V), Channel 4: CH4 (1.1 V)

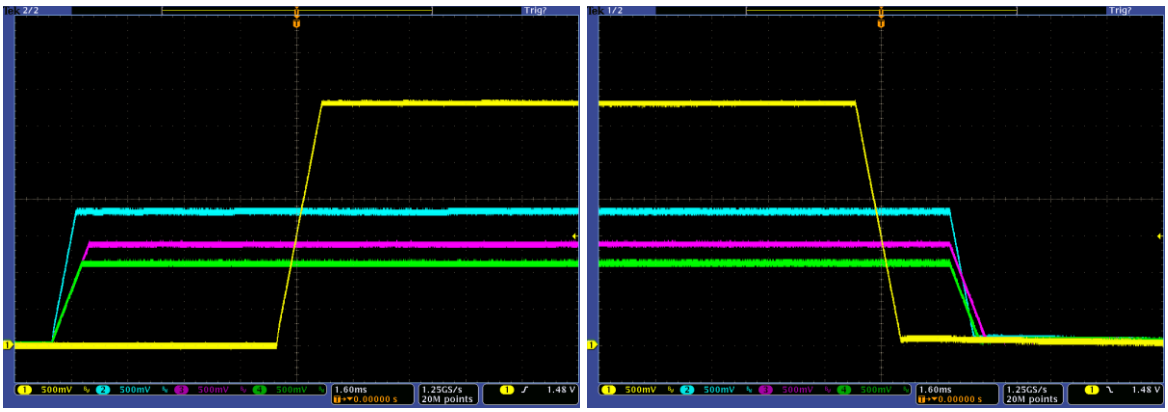

Figure 3. DA9080-62FCBx Power On/Off Sequences

6. Variant Table and Ordering Information

Table 1. Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9080-62FCB2	32 FCQFN	5.0 x 5.0 by 0.5 mm pitch	Tape & Reel	6000
DA9080-62FCBC				1000

7. Detailed Description

Table 2. Register Settings DA9080-62FCBx (I2C slave address is 0x1B (7-bit))

Register Address	Function	Default Value	Description
0x04	PMC_ADC_ENABLE	0x00	ADC disabled
0x05	PMC_CH_EN	0x1F	CH1, CH2, CH3, CH4 and LDO enabled and controlled by the sequencer
0x07	PMC_VOUT_BUCK1	0x3C	VCH1 = 3.3 V
0x08	PMC_VOUT_BUCK2	0x0F	VCH2 = 1.8 V
0x09	PMC_VOUT_BUCK3	0x50	VCH3 = 1.35 V (0x17=0x5F for extended voltage)
0x0A	PMC_VOUT_BUCK4	0x3C	VCH4 = 1.1 V
0x0B	PMC_PHASE_INTERLEAVING	0x88	BUCK1_PHASE = 0º BUCK2_PHASE = 180º BUCK3_PHASE = 0º BUCK4_PHASE = 180º
0x0C	PMC_BUCK_SEQ_GRP	0x03	CH1 = SLOT4, CH2 = SLOT1 CH3 = SLOT1, CH4 = SLOT1
0x0D	PMC_LDO_SEQ_GRP	0x01	LDO = SLOT2
0x0E	PMC_PG1	0x1C	CH2, CH3 and CH4 assigned to PG1
0x0F	PMC_PG2	0x02	CH1 assigned to PG2
0x10	PMC_DISCHARGE	0x1F	CH<x> and LDO discharge enabled
0x62	OTP_CONFIG_ID	0x62	OTP variant number: DA9080-62FCBx

Revision History

Revision	Date	Description
1.0	Feb 26, 2024	First version.
2.0	Oct 02, 2024	Notes added to Figure 2. Figure 2 updated. Table 2 updated.
3.0	Apr 04, 2025	Section 1 updated. Table 1 updated.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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