

RZ/N2L, RZ/T2L, RZ/T2M Power Requirements

Design of Power Supply Circuits for RZ/N2L, RZ/T2L and RZ/T2M using DA9080

This document describes all the register default settings of the DA9080 for supplying power to the RZ/N2L, RZ/T2L and RZ/T2M systems.

The DA9080 is a high-performance, low cost 5 channel PMIC designed for 32-bit and 64-bit MCU / MPU applications. The internally compensated regulators provide a highly integrated, small footprint power solution for System-On-Module (SOM) applications.

To target small design solutions, the RZ/N2L MPU can be supported by DA9083-31UUx which is a compact 36-lead WLCSP package (2.495 mm x 2.495 mm with a 0.4 mm pitch).

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1. Terms and Definitions

ADC	Analog to digital converter
CH<x>	Channel <x>, where x = 1 to 4
FCQFN	Flip chip quad flat-pack no-lead (package)
LDO	Low drop out (regulator)
OTP	One time programmable
PG	Power good

2. References

- [1] DA9080_Datasheet, Renesas Electronics.
- [2] RZ/N2L Group Datasheet, Renesas Electronics.
- [3] RZ/T2L Group Datasheet, Renesas Electronics.
- [4] RZ/T2M Group Datasheet, Renesas Electronics.
- [5] AN-PM-174_DA9083-31UUx Variant Overview - RZN2L MPU_2v0, Renesas Electronics.

Note 1 References are for the latest published version, unless otherwise indicated.

3. Power Requirements

For power-up, 1.1 V and 1.8 V power (i.e., VDD, VCC18, and AVCC) must be supplied first, then 3.3 V power (i.e., VCC33) must be supplied. The power-up sequence must be completed within 100 ms. Reset signal (i.e., RES#) must be held to a low level during the power-up.

For Power-down, 3.3 V power (i.e., VCC33) must go down first and then 1.1 V and 1.8 V power (i.e., VDD, VCC18, and AVCC). The power-down sequence must be completed within 100 ms.

Rise and fall time of each power supply for the power-up and the power-down must be larger than 10 μ s.

Power supply voltages and reset signal must be applied with monotonic increase.

Do not apply a negative voltage to power supply voltages.

A stable clock must be supplied to EXTAL/XTAL or EXTCLKIN pin when reset signal (i.e., RES#) is driven high.

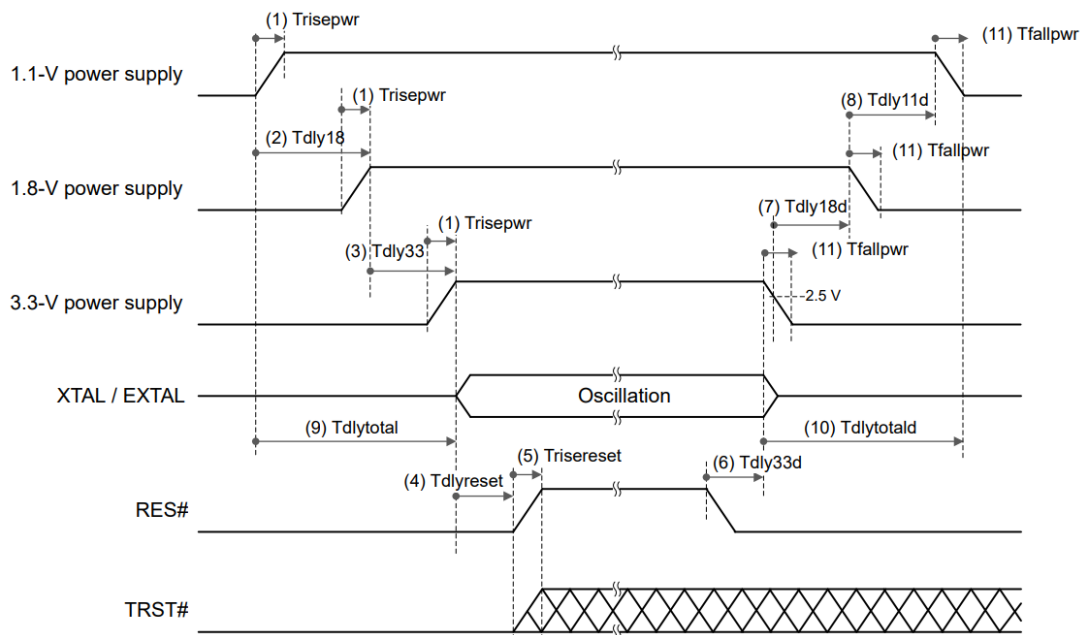


Figure 1. RZ/N2L, RZ/T2L, RZ/T2M Power On/Off Sequence

4. Power Supply Tree Diagram

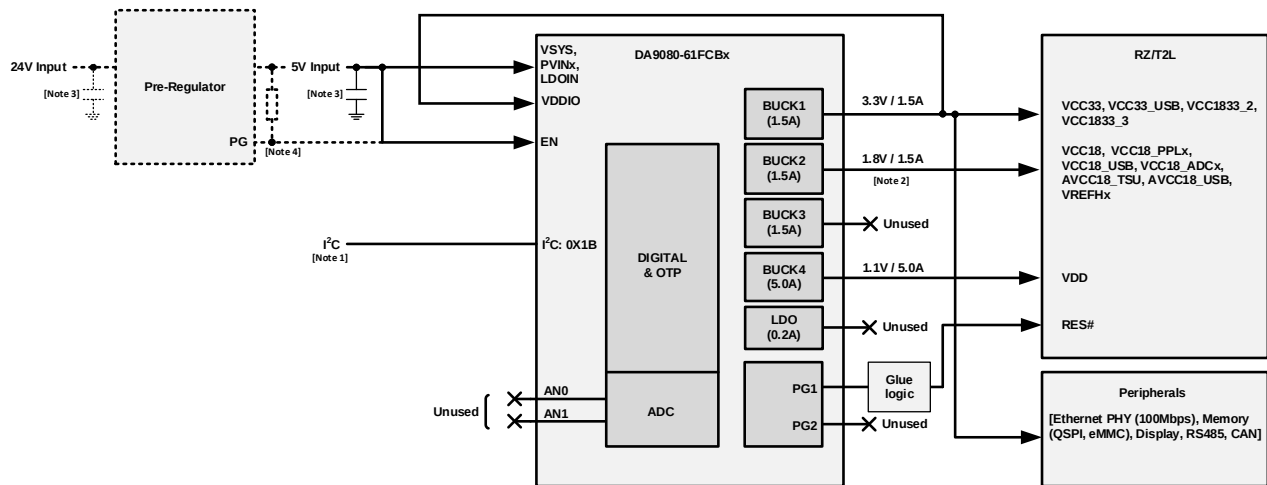


Figure 2. DA9080-61FCBx – RZ/T2L Power Tree (100Mbps PHY)

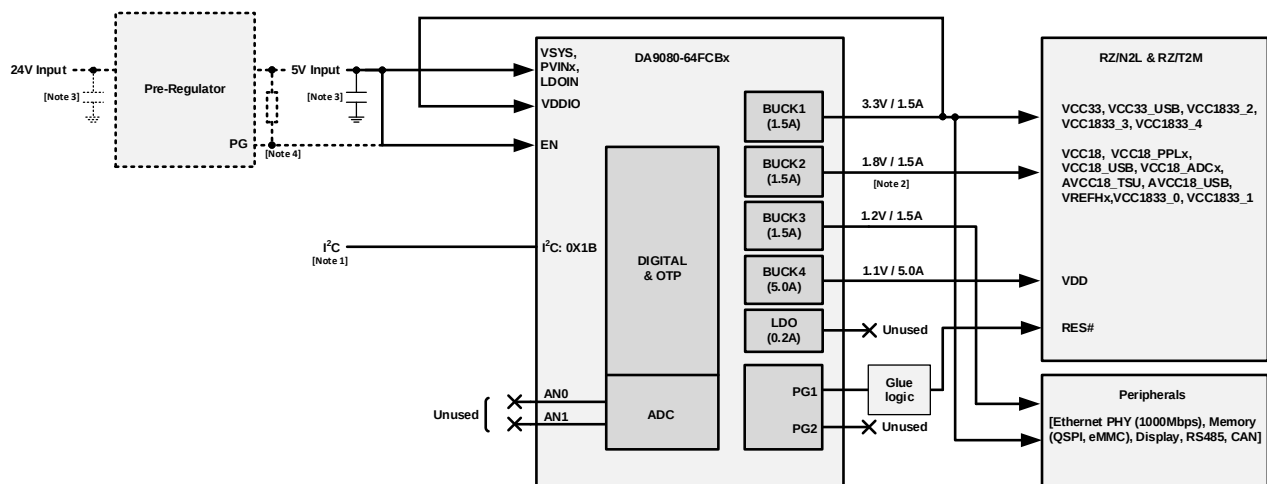


Figure 3. DA9080-64FCBx – RZ/N2L & RZ/T2M Power Tree (1000Mbps PHY)

- Note 1** The I2C (SCL and SDA) should be connected to the RZ/T2L, RZ/N2L or RZ/T2M MPU.
- Note 2** VCC18_ADCx and VREFHx are sensible rails; therefore, it may be required to operate CH2 (1.8 V) in PWM mode.
- Note 3** A large bulk capacitor (100 μ F ~ 1000 μ F) should be added to the 5V input of DA9080 or to the input of the pre-regulator.
- Note 4** If a pre-regulator is used to supply DA9080, it is recommended to connect the pre-regulator's PG to the DA9080's EN.

5. Power On/Off Sequences

Channel1: CH1 (3.3 V), Channel 2: CH2 (1.8 V), Channel 3: CH 4 (1.1 V), Channel 4: PG1 (OD/PU to 3.3 V)

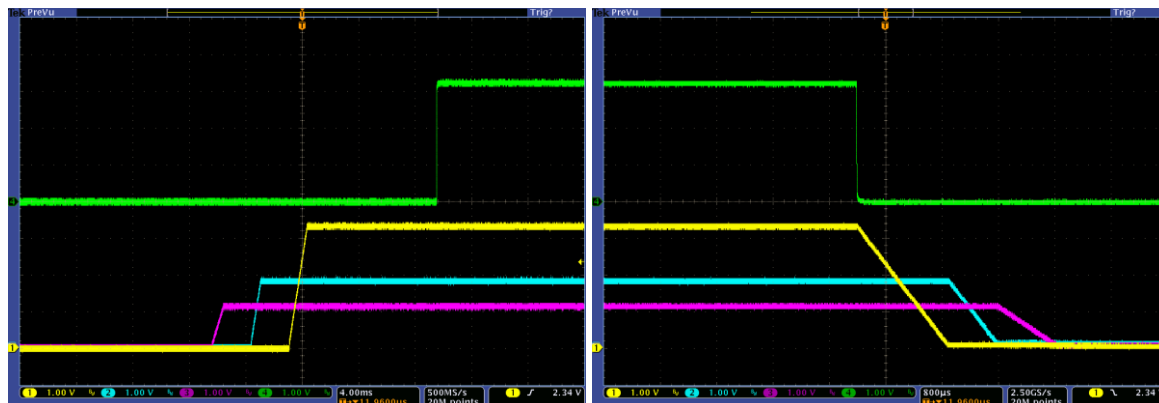


Figure 4. DA9080-61FCBx Power On/Off Sequences

Channel 1: CH 1 (3.3 V), Channel 2: CH 2 (1.8 V), Channel 3: CH 3 (1.2 V), Channel 4: CH 4 (1.1V)

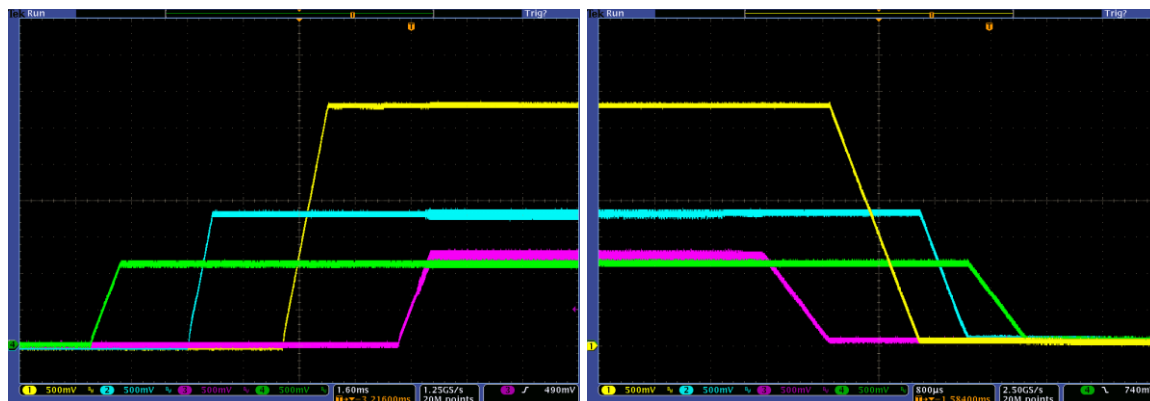


Figure 5. DA9080-64FCBx Power On/Off Sequences

6. Variant Table and Ordering Information

Table 1. Variant Table

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9080-61FCB2	32 FCQFN	5.0 x 5.0 by 0.5 mm pitch	Tape & Reel	4900
DA9080-61FCBC				1000
DA9080-64FCB2				4900
DA9080-64FCBC				1000

7. Detailed Description

Table 2. Register Settings DA9080-61FCBx (I2C slave address is 0x1B (7-bit))

Register Address	Function	Default Value	Description
0x04	PMC_ADC_ENABLE	0x01	ADC enabled
0x05	PMC_CH_EN	0x16	CH1, CH2 and CH4 enabled CH3 and LDO disabled
0x07	PMC_VOUT_BUCK1	0x3C	VCH1 = 3.30 V
0x08	PMC_VOUT_BUCK2	0x0F	VCH2 = 1.80 V
0x09	PMC_VOUT_BUCK3	0x00	VCH3 = 0.90 V
0x0A	PMC_VOUT_BUCK4	0x3C	VCH4 = 1.10 V
0x0B	PMC_PHASE_INTERLEAVING	0x88	BUCK1_PHASE = 0° BUCK2_PHASE = 180° BUCK3_PHASE = 0° BUCK4_PHASE = 180°
0x0C	PMC_BUCK_SEQ_GRP	0x06	CH1 = SLOT3, CH2 = SLOT2 CH3 = NA, CH4 = SLOT1
0x0D	PMC_LDO_SEQ_GRP	0x00	LDO = NA
0x0E	PMC_PG1	0x16	CH1, CH2 and CH4 assigned to PG1
0x0F	PMC_PG2	0x00	PG2 unused
0x10	PMC_DISCHARGE	0x1F	CH<x> and LDO discharge enabled
0x62	OTP_CONFIG_ID	0x61	OTP variant number: DA9080-61FCBx

Table 3. Register Settings DA9080-64FCBx (I2C slave address is 0x1B (7-bit))

Register Address	Function	Default Value	Description
0x04	PMC_ADC_ENABLE	0x01	ADC enabled
0x05	PMC_CH_EN	0x1E	CH1, CH2, CH3 and CH4 enabled LDO disabled
0x07	PMC_VOUT_BUCK1	0x3C	VCH1 = 3.30 V
0x08	PMC_VOUT_BUCK2	0x0F	VCH2 = 1.80 V
0x09	PMC_VOUT_BUCK3	0x3C	VCH3 = 1.20 V
0x0A	PMC_VOUT_BUCK4	0x3C	VCH4 = 1.10 V
0x0B	PMC_PHASE_INTERLEAVING	0x88	BUCK1_PHASE = 0° BUCK2_PHASE = 180° BUCK3_PHASE = 0° BUCK4_PHASE = 180°
0x0C	PMC_BUCK_SEQ_GRP	0x36	CH1 = SLOT3, CH2 = SLOT2 CH3 = SLOT4, CH4 = SLOT1
0x0D	PMC_LDO_SEQ_GRP	0x00	LDO = NA
0x0E	PMC_PG1	0x1E	CH1, CH2, CH3 and CH4 assigned to PG1
0x0F	PMC_PG2	0x00	PG2 unused
0x10	PMC_DISCHARGE	0x1F	CH<x> and LDO discharge enabled
0x62	OTP_CONFIG_ID	0x64	OTP variant number: DA9080-64FCBx

Revision History

Revision	Date	Description
1.0	May 08, 2024	First version.
2.0	Sep 03, 2024	Notes added to Figure 2 & Figure 3 . Figure 2 & Figure 3 updated. Table 2 & Table 3 updated
3.0	Apr 04, 2025	Section 1 updated. Table 1 updated.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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