M16C/62P Group, M16C/65 Group

Differences between M16C/62P and M16C/65

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Abstract

The following document describes differences between M16C/62P 100-pin version and M16C/65 100-pin version. Refer to each device's hardware manual for details.

Products

MCUs: M16C/62P Group, M16C/65 Group

With its enhanced peripheral functions, the M16C/65 Group MCU has pin assignments and peripheral functions that are compatible with the M16C/62P Group, making it simple to replace the M16C/62P Group with the M16C/65 Group.

Contents

1. Differences

1.1 Differences in Functions

Table 1.1 and Table 1.3 list Differences in Functions.

Table 1.1 Differences between Functions (1/3) (1)

Item		M16C/62P	M16C/65
Minimum Instruction Execution Time		41.7 ns (f(BCLK) = 24 MHz, VCC1 = 3.0 to 5.5 V) 100 ns (f(BCLK) = 10 MHz, VCC1 = 2.7 to 5.5 V)	31.25 ns (f(BLCK) = 32 MHz, VCC1 = 2.7 to 5.5 V)
Clock Generator		PLL, XIN, XCIN, on-chip oscillator (approx.1 MHz)	PLL, XIN, XCIN, 125 kHz on-chip oscillator, 40 MHz on-chip oscillator
Power Control	Slow read mode	No	Yes
	Low current consumption read mode	No	Yes
CPU Clock After Reset		Main clock divided by 8	125 kHz on-chip oscillator clock divided by 8
$\overline{\text{NMI}}$ Pin		$\overline{\text{NMI}}$ interrupt input port	PM24 bit = 0 (when $\overline{\text{NMI}}$ is disabled): I/O port (N-channel open drain output) PM24 bit = 1 (when $\overline{\text{NMI}}$ is enabled): $\overline{\text{NMI}}$ interrupt input port
External Bus	Expanded area	04000h to 07FFFh (when PM13 = 0) 08000h to 0FFFFh (when PM10 = 0) 10000h to 26FFFh 28000h to 7FFFFh 80000h to CFFFFh (when PM13 = 0) D0000h to FFFFFh (in microprocessor mode)	04000h to 07FFFh (when PM13 = 0) 08000h to 0CFFFh (when PM10 = 0) 0D800h to 0DFFFh 0E000h to 0FFFFh (when PM10 = 0) 10000h to 13FFFh (when PRG2C0 = 1) 14000h to 26FFFh 28000h to 7FFFFh 80000h to CFFFFh (when PM13 = 0) D0000h to FFFFFh (in microprocessor mode)
	Bus wait	0 to 3 wait(s) selectable	0 to 8 wait(s) selectable
	Recovery cycle	No	0 to 3 cycle(s) selectable
	$\overline{\text{HOLD}}$ input	Enabled	Disabled
Interrupt		External interrupts: 8	External interrupts: 13
Watchdog Timer	Reset start function	No	Selectable from start and stop
	Count source	CPU clock, on-chip oscillator (approx. 1 MHz)	CPU clock, on-chip oscillator (125 kHz)
DMA	DMAC	2 channels Trigger sources: 25	4 channels Trigger sources: 43

PM24: Bit in the PM2 register
PM13,PM10: Bits in the PM1 register
PRG2C0: Bit in the PRG2C register

Note:
1. Refer to hardware manual for electrical characteristics and more details.

Table 1.2 Differences between Functions (2/3) (1)

Item		M16C/62P	M16C/65
Timer	Timer A, timer B count source	Selectable from f1, f2, f8, f32, and fC32	Selectable from f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-S, fOCO-F, and fC32
	Real-time clock	No	Count: second, minute, hour, day of week
	PWM function	No	8 bits x 2
	Remote control signal receive function	No	2 circuits
Serial Interface	UART	Clock synchronous/asynchronous x 3 channels	Clock synchronous/asynchronous x 6 channels
	UART0 to UART2, UART5 to UART7 clock prior to division select function	f1 only	Selectable from f1 and fOCO-F
	CEC	No	Yes
	Multi-master I^2C-bus interface	No	1 channel
A/D Converter	Resolution	8-bit/10-bit (selectable)	10-bit only
	Operation clock ϕAD	Selectable from fAD, fAD divided by 2, fAD divided by 3, fAD divided by 4, fAD divided by 6, and fAD divided by 12	Selectable from f1, f1 divided by 2, f1 divided by 3, f1 divided by 4, f1 divided by 6, f1 divided by 12, fOCO40M divided by 2, fOCO40M divided by 3, fOCO40M divided by 4, fOCO40M divided by 6, and fOCO40M divided by 12
	Sample and hold	Yes/No (selectable)	Yes
CRC Calculator	Generator polynomial	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)	Selectable from CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) and CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
	MSB/LSB select function	No	Yes
	CRC snoop	No	Yes

Note:
1. Refer to hardware manual for electrical characteristics and more details.

Table 1.3 Differences between Functions (3/3) (1)

Item		M16C/62P	M16C/65
Flash Memory	Address FFFFFh function setting	ROM code protect select function	Selectable Options • Watchdog timer autostart function (after reset) • Count source protection mode select function (after reset) • ROM code protect function • Vdet0 select function • Voltage monitor 0 reset function (after hardware reset)
	Memory map	User ROM Program ROM 080000h to 0FFFFFh Data flash Block A 00F000h to 00FFFFh	User ROM • Program ROM 1 080000h to 0FFFFFh • Program ROM 2 010000h to 013FFFh Data flash • Block A 00E000h to 00EFFFh • Block B 00F000h to 00FFFFh
	User ROM (512-Kbyte)	64 Kbytes x 7 32 Kbytes x 1 8 Kbytes x 3 4 Kbytes x 2	64 Kbytes x 8 16 Kbytes x 1 (program ROM 2)
	Data flash	4 Kbytes x 1 (block A)	4 Kbytes x 2 (block A, block B)
	Program method	In units of 1 word (16-bit)	In units of 2 words (32-bit)
	Erase method	Erase all unlocked blocks, block erase	Block erase
	User boot mode	No	Yes

Note:
1. Refer to hardware manual for electrical characteristics and more details.

1.2 Pin Characteristics

Table 1.4 lists Differences between Pin Characteristics.

Table 1.4 Differences between Pin Characteristics

M16C/62P	M16C/65	Changes from M16C/62P
P9_4 / TB4IN / DA1	P9_4 / TB4IN / DA1 / PWM1	Added: PWM1
P9_3 / TB3IN / DA0	P9_3 / TB3IN / DA0 / PWM0	Added: PWM0
P9_2 / TB2IN / SOUT3	P9_2 / TB2IN / SOUT3 / PMC0	Added: PMC0
P9_1 / TB1IN / SIN3	P9_1 / TB1IN / SIN3 / PMC1	Added: PMC1
P8_5 / $\overline{\text{NMI}}$	P8_5 / $\overline{\text{NMI}}$ / $\overline{\text{SD}}$ / CEC	Added: $\overline{\text{SD}}$/CEC
P8_1 / TA4IN / $\overline{\text{U}}$	P8_1 / TA4IN / $\overline{\text{U}}$ / $\overline{\text{CTS5}}$ / $\overline{\text{RTS5}}$	Added: $\overline{\text{CTS5}}$ / $\overline{\text{RTS5}}$
P8_0 / TA4OUT / U	P8_0 / TA4OUT / U / RXD5 / SCL5	Added: RXD5/SCL5
P7_7 / TA3IN	P7_7 / TA3IN / CLK5	Added: CLK5
P7_6 / TA3OUT	P7_6 / TA3OUT / TXD5 / SDA5	Added: TXD5/SDA5
P7_1 / TA0IN / TB5IN / RXD2 / SCL2	P7_1 / TA0IN / TB5IN / RXD2 / SCL2 / SCLMM	Added: SCLMM
P7_0 / TA0OUT / TXD2 / SDA2	P7_0 / TA0OUT / TXD2 / SDA2 / SDAMM	Added: SDAMM
P6_0 / $\overline{\text{CTS0}}$ / $\overline{\text{RTS0}}$	P6_0 / $\overline{\text{CTS0}}$ / $\overline{\text{RTS0}}$ / RTCOUT	Added: RTCOUT
P4_7 / $\overline{\text{CS3}}$	P4_7 / $\overline{\text{CS3}}$ / PWM1 / TXD7 / SDA7	Added: PWM1/TXD7/SDA7
P4_6 / $\overline{\text{CS2}}$	P4_6 / $\overline{\text{CS2}}$ / PWM0 / RXD7 / SCL7	Added: PWM0/RXD7/SCL7
P4_5 / $\overline{\text{CS1}}$	P4_5 / $\overline{\text{CS1}}$ / CLK7	Added: CLK7
P4_4 / $\overline{\text{CS0}}$	P4_4 / $\overline{\text{CS0}}$ / $\overline{\text{CTS7}}$ / $\overline{\text{RTS7}}$	Added: $\overline{\text{CTS7}}$ / $\overline{\text{RTS7}}$
P2_5 / AN2_5 / A5 (/ D5 / D4)	P2_5 / $\overline{\text{INT7}}$ / AN2_5 / A5, [A5 / D5], [A5 / D4]	Added: $\overline{\text{INT7}}$
P2_4 / AN2_4 / A4 (/ D4 / D3)	P2_4 / $\overline{\text{INT6}}$ / AN2_4 / A4, [A4 / D4], [A4 / D3]	Added: $\overline{\text{INT6}}$
P1_7 / $\overline{\text{INT5}}$ / D15	P1_7 / $\overline{\text{INT5}}$ / D15 / IDU	Added: IDU
P1_6 / $\overline{\text{INT4}}$ / D14	P1_6 / $\overline{\text{INT4}}$ / D14 / IDW	Added: IDW
P1_5 / $\overline{\text{INT3}}$ / D13	P1_5 / $\overline{\text{INT3}}$ / D13 / IDV	Added: IDV
P1_3 / D11	P1_3 / D11 / TXD6 / SDA6	Added: TXD6 / SDA6
P1_2 / D10	P1_2 / D10 / RXD6 / SCL6	Added: RXD6 / SCL6
P1_1 / D9	P1_1 / D9 / CLK6	Added: CLK6
P1_0 / D8	P1_0 / D8 / $\overline{\text{CTS6}}$ / $\overline{\text{RTS6}}$	Added: $\overline{\text{CTS6}}$ / $\overline{\text{RTS6}}$

2. Detailed Comparison

2.1 Differences between Protections

Table 2.1 lists Differences in Registers Associated with Protect Functions.

Table 2.1 Differences in Registers Associated with Protect Functions

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
PRCR	000Ah	000Ah	0	Protect bit 0 Enable write access to registers CM0, CM1, CM2, PLC0, and PCLKR	Protect bit 0 Enable write access to registers CM0, CM1, CM2, PLC0, PCLKR, and FRA0
			3	Protect bit 3 Enable write access to registers VCR2, and D4INT	Protect bit 3 Enable write access to registers VCR2, VWCE, VD1LS, VW0C, VW1C, and VW2C
			6	—	Protect bit 6 Enable write access to the PRG2C register

2.2 Differences between Resets

Table 2.2 lists Differences between Resets and Table 2.3 lists Difference between Registers Associated with Resets.

Table 2.2 Differences between Resets

Item	M16C/62P	M16C/65
Types of resets	Hardware reset Brown-out detection reset Oscillation stop detection reset Watchdog timer reset Software reset	Hardware reset Voltage monitor 0 reset Voltage monitor 1 reset Voltage monitor 2 reset Power-on reset Oscillation stop detection reset Watchdog timer reset Software reset
Cold start, warm start discrimination method	WDC5 bit in the WDC register	CWR bit in the RSTFR register
Reset Source Determine Register	No	Yes

Table 2.3 Difference between Registers Associated with Resets

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
RSTFR	—	0018h	—	—	M16C/65 only

2.3 Differences between Voltage Detectors

Table 2.4 lists Differences between Voltage Detectors and Table 2.5 lists Differences between Registers Associated with Voltage Detectors.

Table 2.4 Differences between Voltage Detectors

Item	M16C/62P	M16C/65
Voltage detection interrupt monitor level	Vdet4	• Vdet1 (voltage detection circuit 1) • Vdet2 (voltage detection circuit 2)
Voltage detection reset monitor level	Vdet3	• Vdet0 (voltage detection circuit 0) • Vdet1 (voltage detection circuit 1) • Vdet2 (voltage detection circuit 2)

Refer to the hardware manual and electric characteristics on detection voltage.

Table 2.5 Differences between Registers Associated with Voltage Detectors

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
VCR2	001Ah	001Ah	5	Reserved bit	Voltage detector 0 enable bit 0: Voltage detector 0 disabled 1: Voltage detector 0 enabled
			6	Reset Level Monitor Bit 0 : Disable reset level detection circuit 1 : Enable reset level detection circuit	Voltage detector 1 enable bit 0: Voltage detector 1 disabled 1: Voltage detector 1 enabled
			7	Low Voltage Monitor Bit 0 : Disable low voltage detection circuit 1 : Enable low voltage detection circuit	Voltage detector 2 enable bit 0: Voltage detector 2 disabled 1: Voltage detector 2 enabled
VWCE	—	0026h	—	—	M16C/65 only
VD1LS	—	0028h	—	—	M16C/65 only
VW0C	—	002Ah	—	—	M16C/65 only
VW1C	—	002Bh	—	—	M16C/65 only
VW2C	—	002Ch	—	—	M16C/65 only
D4INT	001Fh	—	—	M16C/62P only	—

2.4 Differences between Clock Generators

Table 2.6 lists Differences between Clock Generators, and Table 2.7 to Table 2.8 list Differences between Registers Associated with Clock Generators.

Table 2.6 Differences between Clock Generators

Item	M16C/62P	M16C/65
Clock output function	Selectable from fC, f8, and f32	Selectable from fC, f8, f32, and f1
CPU clock after reset	Main clock divided by 8 (default setting of the CM21 bit: 0)	125 kHz on-chip oscillator clock divided by 8 (default setting of CM21 bit: 1)
Peripheral clock (fC)	Supply constantly	Provided or not provided can be selected by the PM25 bit
40 MHz on-chip oscillator	No	Yes
125 kHz on-chip oscillator	No	Yes
On-chip oscillator frequency	Approx. 1 MHz	Approx. 125 kHz, approx. 40 MHz
Calculation formula for PLL clock frequency	f(XIN) x n	f(XIN)/m x n

n: Multiply ratio set by bits PLC02 to PLC00 in the PLC0 register
m: Division ratio set by bits PLC05 to PLC04 in the PLC0 register

Table 2.7 Differences between Registers Associated with Clock Generators (1/2)

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
CM1	0007h	0007h	3	Reserved bits	XIN-XOUT feedback resistor select bit 0 : Internal feedback resistor connected 1 : Internal feedback resistor not connected
			4		125 kHz on-chip oscillator oscillation stop bit 0: 125 kHz on-chip oscillator on 1: 125 kHz on-chip oscillator off
PCLKR	025Eh	0012h	—	Different address	
			5	Reserved bit	Clock output function extension bit (valid in single-chip mode) 0: Selected by bits CM01 to CM00 in the CM0 register 1: Output f1
PLC0	001Ch	001Ch	4	Reserved bit Set to 1.	Reference frequency counter set bit 00: No division 01: Divide-by-2 10: Divide-by-4 11: Do not set
			5	Reserved bit	

Table 2.8 Differences between Registers Associated with Clock Generators (2/2)

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
PM2	001Eh	001Eh	0	Specifying wait when accessing SFR at PLL operation 0 : 2 waits 1 : 1 wait	Reserved bit Set to 1.
			2	WDT count source protect bit 0: CPU clock is used for the watchdog timer count source 1: On-chip oscillator clock is used for the watchdog timer count source	No register bit
			4	Reserved bit	$\overline{\text{NMI}}$ interrupt enable bit 0: $\overline{\text{NMI}}$ interrupt disabled 1: $\overline{\text{NMI}}$ interrupt enabled
			5	No register bit	Peripheral clock fC provide bit 0: Not provided 1: Provided
FRA0	—	0022h	—	—	M16C/65 only

2.5 Differences between Power Controls

Table 2.9 lists Differences between Power Controls and Table 2.10 lists Difference between Registers Associated with Power Controls.

Table 2.9 Differences between Power Controls

Item	M16C/62P	M16C/65
Slow read mode	No	Yes
Low current consumption read mode	No	Yes

Table 2.10 Difference between Registers Associated with Power Controls

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
FMR2	—	0222h	—	—	M16C/65 only

2.6 Differences between Processor Modes

Table 2.11 lists Differences between Registers Associated with Processor Modes.

Table 2.11 Differences between Registers Associated with Processor Modes

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
PM1	0005h	0005h	0	$\overline{\text{CS2}}$ area switch bit 0: 08000h to 26FFFh (block A disabled) 1: 10000h to 26FFFh (block A enabled)	$\overline{\text{CS2}}$ area switch bit 0: $\overline{\text{CS2}}$ area (0E000h to 0FFFFh) 1: Data flash (0E000h to 0FFFFh)
PRG2C	—	0010h	—	—	M16C/65 only

2.7 Differences in Bus

Table 2.12 lists Differences between Buses and Table 2.13 lists Differences between Registers Associated with Buses.

Table 2.12 Differences between Buses

Item	M16C/62P	M16C/65
External area wait	Selectable from 0 to 3 wait(s) CSiW bit in the CSR register, Selected by bits CSEi0W and CSEi1W in the CSE register (i = 0 to 3)	Selectable from 0 to 8 wait(s) Selected by CSiW bit in the CSR register, bits CSEi0W and CSEi1W in the CSE register, and bits EWCi0 to EWCi1 in the EWC register
Recovery cycle	No	Selectable from 0 to 3 cycle(s) Selectable by bits EWR0 to EWR1 in the EWR register

Table 2.13 Differences between Registers Associated with Buses

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
CSE	001Bh	001Bh	1 - 0	$\overline{CS0}$ wait expansion bit b1 b0 1 1: Do not set	$\overline{CS0}$ wait expansion bit b1 b0 1 1: Selected by bits EWC01 and EWC00 in the EWC register
			3 -2	$\overline{CS1}$ wait expansion bit b3 b2 1 1: Do not set	$\overline{CS1}$ wait expansion bit b3 b2 1 1: Selected by bits EWC11 and EWC10 in the EWC register
			5 - 4	$\overline{CS2}$ wait expansion bit b5 b4 1 1: Do not set	$\overline{CS2}$ wait expansion bit b5 b4 1 1: Selected by bits EWC21 and EWC20 in the EWC register
			7 - 6	$\overline{CS3}$ wait expansion bit b7 b6 1 1: Do not set	$\overline{CS3}$ wait expansion bit b7 b6 1 1: Selected by bits EWC31 and EWC30 in the EWC register
EWC	—	0011h	—	—	M16C/65 only
EWR	—	0009h	—	—	M16C/65 only

2.8 Differences between Programmable I/O Ports

Table 2.14 lists Difference between Programmable I/O Ports and Table 2.15 lists Differences between Registers Associated with Programmable I/O Ports.

Table 2.14 Difference between Programmable I/O Ports

Item	M16C/62P	M16C/65
$\overline{\text{NMI}}$ / $\overline{\text{SD}}$ digital filter	No	Use or non-use of digital filter can be selectable by the NMIDF register

Table 2.15 Differences between Registers Associated with Programmable I/O Ports

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
PD8	03F2h	03F2h	5	No register bit	Port P8_5 direction bit 0 : Input mode (Functions as an input port) 1 : Output mode (Functions as an output port)
PUR0	03FCh	0360h	—	Different address	
PUR1	03FDh	0361h	—	Different address	
PUR2	03FEh	0362h	—	Different address	
PCR	03FFh	0366h	—	Different address	
			3	No register bit	Reserved bit
			4	No register bit	CEC output enable bit
			5	No register bit	$\overline{\text{INT6}}$ input enable bit
			6	No register bit	$\overline{\text{INT7}}$ input enable bit
			7	No register bit	Key input enable bit
NMIDF	—	0369h	—	—	M16C/65 only

2.9 Differences between Interrupts

Table 2.16 lists Difference between Interrupts and Table 2.17 to Table 2.18 list Differences in Interrupt Vectors, and Table 2.19 lists Differences between Registers Associated with Interrupts.

Table 2.16 Difference between Interrupts

Item	M16C/62P	M16C/65
$\overline{\text{NMI}}$ enable function	Enable only	Enable or disable is selectable by the PM24 bit in the PM2 register

Table 2.17 Differences between Interrupt Vectors - (1/2)

Software Interrupt Number	Vector Address	M16C/62P	M16C/65
0	+0 to +3 (0000h to 0003h)	BRK instruction	BRK instruction
1	+4 to +7 (0004h to 0007h)	— (Reserved)	INT instruction interrupt
2	+8 to +11 (0008h to 000Bh)		$\overline{\text{INT7}}$
3	+12 to +15 (000Ch to 000Fh)		$\overline{\text{INT6}}$
4	+16 to +19 (0010h to 0013h)	$\overline{\text{INT3}}$	$\overline{\text{INT3}}$
5	+20 to +23 (0014h to 0017h)	Timer B5	Timer B5
6	+24 to +27 (0018h to 001Bh)	Timer B4, UART1 start/stop condition detection, bus collision detection	Timer B4, UART1 start/stop condition detection, bus collision detection
7	+28 to +31 (001Ch to 001Fh)	Timer B3, UART0 start/stop condition detection, bus collision detection	Timer B3, UART0 start/stop condition detection, bus collision detection
8	+32 to +35 (0020h to 0023h)	SI/O4, $\overline{\text{INT5}}$	SI/O4, $\overline{\text{INT5}}$
9	+36 to +39 (0024h to 0027h)	SI/O3, $\overline{\text{INT4}}$	SI/O3, $\overline{\text{INT4}}$
10	+40 to +43 (0028h to 002Bh)	UART2 start/stop condition detection, bus collision detection	UART2 start/stop condition detection, bus collision detection
11	+44 to +47 (002Ch to 002Fh)	DMA0	DMA0
12	+48 to +51 (0030h to 0033h)	DMA1	DMA1
13	+52 to +55 (0034h to 0037h)	Key input interrupt	Key input interrupt
14	+56 to +59 (0038h to 003Bh)	A/D converter	A/D converter
15	+60 to +63 (003Ch to 003Fh)	UART2 transmit, NACK2	UART2 transmit, NACK2
16	+64 to +67 (0040h to 0043h)	UART2 receive, ACK2	UART2 receive, ACK2
17	+68 to +71 (0044h to 0047h)	UART0 transmit, NACK0	UART0 transmit, NACK0
18	+72 to +75 (0048h to 004Bh)	UART0 receive, ACK0	UART0 receive, ACK0
19	+76 to +79 (004Ch to 004Fh)	UART1 transmit, NACK1	UART1 transmit, NACK1
20	+80 to +83 (0050h to 0053h)	UART1 receive, ACK1	UART1 receive, ACK1
21	+84 to +87 (0054h to 0057h)	Timer A0	Timer A0
22	+88 to +91 (0058h to 005Bh)	Timer A1	Timer A1
23	+92 to +95 (005Ch to 005Fh)	Timer A2	Timer A2
24	+96 to +99 (0060h to 0063h)	Timer A3	Timer A3
25	+100 to +103 (0064h to 0067h)	Timer A4	Timer A4
26	+104 to +107 (0068h to 006Bh)	Timer B0	Timer B0
27	+108 to +111 (006Ch to 006Fh)	Timer B1	Timer B1
28	+112 to +115 (0070h to 0073h)	Timer B2	Timer B2

Table 2.18 Differences between Interrupt Vectors - (2/2)

Software Interrupt Number	Vector Address	M16C/62P	M16C/65
29	+116 to +119 (0074h to 0077h)	$\overline{\text{INT0}}$	$\overline{\text{INT0}}$
30	+120 to +123 (0078h to 007Bh)	$\overline{\text{INT1}}$	$\overline{\text{INT1}}$
31	+124 to +127 (007Ch to 007Fh)	$\overline{\text{INT2}}$	$\overline{\text{INT2}}$
32 to 40	+128 to +131 (0080h to 0083h) to +160 to +163 (00A0h to 00A3h)	INT instruction interrupt	INT instruction interrupt
41	+164 to +167 (00A4h to 00A7h)		DMA2
42	+168 to +171 (00A8h to 00ABh)		DMA3
43	+172 to +175 (00ACh to 00AFh)		UART5 start/stop condition detection, bus collision detection, CEC1
44	+176 to +179 (00B0h to 00B3h)		UART5 transmit, NACK5, CEC2
45	+180 to +183 (00B4h to 00B7h)		UART5 receive, ACK5
46	+184 to +187 (00B8h to 00BBh)		UART6 start/stop condition detection, bus collision detection, real-time clock period
47	+188 to +191 (00BCh to 00BFh)		UART6 transmit, NACK6, real-time clock compare
48	+192 to +195 (00C0h to 00C3h)		UART6 receive, ACK6
49	+196 to +199 (00C4h to 00C7h)		UART7 start/stop condition detection, bus collision detection, remote control 0
50	+200 to +203 (00C8h to 00CBh)		UART7 transmit, NACK7, remote control 1
51	+204 to +207 (00CCh to 00CFh)		UART7 receive, ACK7
52 to 58	+208 to +211 (00D0h to 00D3h) to +232 to +235 (00E8h to 00EBh)		INT instruction interrupt
59	+236 to +239 (00ECh to 00EFh)		I^2C-bus interface interrupt
60	+240 to +243 (00F0h to 00F3h)		SCL/SDA interrupt
61 to 63	+244 to +247 (00F4h to 00F7h) to +252 to +255 (00FCh to 00FFh)		INT instruction interrupt

Table 2.19 Differences between Registers Associated with Interrupts

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
IFSR3A	—	0205h	—	—	M16C/65 only
IFSR2A	035Eh	0206h	—	Different address	
			2	No register bit	Interrupt request source select bit 0: Not used 1: I²C-bus interface
			3	No register bit	Interrupt request source select bit 0: Not used 1: SCL/SDA
			4	No register bit	Interrupt request source select bit 0: UART7 start/stop condition detection, bus collision detection 1: Remote control receiving function 0
			5	No register bit	Interrupt request source select bit 0: UART7 transmission, NACK 1: Remote control receiving function 1
			6	Interrupt request factor select bit 0: Timer B3 1: UART0 bus collision detection	Interrupt request source select bit 0: Timer B3 1: UART0 start/stop condition detection, bus collision detection
			7	Interrupt request factor select bit 0: Timer B4 1: UART1 bus collision detection	Interrupt request source select bit 0: Timer B4 1: UART1 start/stop condition detection, bus collision detection
IFSR	035Fh	0207h	—	Different address	
AIER	0009h	020Eh	—	Different address	
AIER2	01BBh	020Fh	—	Different address	
RMAD0	0010h to 0012h	0210h to 0212h	—	Different address	
RMAD1	0014h to 0016h	0214h to 0216h	—	Different address	
RMAD2	01B8h to 01BAh	0218h to 021Ah	—	Different address	
RMAD3	01BCh to 01BEh	021Ch to 021Eh	—	Different address	

2.10 Differences in Watchdog Timers

Table 2.20 lists Differences between Watchdog Timers and Table 2.21 lists Differences in Registers Associated with Watchdog Timer.

Table 2.20 Differences between Watchdog Timers

Item	M16C/62P	M16C/65
Count source protect mode enable setting	Set the PM22 bit to 1.	Set the CSPRO bit to 1. (1)
Watchdog timer cycle in count source protection mode	Approx. 32.8 ms (32768 / approx. 1 MHz)	Approx. 32.8 ms (4096 / approx. 125 kHz)
Watchdog timer counter refresh	Watchdog timer counter is initialized and starts counting by writing to the WDTS register.	Write 00h, and then FFh to the WDTR register
Count start conditions		Count automatically starts after reset by setting the WDTON bit in the OFS1 address to 0. Count starts by writing to the WDTS register.

Note:
1. When the CSPROINI bit in the OFS1 address is 0, the value after reset becomes 1.

Table 2.21 Differences in Registers Associated with Watchdog Timers

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
WDTS	000Eh	037Eh	—	Different address	
WDC	000Fh	037Fh	—	Different address	
			5	Cold Start / Warm Start Discrimination Flag 0 : Cold Start 1 : Warm Start	No register bit
VW2C	—	002Ch	—	—	M16C/65 only
CSPR	—	037Ch	—	—	M16C/65 only
WDTR	—	037Dh	—	—	M16C/65 only

2.11 Differences between DMACs

Table 2.22 lists Difference between DMACs, Table 2.23 to 2.24 list Differences in DMA Request Sources, and Table 2.25 lists Differences between Registers Associated with DMACs.

Table 2.22 Difference between DMACs

Item	M16C/62P	M16C/65
Number of channels	2 channels	4 channels

Table 2.23 Differences between DMAi Request Sources (i=0 and 1 in M16C/62P; i=0 to 3 in M16C/65)(1/2)

DSEL4 to DSEL0	M16C/62P		M16C/65	
	DMS = 0	DMS = 1	DMS = 0	DMS = 1
00000b	Falling edge of $\overline{\text{INTi}}$ pin	—	Falling edge of $\overline{\text{INTi}}$ pin	—
00001b	Software trigger	—	Software trigger	—
00010b	Timer A0	—	Timer A0	—
00011b	Timer A1	—	Timer A1	—
00100b	Timer A2	—	Timer A2	—
00101b	Timer A3	SI/O3 (DMA1 only)	Timer A3	SI/O3 (DMA1, DMA3 only)
00110b	Timer A4	DMA0: Both edges of $\overline{\text{INTi}}$ pin DMA1: SI/O4	Timer A4	DMA0, DMA2: Both edges of $\overline{\text{INTi}}$ pin DMA1, DMA3: SI/O4
00111b	Timer B0	DMA0, DMA2: Timer B3 DMA1, DMA3: Both edges of $\overline{\text{INTi}}$ pin	Timer B0	DMA0, DMA2: Timer B3 DMA1,DMA3: Both edges of $\overline{\text{INTi}}$ pin
01000b	Timer B1	Timer B4 (DMA0 only)	Timer B1	Timer B4 (DMA0, DMA2 only)
01001b	Timer B2	Timer B5 (DMA0 only)	Timer B2	Timer B5 (DMA0, DMA2 only)
01010b	UART0 transmission	—	UART0 transmission	—
01011b	DMA0: UART0 reception DMA1: UART0 reception / ACK0	—	DMA0, DMA2: UART0 reception DMA1, DMA3: UART0 reception / ACK0	—
01100b	UART2 transmission	—	UART2 transmission	—
01101b	DMA0: UART2 reception DMA1: UART2 reception / ACK2	—	DMA0, DMA2: UART2 reception DMA1, DMA3: UART2 reception / ACK2	—
01110b	A/D converter	—	A/D converter	—
01111b	DMA0: UART1 transmission DMA1: UART1 reception / ACK1	—	DMA0, DMA2: UART1 transmission DMA1, DMA3: UART1 reception / ACK1	—

Table 2.24 Differences between DMAi Request Sources (i=0 and 1 in M16C/62P; i=0 to 3 in M16C/65)(2/2)

DSEL4 to DSEL0	M16C/62P		M16C/65	
	DMS = 0	DMS = 1	DMS = 0	DMS = 1
10000b			DMA0, DMA2: UART1 reception DMA1, DMA3: UART1 transmission	Falling edge of $\overline{\text{INTj}}$ pin (j = 4 to 7)
10001b			UART5 transmission	Both edges of $\overline{\text{INTj}}$ pin
10010b			DMA0, DMA2: UART5 reception DMA1, DMA3: UART5 reception / ACK5	—
10011b			UART6 transmission	—
10100b			DMA0, DMA2: UART6 reception DMA1, DMA3: UART6 reception / ACK6	—
10101b			UART7 transmission	—
10110b			DMA0, DMA2: UART7 reception DMA1, DMA3 UART7 reception / ACK7	—

Table 2.25 Differences between Registers Associated with DMACs

Symbol	Address		Bits	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
DAR0	0024h to 0026h	0184h to 0186h	—	Different address	
DAR1	0034h to 0036h	0194h to 0196h	—	Different address	
DAR2	—	01A4h to 01A6h	—	—	M16C/65 only
DAR3	—	01B4h to 01B6h	—	—	M16C/65 only
DM0CON	002Ch	018Ch	—	Different address	
DM1CON	003Ch	019Ch	—	Different address	
DM2CON	—	01ACh	—	—	M16C/65 only
DM3CON	—	01BCh	—	—	M16C/65 only
SAR0	0020h to 0022h	0180h to 0182h	—	Different address	
SAR1	0030h to 0032h	0190h to 0192h	—	Different address	
SAR2	—	01A0h to 01A2h	—	—	M16C/65 only
SAR3	—	01B0h to 01B2h	—	—	M16C/65 only
TCR0	0028h to 0029h	0188h to 0189h	—	Different address	
TCR1	0038h to 0039h	0198h to 0199h	—	Different address	
TCR2	—	01A8h to 01A9h	—	—	M16C/65 only
TCR3	—	01B8h to 01B9h	—	—	M16C/65 only
DM0SL	03B8h	0398h	—	Different address	
DM1SL	03BAh	039Ah	—	Different address	
DM2SL	—	0390h	—	—	M16C/65 only
DM3SL	—	0392h	—	—	M16C/65 only

2.12 Differences in Timers

Table 2.26 lists Differences between Timers, and Table 2.27 to Table 2.28 list Differences in Registers Associated with Timers.

Table 2.26 Differences between Timers

Item	M16C/62P	M16C/65
Count source	f1, f2, f8, f32, fC32	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-S, fOCO-F, fC32
Output polarity inversion function	No	Yes
Clock select prior to timer AB division	No	Selectable from f1 and fOCO-F
Programmable output mode	No	Yes
Count direction (up/down) selected by the TAiOUT pin (i = 0 to 4)	Yes	No
Default value in pulse period/pulse width measurement modes	Undefined	Programmable
Read from timer register when in pulse period/pulse width measurement modes	Contents of the reload register (measurement result) can be read by reading the TBj register (j = 0 to 5).	When bits PPWFSk2 to PPWFSk0 in the PPWFSk register (k = 1 and 2) are 0: • Contents of the reload register (measurement result) can be read by reading the TBj register. When bits PPWFSk2 to PPWFSk0 in the PPWFSk register are 1: • Contents of the counter (counter value) can be read by reading the TBj register • Contents of the reload register (measurement result) can be read by reading the TBj1 register
Write to timer register when in pulse period/pulse width measurement modes	The value written to the TBj register is not written to neither the reload register nor the counter.	When a value is written to the TBj register while the counter stops, the value is written to both the reload register and the counter.
Overflow flag clear method	Wait one or more count source cycles after the MR3 bit becomes 1 (overflow) while the TBjS bit is 1 (start counting), then write a value to the TBjMR register.	Write a value to the TBjMR register

Table 2.27 Differences between Registers Associated with Timers (1/2)

Symbol	Address		Bits	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
TACS0 to TACS2	—	01D0h to 01D2h	2 - 0	—	TAi count source select bit (i = 0, 2, and 4) Select the TAi count source
			3	—	TAi count source option specified bit 0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled
			6 - 4	—	TAj count source select bit (j = 1 and 3) Select the TAj count source
			7	—	TAj count source option specified bit 0: TCK0 to TCK1 enabled, TCS4 to TCS6 disabled 1: TCK0 to TCK1 disabled, TCS4 to TCS6 enabled
TA0MR to TA4MR	0396h to 039Ah	0336h to 033Ah	—	Different address	
			4	Up/Down switching factor select bit 0: UDF register 1: Input signal to TAiOUT pin	—
TA0	0386h to 0387h	0326h to 0327h	—	Different address	
TA1	0388h to 0389h	0328h to 0329h	—	Different address	
TA2	038Ah to 038Bh	032Ah to 032Bh	—	Different address	
TA3	038Ch to 038Dh	032Ch to 032Dh	—	Different address	
TA4	038Eh to 038Fh	032Eh to 032Fh	—	Different address	
TABSR	0380h	0320h	—	Different address	
UDF	0384h	0324h	—	Different address	
ONSF	0382h	0322h	—	Different address	
TRGSR	0383h	0323h	—	Different address	
CPSRF	0381h	0015h	—	Different address	
TCKDIVC0	—	01CBh	—	—	M16C/65 only
PWMFS	—	01D4h	—	—	M16C/65 only
TAPOFS	—	01D5h	—	—	M16C/65 only
TAOW	—	01D8h	—	—	M16C/65 only
TA11	0342h to 0343h	0302h to 0303h	—	Different address	
			—	—	Used in programmable output mode
TA21	0344h to 0345h	0304h to 0305h	—	Different address	
			—	—	Used in programmable output mode
TA41	0346h to 0347h	0306h to 0307h	—	Different address	
			—	—	Used in programmable output mode

Table 2.28 Differences between Registers Associated with Timers (2/2)

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
TBCS0 TBCS1 TBCS2 TBCS3	—	01C8h 01C9h 01E8h 01E9h	2 - 0	—	TBi count source select bit (i = 0, 2, 3, and 5) Select the TBi count source
			3	—	TBi count source option specified bit 0: TCK0 to TCK1 enabled, TCS0 to TCS2 disabled 1: TCK0 to TCK1 disabled, TCS0 to TCS2 enabled
			6 - 4	—	TBj count source select bit (j = 1 and 4) Select the TBj count source
			7	—	TBj count source option specified bit 0: TCK0 to TCK1 enabled, TCS4 to TCS6 disabled 1: TCK0 to TCK1 disabled, TCS4 to TCS6 enabled
TB0MR to TB2MR	039Bh to 039Dh	033Bh to 033Dh	—	Different address	
TB3MR to TB5MR	035Bh to 035Dh	031Bh to 031Dh	—	Different address	
TB0	0390h to 0391h	0330h to 0331h	—	Different address	
TB1	0392h to 0393h	0332h to 0333h	—	Different address	
TB2	0394h to 0395h	0334h to 0335h	—	Different address	
TB3	0350h to 0351h	0310h to 0311h	—	Different address	
TB4	0352h to 0353h	0312h to 0313h	—	Different address	
TB5	0354h to 0355h	0314h to 0315h	—	Different address	
TBSR	0340h	0300h	—	Different address	
TABSR	0380h	0320h	—	Different address	
PPWFS1	—	01C6h	—	—	M16C/65 only
PPWFS2	—	01E6h	—	—	M16C/65 only
TB01	—	01C0h to 01C1h	—	—	M16C/65 only
TB11	—	01C2h to 01C3h	—	—	M16C/65 only
TB21	—	01C4h to 01C5h	—	—	M16C/65 only
TB31	—	01E0h to 01E1h	—	—	M16C/65 only
TB41	—	01E2h to 01E3h	—	—	M16C/65 only
TB51	—	01E4h to 01E5h	—	—	M16C/65 only

2.13 Differences between Three-phase Motor Control Timer Functions

Table 2.29 lists Differences between Three-phase Motor Control Timer Functions and Table 2.30 lists Differences between Registers Associated with Three-phase Motor Control Timer Functions.

Table 2.29 Differences between Three-phase Motor Control Timer Functions

Item	M16C/62P	M16C/65
Count source	f1, f2, f8, f32, fC32	f1TIMAB, f2TIMAB, f8TIMAB, f32TIMAB, f64TIMAB, fOCO-S, fOCO-F, fC32
Position data retain function	No	Yes
Three-phase PWM output pin select function	No	Yes

Table 2.30 Differences between Registers Associated with Three-phase Motor Control Timer Functions

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
DTT	034Ch	030Ch	—	Different address	
ICTB2	034Dh	030Dh	—	Different address	
IDB0	034Ah	030Ah	—	Different address	
IDB1	034Bh	030Bh	—	Different address	
INVC0	0348h	0308h	—	Different address	
INVC1	0349h	0309h	—	Different address	
TA1	0388h to 0389h	0328h to 0329h	—	Different address	
TA2	038Ah to 038Bh	032Ah to 032Bh	—	Different address	
TA4	038Eh to 038Fh	032Eh to 032Fh	—	Different address	
TA11	0342h to 0343h	0302h to 0303h	—	Different address	
TA21	0344h to 0345h	0304h to 0305h	—	Different address	
TA41	0346h to 0347h	0306h to 0307h	—	Different address	
TB2SC	039Eh	033Eh	—	Different address	
TB2	0394h to 0395h	0334h to 0335h	—	Different address	
TRGSR	0383h	0323h	—	Different address	
TABSR	0380h	0320h	—	Different address	
PDRF	—	030Eh	—	—	M16C/65 only
PFCR	—	0318h	—	—	M16C/65 only
TPRC	—	01DAh	—	—	M16C/65 only

2.14 Differences between Serial Interfaces

Table 2.31 lists Differences between Serial Interfaces, and Table 2.32 to Table 2.33 list Differences in Registers Associated with Serial Interface.

Table 2.31 Differences between Serial Interfaces

Item		M16C/62P	M16C/65
Clock synchronous/asynchronous		3 channels (UART0 to UART2)	6 channels (UART0 to 2, UART5 to 7)
I^2C mode			
Special mode 2			
IE mode			
UART0 to UART2, UART5 to UART7 clock prior to division select function		f1 only	Selectable from f1 and fOCO-F
SI/O3,4	Output control after transmission	The state of pins SOUT3 and SOUT4 after transmission is high-impedance.	The state after transmission can be selected whether to set high-impedance or retain the last bit level, by bits SM27 and SM26 in the S34C2 register.
	SI/O prior to division clock	f1 only	Selectable from f1 and fOCO-F

Table 2.32 Differences between Registers Associated with Serial Interfaces (1/2)

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
U0BRG	03A1h	0249h	—	Different address	
U0C0	03A4h	024Ch	—	Different address	
U0C1	03A5h	024Dh	—	Different address	
U0MR	03A0h	0248h	—	Different address	
U0RB	03A6h to 03A7h	024Eh to 024Fh	—	Different address	
U0SMR	036Fh	0247h	—	Different address	
			3	LSYN (1)	Reserved bit
U0SMR2	036Eh	0246h	—	Different address	
U0SMR3	036Dh	0245h	—	Different address	
U0SMR4	036Ch	0244h	—	Different address	
U0TB	03A2h to 03A3h	024Ah to 024Bh	—	Different address	
UCON	03B0h	0250h	—	Different address	
UCLKSEL0	—	0252h	—	—	M16C/65 only
U1BRG	03A9h	0259h	—	Different address	
U1C0	03ACh	025Ch	—	Different address	
U1C1	03ADh	025Dh	—	Different address	
U1MR	03A8h	0258h	—	Different address	
U1RB	03AEh to 03AFh	025Eh to 025Fh	—	Different address	
U1SMR	0373h	0257h	—	Different address	
			3	LSYN (1)	Reserved bit
U1SMR2	0372h	0256h	—	Different address	
U1SMR3	0371h	0255h	—	Different address	
U1SMR4	0370h	0254h	—	Different address	
U1TB	03AAh to 03ABh	025Ah to 025Bh	—	Different address	
U2BRG	0379h	0269h	—	Different address	
U2C0	037Ch	026Ch	—	Different address	
U2C1	037Dh	026Dh	—	Different address	
U2MR	0378h	0268h	—	Different address	
U2RB	037Eh to 037Fh	026Eh to 026Fh	—	Different address	
U2SMR	0377h	0267h	—	Different address	
			3	LSYN (1)	Reserved bit
U2SMR2	0376h	0266h	—	Different address	
U2SMR3	0375h	0265h	—	Different address	
U2SMR4	0374h	0264h	—	Different address	
U2TB	037Ah to 037Bh	026Ah to 026Bh	—	Different address	

Note:
1. Only enabled in M3062LFGPFP and M3062LFGPGP. This is a reserved bit in other products.

Table 2.33 Differences in Registers Associated with Serial Interfaces (2/2)

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
U5BRG	—	0289h	—	—	M16C/65 only
U5C0	—	028Ch	—	—	M16C/65 only
U5C1	—	028Dh	—	—	M16C/65 only
U5MR	—	0288h	—	—	M16C/65 only
U5RB	—	028Eh to 028Fh	—	—	M16C/65 only
U5SMR	—	0287h	—	—	M16C/65 only
U5SMR2	—	0286h	—	—	M16C/65 only
U5SMR3	—	0285h	—	—	M16C/65 only
U5SMR4	—	0284h	—	—	M16C/65 only
U5TB	—	028Ah to 028Bh	—	—	M16C/65 only
U6BRG	—	0299h	—	—	M16C/65 only
U6C0	—	029Ch	—	—	M16C/65 only
U6C1	—	029Dh	—	—	M16C/65 only
U6MR	—	0298h	—	—	M16C/65 only
U6RB	—	029Eh to 029Fh	—	—	M16C/65 only
U6SMR	—	0297h	—	—	M16C/65 only
U6SMR2	—	0296h	—	—	M16C/65 only
U6SMR3	—	0295h	—	—	M16C/65 only
U6SMR4	—	0294h	—	—	M16C/65 only
U6TB	—	029Ah to 029Bh	—	—	M16C/65 only
U7BRG	—	02A9h	—	—	M16C/65 only
U7C0	—	02ACh	—	—	M16C/65 only
U7C1	—	02ADh	—	—	M16C/65 only
U7MR	—	02A8h	—	—	M16C/65 only
U7RB	—	02AEh to 02AFh	—	—	M16C/65 only
U7SMR	—	02A7h	—	—	M16C/65 only
U7SMR2	—	02A6h	—	—	M16C/65 only
U7SMR3	—	02A5h	—	—	M16C/65 only
U7SMR4	—	02A4h	—	—	M16C/65 only
U7TB	—	02AAh to 02ABh	—	—	M16C/65 only
S3C	0362h	0272h	—	Different address	
S4C	0366h	0276h	—	Different address	
S3BRG	0363h	0273h	—	Different address	
S4BRG	0367h	0277h	—	Different address	
S3TRR	0360h	0270h	—	Different address	
S4TRR	0364h	0274h	—	Different address	
S34C2	—	0278h	—	—	M16C/65 only

2.15 Differences between A/D Converters

Table 2.34 lists Differences between A/D Converters and Table 2.35 lists Differences in Registers Associated with A/D Converters.

Table 2.34 Differences between A/D Converters

Item	M16C/62P	M16C/65
Operation clock ϕAD	fAD, fAD divided by 2, fAD divided by 3, fAD divided by 4, fAD divided by 6, and fAD divided by 12	f1, f1 divided by 2, f1 divided by 3, f1 divided by 4, f1 divided by 6, f1 divided by 12, fOCO40M divided by 2, fOCO40M divided by 3, fOCO40M divided by 4, fOCO40M divided by 6, and fOCO40M divided by 12
Conversion rate per pin	Without sample and hold 8-bit resolution: 49 ϕAD cycles 10-bit resolution: 59 ϕAD cycles With sample and hold 8-bit resolution: 28 ϕAD cycles 10-bit resolution: 33 ϕAD cycles	Minimum 43 ϕAD cycles
External op-amp connection mode	Yes	No
Resolution	8-bit/10-bit (selectable)	10-bit
Sample and hold	Yes/No (selectable)	Yes
fAD	f1 only	Selectable from f1 and fOCO40M
Open-circuit detection assist function	No	Yes

Table 2.35 Differences in Registers Associated with A/D Converters

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
ADCON1	03D7h	03D7h	3	8/10-Bit Mode Select Bit 0: 8-bit mode 1: 10-bit mode	No register bit
			5	Vref Connect Bit 0: Vref not connected 1: Vref connected	A/D standby bit 0: A/D operation stopped (standby) 1: A/D operation enabled
			7-6	External Op-Amp Connection Mode Bit 0 0: ANEX0 and ANEX1 are not used 0 1: ANEX0 input is A/D converted 1 0: ANEX1 input is A/D converted 1 1: External op-amp connection mode	Extended pin select bit 0 0: ANEX0 and ANEX1 are not used 0 1: ANEX0 input is A/D converted 1 0: ANEX1 input is A/D converted 1 1: Do not set
ADCON2	03D4h	03D4h	0	A/D Conversion Method Select Bit 0: Without sample and hold function 1: With sample and hold function	No register bit
			7	No register bit	fAD select bit 0: f1 1: fOCO40M
AINRST	—	03A2h	—	—	M16C/65 only

2.16 Differences between CRC Calculators

Table 2.36 lists Differences between CRC Calculators and Table 2.37 lists Differences between Registers Associated with CRC Calculators.

Table 2.36 Differences between CRC Calculators

Item	M16C/62P	M16C/65
CRC generator polynomial	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$)	CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) or CRC-16 ($X^{16} + X^{15} + X^2 + 1$)
MSB/LSB selection	No	MSB/LSB (selectable)
CRC snoop	No	Yes

Table 2.37 Differences between Registers Associated with CRC Calculators

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
CRCMR	—	03B6h	—	—	M16C/65 only
CRCSAR	—	03B4h to 03B5h	—	—	M16C/65 only

2.17 Differences between Flash Memories

Table 2.38 lists Differences between Flash Memories and Table 2.39 lists Differences between Software Commands, and 2.40 lists Differences between Registers Associated with Flash Memories.

Table 2.38 Differences between Flash Memories

Item	M16C/62P	M16C/65
Program method	1-word units (16-bit)	2-word units (32-bit)
Number of programs and erase cycles	100 times (all areas) or 1,000 times (all blocks other than block A and block 1 in user ROM area)/10,000 times (block A, block 1)	1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash)
User boot function	No	Yes
Forced erase function	No	Yes
Data retention	10 years	20 years

Table 2.39 Differences between Software Commands

Software Command	MCU	First Bus Cycle		Second Bus Cycle		Third Bus Cycle	
		Address	Data	Address	Data	Address	Data
Read array	M16C/62P	X	XXFFh	—	—	—	—
	M16C/65 (1)	X	XXFFh	—	—	—	—
	M16C/65 (2)	B0-7	XXFFh	B8	XXFFh	—	—
Read status register	M16C/62P	X	XX70h	X	SRD	—	—
	M16C/65 (1)	X	XX70h	X	SRD	—	—
	M16C/65 (2)	BA	XX70h	X	SRD	—	—
Clear status register	M16C/62P	X	XX50h	—	—	—	—
	M16C/65 (1)	X	XX50h	—	—	—	—
	M16C/65 (2)	B0-7	XX50h	B8	XX50h	—	—
Program	M16C/62P	WA	XX40h	WA	WD	—	—
	M16C/65 (1)	WA	XX41h	WA	WD0	WA	WD1
	M16C/65 (2)	WA	XX41h	WA	WD0	WA	WD1
Block erase	M16C/62P	X	XX20h	BA	XXD0h	—	—
	M16C/65 (1)	X	XX20h	BA	XXD0h	—	—
	M16C/65 (2)	BA	XX20h	BA	XXD0h	—	—
Erase all unlocked blocks	M16C/62P	X	XXA7h	X	XXD0h	—	—
	M16C/65 (1)	—	—	—	—	—	—
	M16C/65 (2)	—	—	—	—	—	—
Read lock bit status	M16C/62P	X	XX71h	BA	XXD0h	—	—
	M16C/65 (1)	X	XX71h	BA	XXD0h	—	—
	M16C/65 (2)	BA	XX71h	BA	XXD0h	—	—
Block blank check (3)	M16C/62P	—	—	—	—	—	—
	M16C/65 (1)	X	XX25h	BA	XXD0h	—	—
	M16C/65 (2)	BA	XX25h	BA	XXD0h	—	—

Notes:
1. Program ROM 1 is not over 512 KB
2. Program ROM 1 is over 512 KB
3. Block blank check command is designed for programmer manufacturer. Not for customers in general.

SRD: Data in the status register (D7 to D0)
WA: Even write address (but in M16C/65, set the end of the address to 0, 4, 8, or C (hexadecimal) only.)
WD: 16-bit write data
WD0: 16-bit write data lower word
WD1: 16-bit write data upper word
BA: Highest-order block address (even address)
B0-7: Any even address in blocks 0 to 7, program ROM2, or data flash
B8: Any even address in blocks after 8.
X: Any even address in user ROM area
XX: Eight high-order bits of command code (ignored)

Table 2.40 Differences between Registers Associated with Flash Memories

Symbol	Address		Bit	Differences	
	M16C/62P	M16C/65		M16C/62P	M16C/65
FIDR	01B4h	—	—	M16C/62P only	—
FMR0	01B7h	0220h	—	Different address	
FMR1	01B5h	0221h	1	EW1 mode select bit 0: EW0 mode 1: EW1 mode	Write to FMR6 register enabled bit 0: Disabled 1: Enabled
			7	Reserved bit	Data flash wait bit 0: 1 wait 1: Follow the setting of the PM17 bit
FMR2	—	0222h	—	—	M16C/65 only
FMR6	—	0230h	—	—	M16C/65 only

2.18 Differences between Flash Memory Block Configurations

The flash ROM block configurations differ between the M16C/62P and the M16C/65. Figure 2.1 shows the Differences between Flash Memory Block Configurations. The differences are marked in yellow.

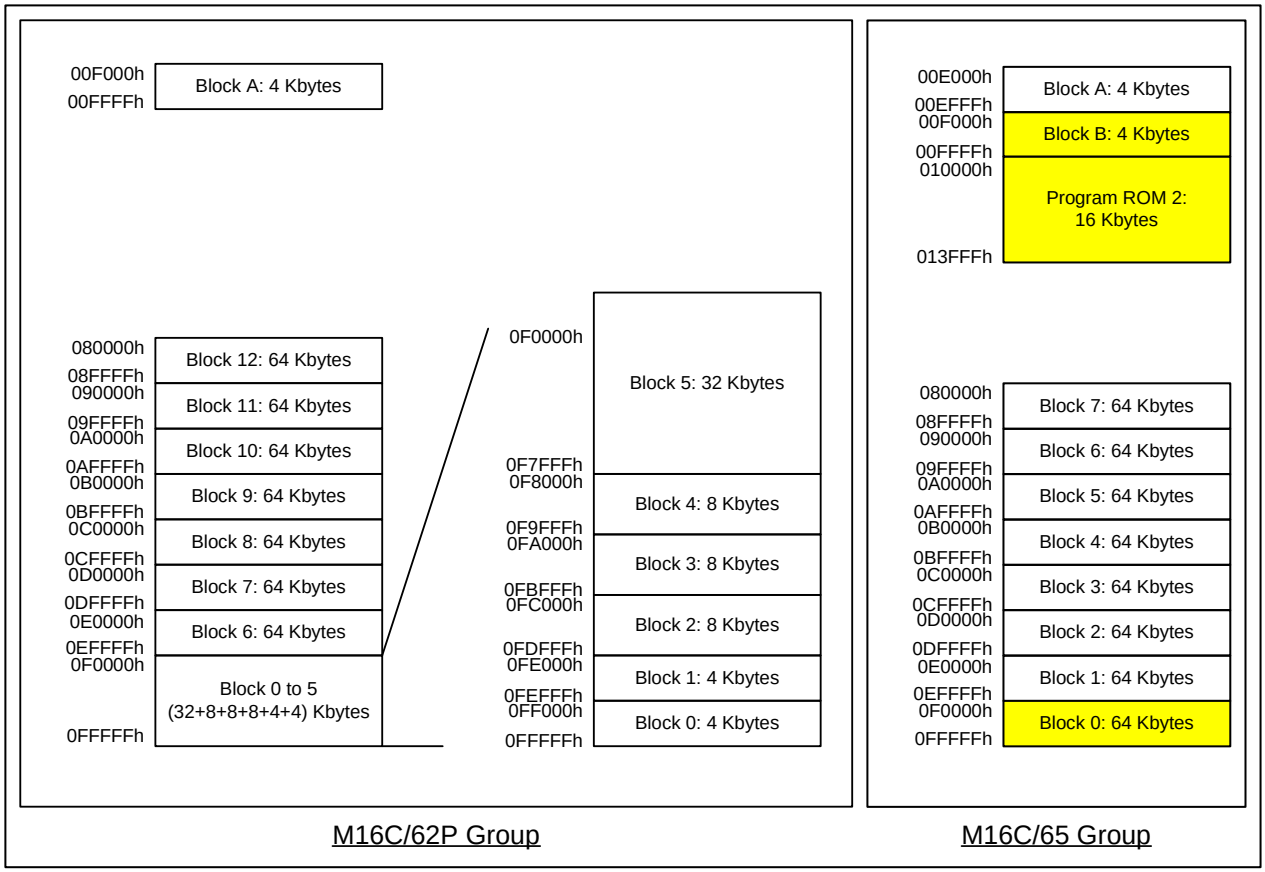

Figure 2.1 Differences between Flash Memory Block Configurations

2.19 New Functions added in the M16C/65

The following functions have been added in the M16C/65 Group MCU:

- Multi-master I^2C-bus interface
- CEC function
- Real-time clock
- PWM function
- Remote control signal receiver

2.20 Differences in Development Tool

Table 2.41 lists Differences in Development Tool.

Table 2.41 Differences in Development Tool

Types of Tool	M16C/62P	M16C/65
C compiler	M3T-NC30WA	M3T-NC30WA
Real-time OS	M3T-MR30	M3T-MR30
Emulator debugger	PC7501	E100
Emulation probe	M3062PT2-EPB	—
MCU unit	—	R0E530650MCU00
Compact emulator	M3062PT3-CPE	—
On-chip debugging emulator	E8 E8a (7-wire system)	E8a (single-wire system)
Renesas starter kits	R0K33062PS001BE	R0K53650ES000BE

3. Reference Documents

M16C/62P Group Hardware Manual Rev.2.41
M16C/65 Group User's Manual: Hardware Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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Revision History	M16C/62P Group, M16C/65 Group Differences between M16C/62P and M16C/65

Rev.	Date	Description	
		Page	Summary
1.00	May 21, 2008	—	First edition issued
1.01	Feb 5, 2009	2	31.25 ns (f(BLCK) = 32 MHz, VCC1 = 3.0 to 5.5 V) 40 ns (f(BCLK) = 25 MHz, VCC1 = 2.7 to 5.5 V) --> 31.25 ns (f(BLCK) = 32 MHz, VCC1 = 2.7 to 5.5 V)
		3	Suspend function delete
1.02	May 29, 2009	2	Table3.1 M16C/65: low-speed on-chip oscillator(125kHz) --> 125 kHz on-chip
			oscillator, high-speed on-chip oscillator(40MHz) --> 40 MHz on-chip oscillator
		2,9	Table 3.1, Table4.11 0 to 3 wait(s) -->0 to 3 cycle(s)
		4	Table3.3 Deleted: P3_0,P2_7,P2_6,P2_3,P2_2,P2_1,P2_0
		5	Table4.1 Added: M16C/65 bit3 VWCE,VD1LS
		6	Table4.5 Added: VCR2 register
		7	Table4.7 Added: bit 3 in the CM1 register, bit 0 in the PM2 register
			Bit5-4 in the PLC0 register added: M16/62P bit4 Set to1, M16C/65 11:Do not set
		10	Table4.14 Added: PD8 register
		11	Table4.16 Added: M16C/62P start/stop condition detection
		12	Table4.17 Modified: Vector Address 46 to 51,and 63
			M16C/65 -(Reserved) --> INT instruction interrupt
		14	Table4.20 Added.
		18	Table4.26 Added: TAOW register
		24	Table4.34 Bit Symbol --> Bit Name,
			Bit 0 in the ADCON2: With --> Without, Without --> With
		26	Table4.37 Deleted: Suspend function
		27	Table4.38 revised.
		28	Table4.39 FMR3 --> FMR2, 0223h --> 0222h
		29	Figure4.1 M16C/62P Block A 080000h --> 00F000h
1.03	Jul 30, 2011	Overall	Updated configuration of this document.
		3	Table 1.1: Deleted the Power Consumption row, and added HOLD input to the External Bus row.
		4	Table 1.2: Added sub items to the Serial Interface, A/D Converter, and CRC Calculator.
		5	Table 1.3: Added last two options to the Address FFFFFh function setting for M16C/65.
		7	Table 2.2: • Deleted “(operates at the same time as voltage monitor 0 reset)” from the M16C/65 column of the Cold start, warm start discrimination method row. • Added Reset Source Determine Register row.
		9	Table 2.6 • Added the 125 kHz on-chip oscillator row. • Added “approx. 40 MHz” to the M16C/65 column of the On-chip oscillator frequency row.

Revision History	M16C/62P Group, M16C/65 Group Differences between M16C/62P and M16C/65

Rev.	Date	Description	
		Page	Summary
1.03	Jul 30, 2011	16	Table 2.20: Changed “Watchdog timer counter initialization” to “Watchdog timer counter refresh”.
		19	Table 2.26: • Changed the descriptions in the M16C/65 column of the Count source. • “Added the Write to timer register in pulse period/pulse width measurement modes” row. • Changed the Overflow flag clear method for M16C/62P.
		22	Table 2.29: Changed the M16C/65 column of the Count source.
		26	Table 2.34: Added the Operation clock ϕAD row.
		27	Table 2.38: Added the Data retention row.
		28	Table 2.39: Added note 3.
		31	Table 2.41: • Changed the statuses of the Emulation probe and Renesas starter kits for M16C/65. • Added the MCU unit row.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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