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H8S/2400 Series

DTC Data Transfer Initiated by IRQ Interrupt

Introduction

This application note describes an example of 128-byte data transfer by using the data transfer controller (DTC). An IRQ interrupt initiates transfer by the DTC.

The DTC is capable of transferring one block (up to 128 bytes) of data in response to a single activation event without CPU intervention.

Target Device

H8S/2472, H8S/2463, H8S/2462 Group

Preface

This application note was prepared using the H8S/2472, H8S/2463, H8S/2462 Group, one of the devices on which operation has been confirmed, as the basis.

This program can be used with other H8S/2400 Series MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

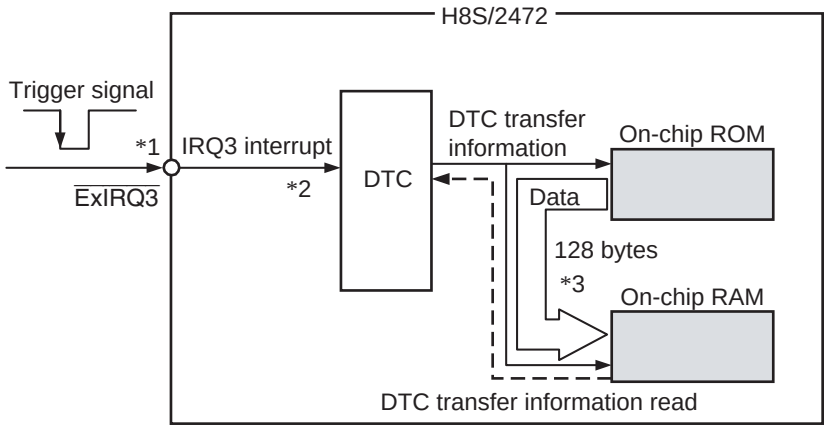
Contents

1. Specifications

In this application note, data in the on-chip ROM are transferred to the on-chip RAM by the DTC, which is activated by the IRQ3 interrupt.

Figure 1 is an overview of the operations, and the list below covers the specifications in detail.

- The DTC is initiated by the IRQ3 interrupt.
- The IRQ interrupt is detected as the falling edge of the signal on the $\overline{\text{ExIRQ3}}$ pin.
- Set the DTC transfer mode as block transfer mode.
- Specify the number of bytes in a block for transfer as 128.
- The DTC transfers 128 bytes of data in response to a single IRQ3 interrupt request.
- The source area for transfer by the DTC is in the on-chip ROM at addresses H'004000 to H'00407F.
- The amount of data for transfer is 128 bytes, consisting of the following sequence of bytes: H'00, H'01,…, H'7F.
- The destination area for transfer by the DTC is in the on-chip RAM at addresses H'FF0800 to H'FF087F.
- The result (pass or fail) of verifying the data transferred by the DTC is stored in the on-chip RAM from within the IRQ3 interrupt processing routine at the end of transfer by the DTC.



Notes: *1 An IRQ3 interrupt is generated on the falling edge of the signal on the $\overline{\text{ExIRQ3}}$ pin.
*2 The DTC is activated by an IRQ3 interrupt.
*3 128 bytes of data are transferred from the on-chip ROM to on-chip RAM.

Figure 1 Overview

2. Conditions for Application

Table 1 Conditions for Application

Item	Contents
Operating frequency	Input clock: 8 MHz System clock (ϕ): 32 MHz (8 MHz multiplied by 4)
Operating voltage	3.3 V
Operating mode	Mode 2 ($\overline{MD2}$ = 1, MD1 = 1)
Integrated development environment	High-performance Embedded Workshop Version 4.05.00.059
Evaluation board	Renesas Technology R0K402472D000BR
C/C++ compiler	Renesas Technology H8S,H8/300 C/C++ Compiler (V.6.02.01.000)
Compile options	-cpu=2600A:24 -optimize=1 -regparam=3 -speed=register,shift,struct,expression
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V.9.04.01.000)
Linker options	-start= CDTCV/0426, PResetPRG,PIntPRG/01000, P,C,C$DSEC,C$BSEC,D/01400, B,R/0FF0800, S/0FF9600

3. Description of Modules Used

3.1 DTC Operation

The DTC stores register information in on-chip RAM. When activated, the DTC reads register information in on-chip RAM and transfers data. After the data transfer, the DTC writes updated register information back to on-chip RAM. The pre-storage of register information in memory makes it possible to transfer data over any required number of channels. The transfer mode can be specified as normal, repeat, or block transfer mode. Setting the CHNE bit in DTC Mode Register B (MRB) to 1 makes it possible to perform a number of transfers with a single activation source (chain transfer).

The 24-bit DTC Source Address Register (SAR) designates the DTC transfer source address, and the 24-bit DTC Destination Address Register (DAR) designates the transfer destination address. After each transfer, SAR and DAR are independently incremented, decremented, or left fixed depending on its register information.

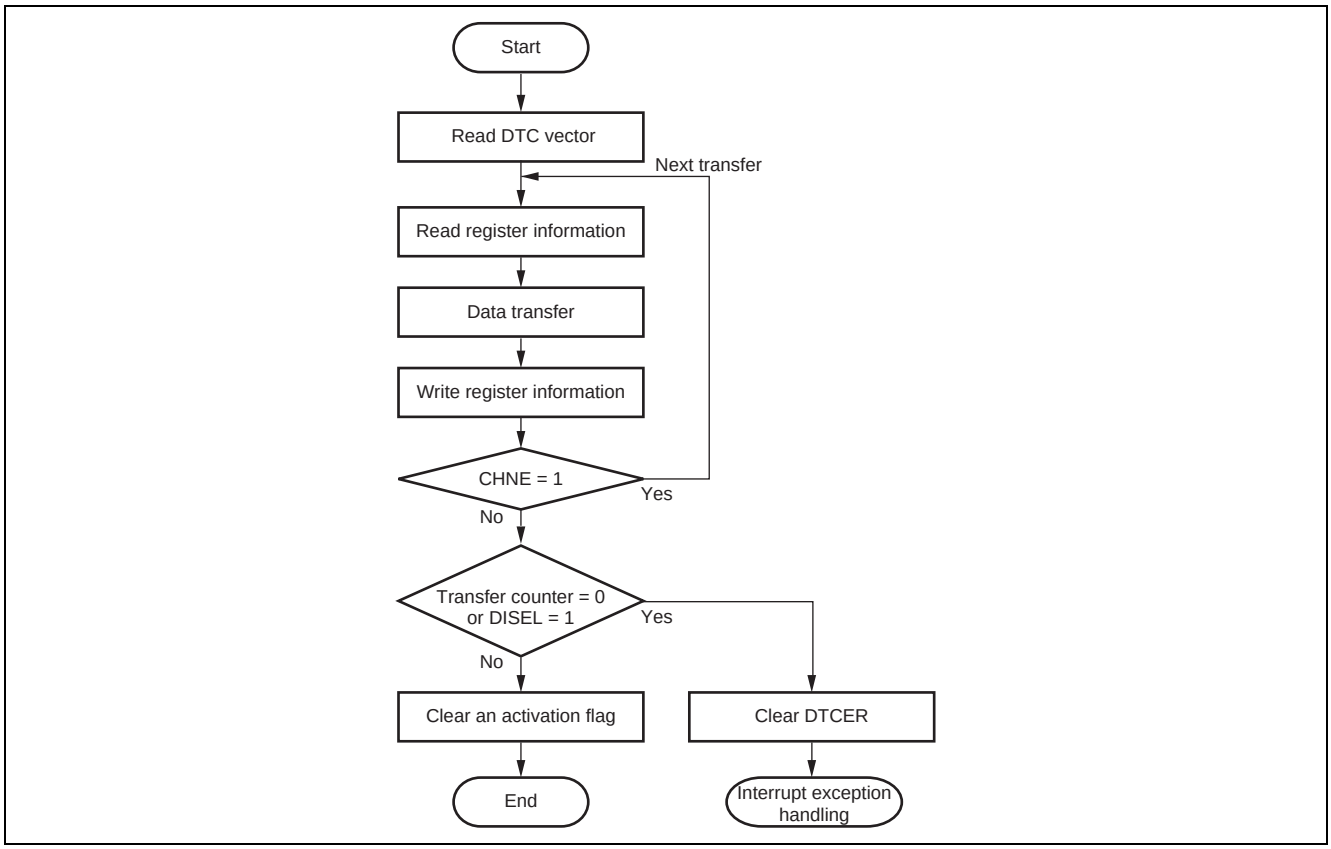


Figure 2 DTC Operation

3.2 DTC Activation Sources

The DTC is activated by an interrupt request or by a write to DTC Vector Register (DTVECR) by software. The interrupt request source to activate the DTC is selected by DTC Enable Registers (DTCER). At the end of a data transfer (or the last consecutive transfer in the case of chain transfer), the interrupt flag that became the activation source or the corresponding DTCER bit is cleared. The activation source flag, in the case of RXI1, for example, is the RDRF flag in SCI_1.

When an interrupt has been designated as a DTC activation source, the existing CPU mask level and interrupt controller priorities have no effect. If there is more than one activation source at the same time, the DTC operates in accordance with the default priorities. Figure 3 shows a block diagram of DTC activation source control.

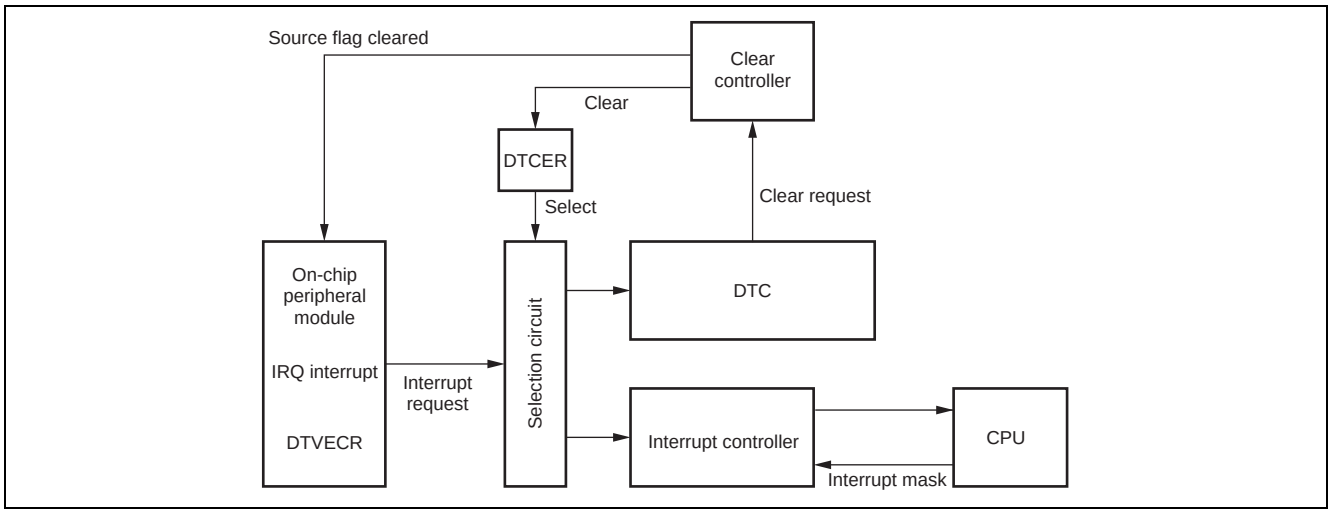


Figure 3 Block Diagram of DTC Activation Source Control

3.3 Location of Register Information and DTC Vector Table

Locate the register information in the on-chip RAM (addresses: H'FFEC00 to H'FFEFFF). Register information should be located at an address that is a multiple of four within the range. The method for locating the register information in address space is shown in figure 4 Locate DTC Mode Register A (MRA), SAR, MRB, DAR, DTC Transfer Count Register A (CRA), and DTC Transfer Count Register B (CRB), in that order, from the start address of the register information. In the case of chain transfer, register information should be located in consecutive areas as shown in figure 4, and the register information start address should be located at the vector address corresponding to the interrupt source in the DTC vector table. The DTC reads the start address of the register information from the vector table set for each activation source, and then reads the register information from that start address.

When the DTC is activated by software, the vector address is obtained from: H'0400 + (DTVECR[6:0] × 2). For example, if DTVECR is H'10, the vector address is H'0420.

The configuration of the vector address is a 2-byte unit. Specify the lower two bytes of the register information start address.

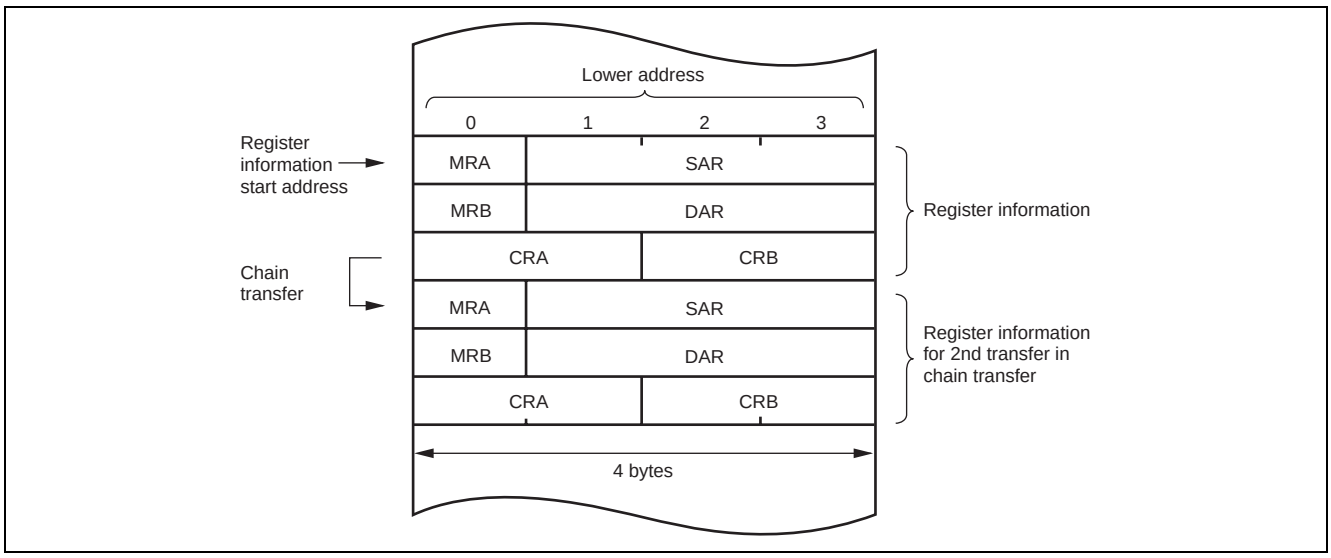


Figure 4 DTC Register Information Location in Address Space

Table 2 Interrupt Sources, DTC Vector Addresses, and Corresponding DTCEs

Activation Source Origin	Activation Source	Vector Number	DTC Vector Address	DTCE*[1]	Priority
Software	Write to DTVECR	DTVECR	H'0400 + (vector number × 2)	—	High
External pins	IRQ0	16	H'0420	DTCEA7	
	IRQ1	17	H'0422	DTCEA6	
	IRQ2	18	H'0424	DTCEA5	
	IRQ3	19	H'0426	DTCEA4	
A/D converter	ADI	28	H'0438	DTCEA3	
EVC	EVENTI	29	H'043A	DTCEC4	
IIC_2	IICI2	76	H'0498	DTCEB6	
IIC_3	IICI3	78	H'049C	DTCED4	
SCI_3	RXI3	81	H'04A2	DTCEC2	
	TXI3	82	H'04A4	DTCEC1	
SCI_1	RXI1	85	H'04AA	DTCEC0	
	TXI1	86	H'04AC	DTCED7	
SSU	RXIS	89	H'04B2	DTCED6	
	TXIS	90	H'04B4	DTCED5	
IIC_0	IICI0	94	H'04BC	DTCEB5	
IIC_1	IICI1	98	H'04C4	DTCED3	
LPC	ERRI	104	H'04D0	DTCEE3	
	IBFI1	105	H'04D2	DTCEE2	
	IBFI2	106	H'04D4	DTCEE1	
	IBFI3	107	H'04D6	DTCEE0	
USB (only in the H8S/2472)	USBINT0	115	H'04E6	DTCEF7	
	USBINT1	118	H'04EC	DTCEF6	Low

Notes: *1 DTCE bits with no corresponding interrupt are reserved, and the write value should always be 0.

3.4 Block Transfer Mode

In block transfer mode, one activation source transfers one block of data. Either the transfer source or the transfer destination is designated as a block area. Table 3 lists the register functions in block transfer mode. The block size can be between 1 and 256. When the transfer of one block ends, the initial state of the block size counter and the address register that is specified as the block area is restored. The other address register is then incremented, decremented, or left fixed according to the register information. From 1 to 65,536 transfers can be specified. Once the specified number of transfers has been completed, a CPU interrupt is requested.

Table 3 Register Functions in Block Transfer Mode

Name	Abbreviation	Function
DTC source address register	SAR	Transfer source address
DTC destination address register	DAR	Transfer destination address
DTC transfer count register AH	CRAH	Holds block size
DTC transfer count register AL	CRAL	Block size counter
DTC transfer count register B	CRB	Transfer counter

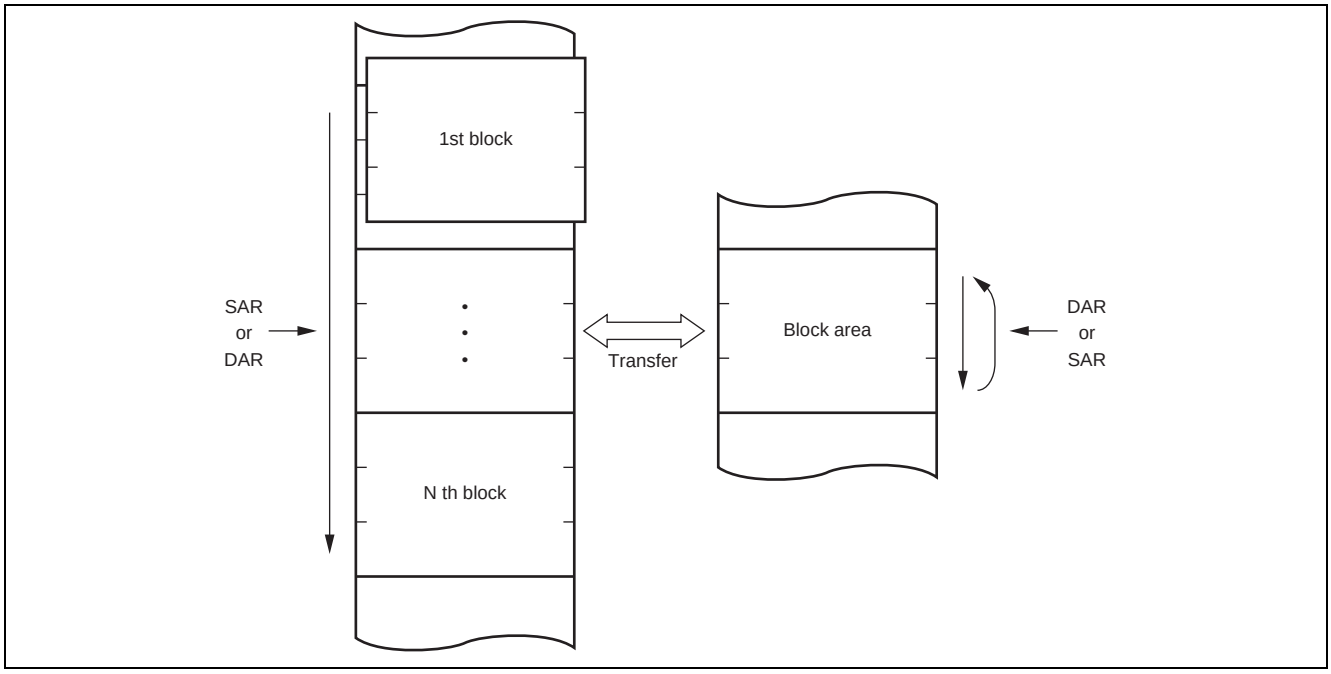


Figure 5 Memory Mapping in Block Transfer Mode

4. Description of Operation

Figure 6 shows the operation described in this application note.

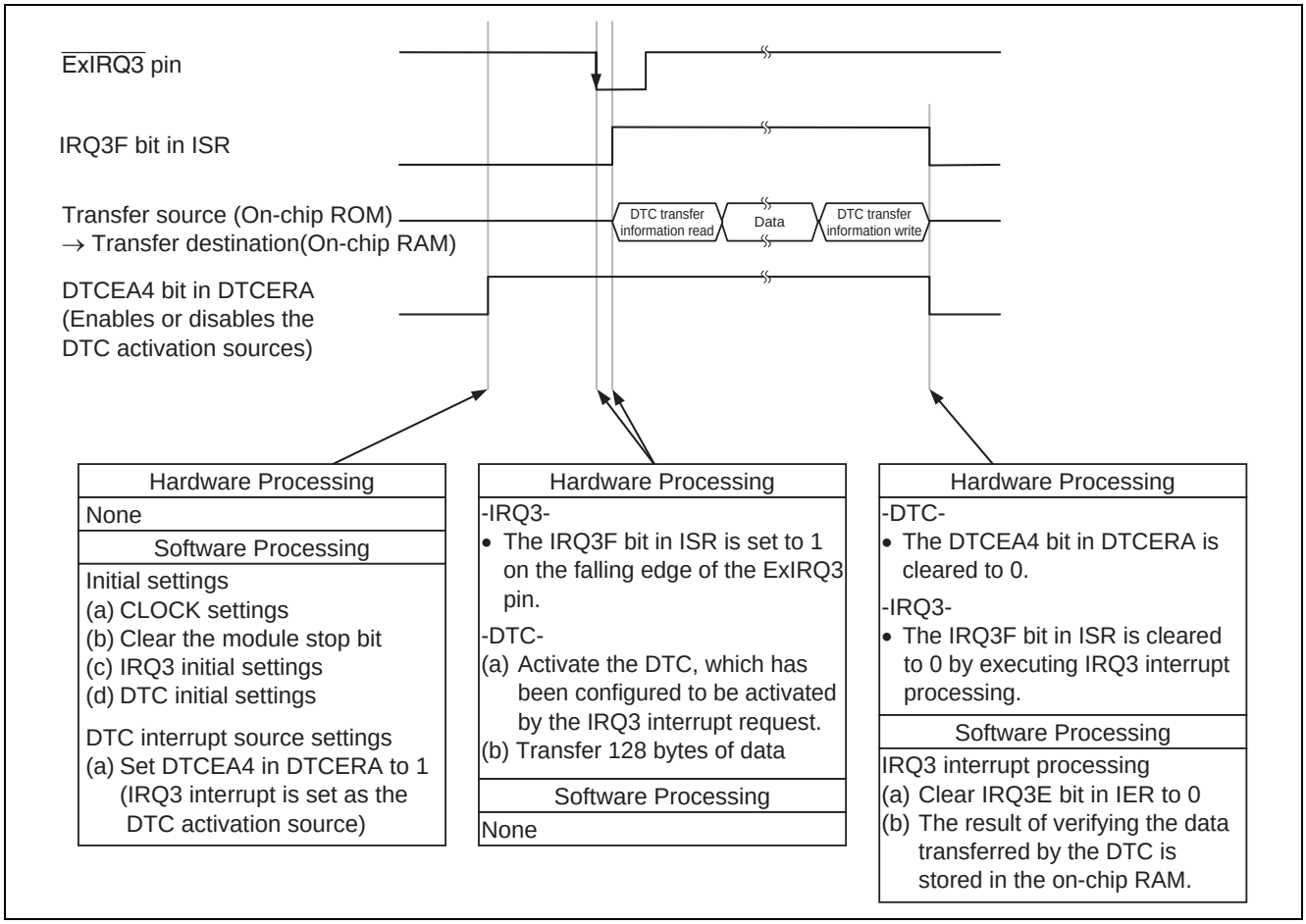


Figure 6 Description of Operation

5. Description of Software

5.1 Symbolic Constants

Table 4 List of Symbolic Constants

Constant Name	Setting	Description	Used by Functions
TRINF	(*(volatile struct dtc_tag *)0xFFEC00)	DTC transfer information start address (H'FFEC00)	init

5.2 ROM Variables

Table 5 List of ROM Variables

Type	Variable Name	Setting	Description	Used by Functions
const unsigned char	datatable[128]	H'00 to H'7F	Transfer data	init, INT_IRQ3
const unsigned short	dtcad	(unsigned short)&TRINF.R_mrasar.R_mra	DTC transfer information start address	—

5.3 RAM Variables

Table 6 List of RAM Variables

Type	Variable Name	Description	Used by Functions
unsigned short	ramarea[128]	DTC transfer destination area	main, init, INT_IRQ3
unsigned char	dtcend	DTC transfer state determination flag 0: DTC transfer is in progress 1: DTC transfer verify error 2: DTC transfer normal completion	main, INT_IRQ3

5.4 Structure

Table 7 List of Structure

Structure Name	Type	Variable Name	Type	Variable Name	Number of bits	Description
struct dtc_tag	union	R_mrasar	unsigned char	R_mra	8	MRA setting value
			unsigned long	R_sar	32	SAR setting value
	union	R_mrbdar	unsigned char	R_mrb	8	MRB setting value
			unsigned long	R_dar	32	DAR setting value
	unsigned short	R_cra	—	—	16	CRA setting value
	unsigned short	R_crb	—	—	16	CRB setting value

5.5 List of Functions

Table 8 List of Functions

Function Name	Descriptions
PowerOn_Reset	• Initial settings function Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, and calls main function.
main	• Main function Calls init function. Determine DTC transfer end.
init	• I/O register initialization function Sets clock mode, module stop mode, IRQ3 interrupt, and DTC operation.
INT_IRQ3	• IRQ3 interrupt processing IRQ3 interrupt request is set to disable. The result of verifying the data transferred by the DTC is stored in the on-chip RAM (dtcend).

5.6 Functions

5.6.1 PowerON_Reset Function

(1) Functional overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then it calls the main function.

(2) Arguments

None

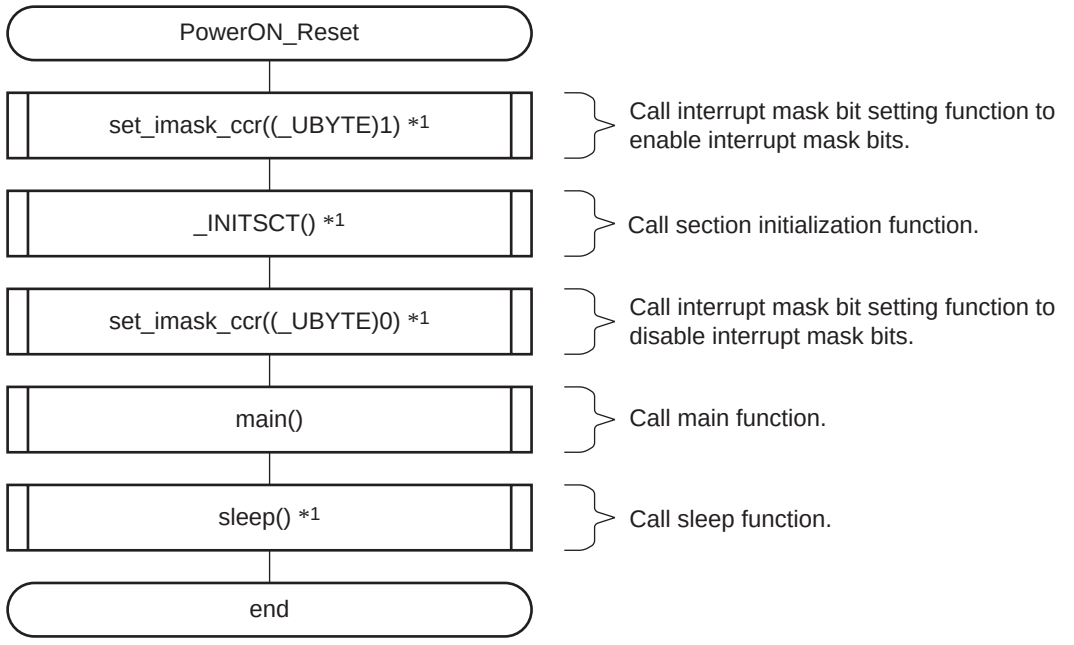
(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart



Note: *1 • set_imask_ccr function: Intrinsic function
• _INITSCT function: Standard library function
• sleep function: Intrinsic function
For details, please refer to the *Development Environment Manual* in the "6. Documents for Reference".

Figure 7 Flowchart (PowerON_Reset)

5.6.2 main Function

(1) Functional overview

The main function calls the init function to detect the end of the DTC transfer.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below.

Note that the setting values shown are those used in this application note and differ from the initial values.

- Mode Control Register (MDCR) Number of bits: 8 Address: H'FFFFC5

Bit	Bit Name	Setting	R/W	Descriptions
7	EXPE	0	R/W	Extended Mode Enable Specifies extended mode. 0: Single-chip mode 1: Extended mode
2	MDS2	—*	R	Mode Select 2 and 1
1	MDS1	—*	R	These bits indicate the input levels at mode pins ($\overline{MD2}$ and MD1) (the current operating mode). Bits MDS2 and MDS1 correspond to $\overline{MD2}$ and MD1, respectively. MDS2 and MDS1 are read-only bits and they cannot be written to. The mode pin ($\overline{MD2}$ and MD1) input levels are latched into these bits when MDCR is read. These latches are canceled by a reset.

Note: * The initial values are determined by the settings of the $\overline{MD2}$ and MD1 pins.

(5) Flowchart

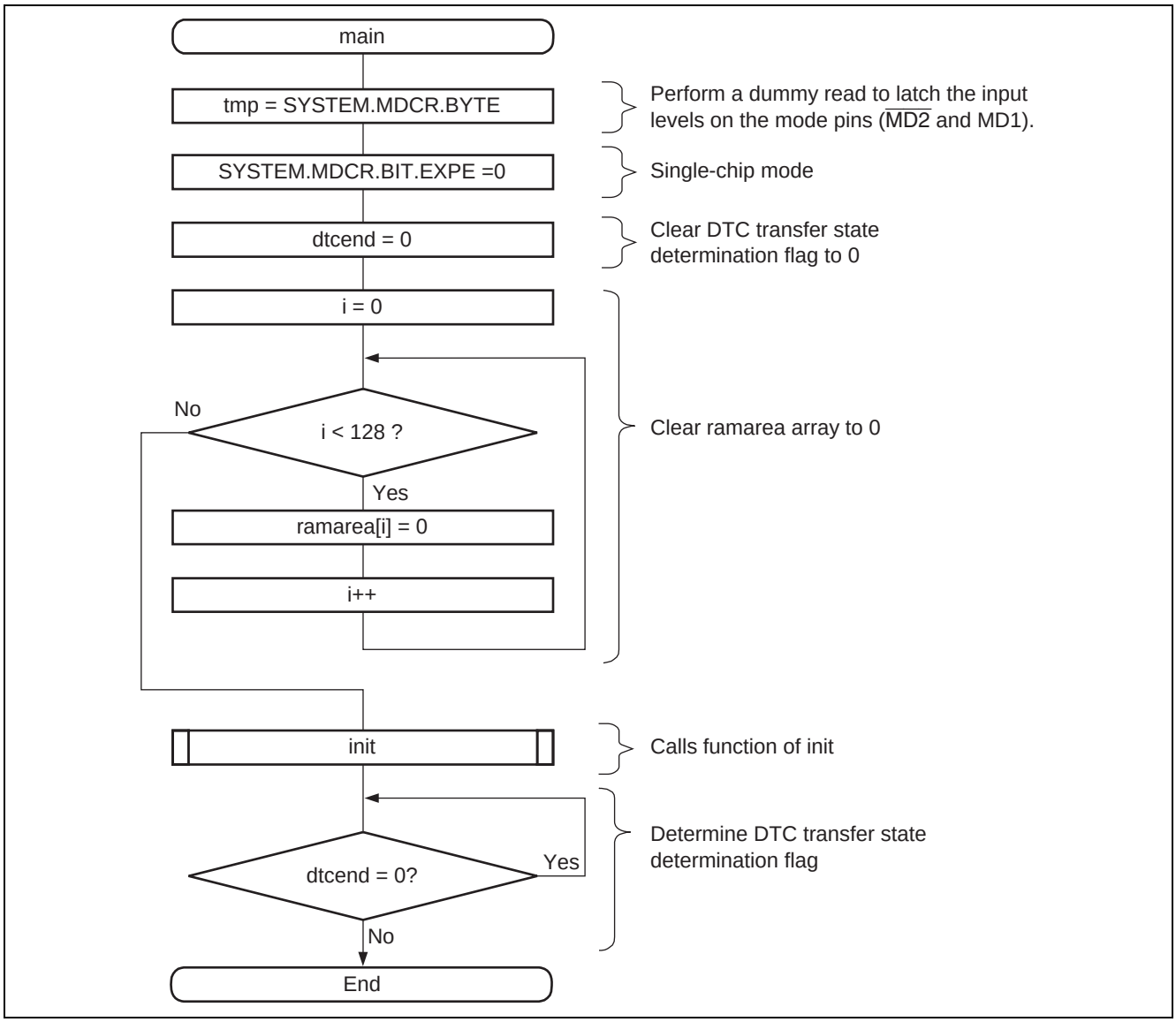


Figure 8 Flowchart

5.6.3 init Function

(1) Functional overview

The init function sets the clock mode, module stop mode, IRQ3 interrupt, and DTC operation.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below.

Note that the setting values shown are those used in this application note and differ from the initial values.

- Interrupt Control Registers A (ICRA) Number of bits: 8 Address: H'FFFEE8

Bit	Bit Name	Setting	R/W	Descriptions
5	ICRA5	0	R/W	Interrupt Control Level 0: Corresponding interrupt source (IRQ2 and IRQ3) is interrupt control level 0 (no priority)

- IRQ Status Registers (ISR) Number of bits: 8 Address: H'FFFEEB

Bit	Bit Name	Setting	R/W	Descriptions
3	IRQ3F	0	R/W	[Setting condition] • When the interrupt source selected by the ISCR registers occurs [Clearing conditions] • When reading 1, then writing 0 • When interrupt exception handling is executed when low-level detection is set and $\overline{\text{IRQ3}}$ or $\overline{\text{ExIRQ3}}$ input is high • When IRQ3 interrupt exception handling is executed when falling-edge, rising-edge, or both-edge detection is set

- IRQ Sense Control Register L (ISCRL) Number of bits: 8 Address: H'FFFEED

Bit	Bit Name	Setting	R/W	Descriptions
7	IRQ3SCB	0	R/W	IRQ3 Sense Control B
6	IRQ3SCA	1	R/W	IRQ3 Sense Control A 01: Interrupt request generated at falling edge of $\overline{\text{IRQ3}}$ or $\overline{\text{ExIRQ3}}$ input

- DTC Enable Register A (DTCERA) Number of bits: 8 Address: H'FFFEEE

DTCER specifies DTC activation interrupt sources. DTCER is comprised of five registers: DTCERA to DTCERF. For DTCE bit setting, use bit manipulation instructions such as BSET and BCLR. Multiple DTC activation sources can be set at one time (only at the initial setting) by masking all interrupts and writing data after executing a dummy read on the relevant register.

Bit	Bit Name	Setting	R/W	Descriptions
4	DTCEA4	1	R/W	DTC Activation Enable Setting this bit to 1 specifies a relevant interrupt source as a DTC activation source. [Clearing conditions] • When data transfer has ended with the DISEL bit in MRB set to 1 • When the specified number of transfers have ended These bits are not cleared when the DISEL bit is 0 and the specified number of transfers have not been completed

- IRQ Sense Port Select Register (ISSR) Number of bits: 8 Address: H'FFFEFD

Bit	Bit Name	Setting	R/W	Descriptions
3	ISS3	1	R/W	1: PA3/$\overline{\text{ExIRQ3}}$ is selected

- Standby Control Register (SBYCR) Number of bits: 8 Address: H'FFFF84

Bit	Bit Name	Setting	R/W	Descriptions
2	SCK2	0	R/W	System Clock Select 2 to 0
1	SCK1	0	R/W	Select a clock for the bus master in high-speed mode or medium-speed mode.
0	SCK0	0	R/W	000: High-speed mode

- Low-Power Control Register (LPWRCR) Number of bits: 8 Address: H'FFFF85

Bit	Bit Name	Setting	R/W	Descriptions
4	EXCLE	0	R/W	Subclock Input Enable Enables/disables subclock input from the EXCL pin. 0: Disables subclock input from the EXCL pin

- Module Stop Control Registers H (MSTPCRH) Number of bits: 8 Address: H'FFFF86

Bit	Bit Name	Setting	R/W	Descriptions
6	MSTP14	0	R/W	Data transfer controller (DTC)
5	MSTP13	1	R/W	16-bit free-running timer (FRT)
4	MSTP12	1	R/W	8-bit timers (TMR_0, TMR_1)
3	MSTP11	1	R/W	14-bit PWM timer (PWMX)
1	MSTP9	1	R/W	A/D converter
0	MSTP8	1	R/W	8-bit timers (TMR_X, TMR_Y)

- Port A Data Direction Register (PADDR) Number of bits: 8 Address: H'FFFFAB

Bit	Bit Name	Setting	R/W	Descriptions
7	PA7DDR	0	W	When set to 1, the corresponding pins function as output port pins; when cleared to 0, function as input port pins. As the address of this register is the same as that of PAPIN, reading from this register indicates the state of port A.
6	PA6DDR	0	W	
5	PA5DDR	0	W	
4	PA4DDR	0	W	
3	PA3DDR	0	W	
2	PA2DDR	0	W	
1	PA1DDR	0	W	
0	PA0DDR	0	W	

- IRQ Enable Register (IER) Number of bits: 8 Address: H'FFFFC2

Bit	Bit Name	Setting	R/W	Descriptions
3	IRQ3E	1	R/W	IRQ3 Enable The IRQ3 interrupt request is enabled when this bit is 1.

- System Control Register (SYSCR) Number of bits: 8 Address: H'FFFFC4

Bit	Bit Name	Setting	R/W	Descriptions
5	INTM1	0	R	These bits select the control mode of the interrupt controller. 00: Interrupt control mode 0
4	INTM0	0	R/W	

- DTC Mode Register A (MRA) Number of bits: 8 (Cannot be directly accessed by the CPU)

Bit	Bit Name	Setting	R/W	Descriptions
7	SM1	1	—	Source Address Mode 1 and 0 These bits specify an SAR operation after a data transfer. 10: SAR is incremented after a transfer (by +1 when Sz = 0, by +2 when Sz = 1)
6	SM0	0	—	
5	DM1	1	—	Destination Address Mode 1 and 0 These bits specify a DAR operation after a data transfer. 10: DAR is incremented after a transfer (by +1 when Sz = 0, by +2 when Sz = 1)
4	DM0	0	—	
3	MD1	1	—	DTC Mode These bits specify the DTC transfer mode. 10: Block transfer mode
2	MD0	0	—	
1	DTS	0	—	DTC Transfer Mode Select Specifies whether the source side or the destination side is set to be a repeat area or block area in repeat mode or block transfer mode. 0: Destination side is repeat area or block area
0	Sz	0	—	DTC Data Transfer Size Specifies the size of data to be transferred. 0: Byte-size transfer

- DTC Mode Register B (MRB) Number of bits: 8, (Cannot be directly accessed by the CPU)

Bit	Bit Name	Setting	R/W	Descriptions
7	CHNE	0	—	DTC Chain Transfer Enable When this bit is set to 1, a chain transfer will be performed. n data transfer with CHNE set to 1, determination of the end of the specified number of data transfers, clearing of the interrupt source flag, and clearing of DTCER are not performed.
6	DISEL	0	—	DTC Interrupt Select When this bit is set to 1, a CPU interrupt request is generated every time data transfer ends. When this bit is cleared to 0, a CPU interrupt request is generated only when the specified number of data transfer ends.

- DTC Source Address Register (SAR) Number of bits: 24, (Cannot be directly accessed by the CPU)
  SAR is a 24-bit register that designates the source address of data to be transferred by the DTC. For word-size transfer, specify an even source address.
  Setting: Start address of array datatable

- DTC Destination Address Register (DAR) Number of bits: 24, (Cannot be directly accessed by the CPU)
  DAR is a 24-bit register that designates the destination address of data to be transferred by the DTC. For word-size transfer, specify an even destination address.
  Setting: Start address of array ramarea

- DTC Transfer Count Register A (CRA) Number of bits: 16, (Cannot be directly accessed by the CPU)
  CRA is a 16-bit register that designates the number of times data is to be transferred by the DTC.
  In block transfer mode, the CRA is divided into two parts; the upper eight bits (CRAH) and the lower 8 bits (CRAL). CRAH holds the number of transfers while CRAL functions as an 8-bit transfer counter (1 to 256). CRAL is decremented by 1 every time data is transferred, and the contents of CRAH are sent when the count reaches H'00.
  Setting: H'8080 (When MRA.Sz = B'0 (specifying byte size transfer) and CRA = H'8080, a data block consists of 128 bytes.)

- DTC Transfer Count Register B (CRB) Number of bits: 16, (Cannot be directly accessed by the CPU)
  CRB is a 16-bit register that designates the number of times data is to be transferred by the DTC in block transfer mode. It functions as a 16-bit transfer counter (1 to 65536) that is decremented by 1 every time data is transferred, and transfer ends when the count reaches H'0000.
  Setting: H'0001

(5) Flowchart

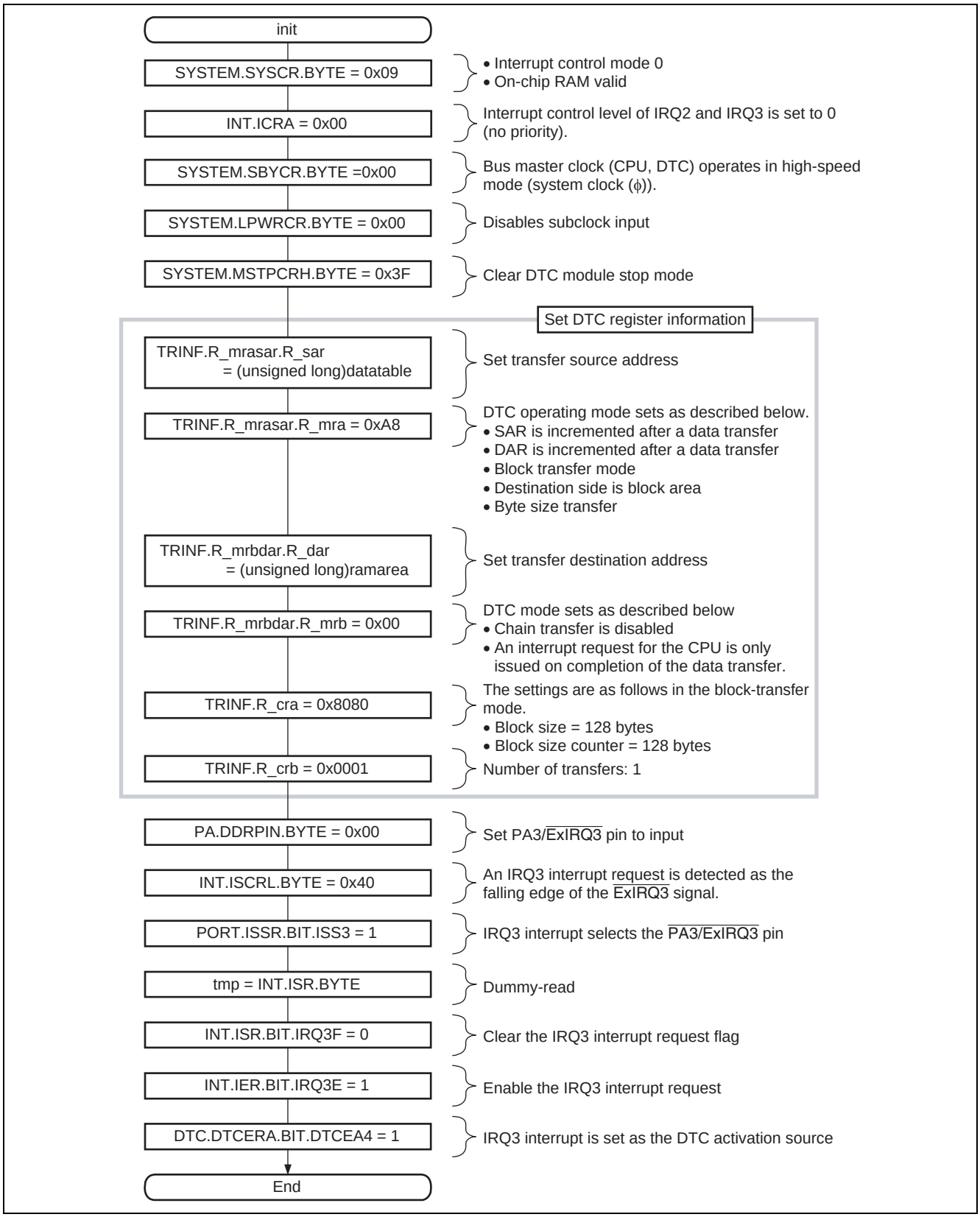


Figure 9 Flowchart

5.6.4 INT_IRQ3 Function

(1) Functional overview

The IRQ3 interrupt processing routine disables the IRQ3 interrupt request, and stores the result of verifying the data transferred by the DTC in the on-chip RAM (dtcend).

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below.

Note that the setting values shown are those used in this application note and differ from the initial values.

- IRQ Enable Registers (IER) Number of bits: 8 Address: H'FFFFC2

Bit	Bit Name	Setting	R/W	Descriptions
3	IRQ3E	0	R/W	IRQ3 Enable The IRQ3 interrupt request is enabled when this bit is 1.

(5) Flowchart

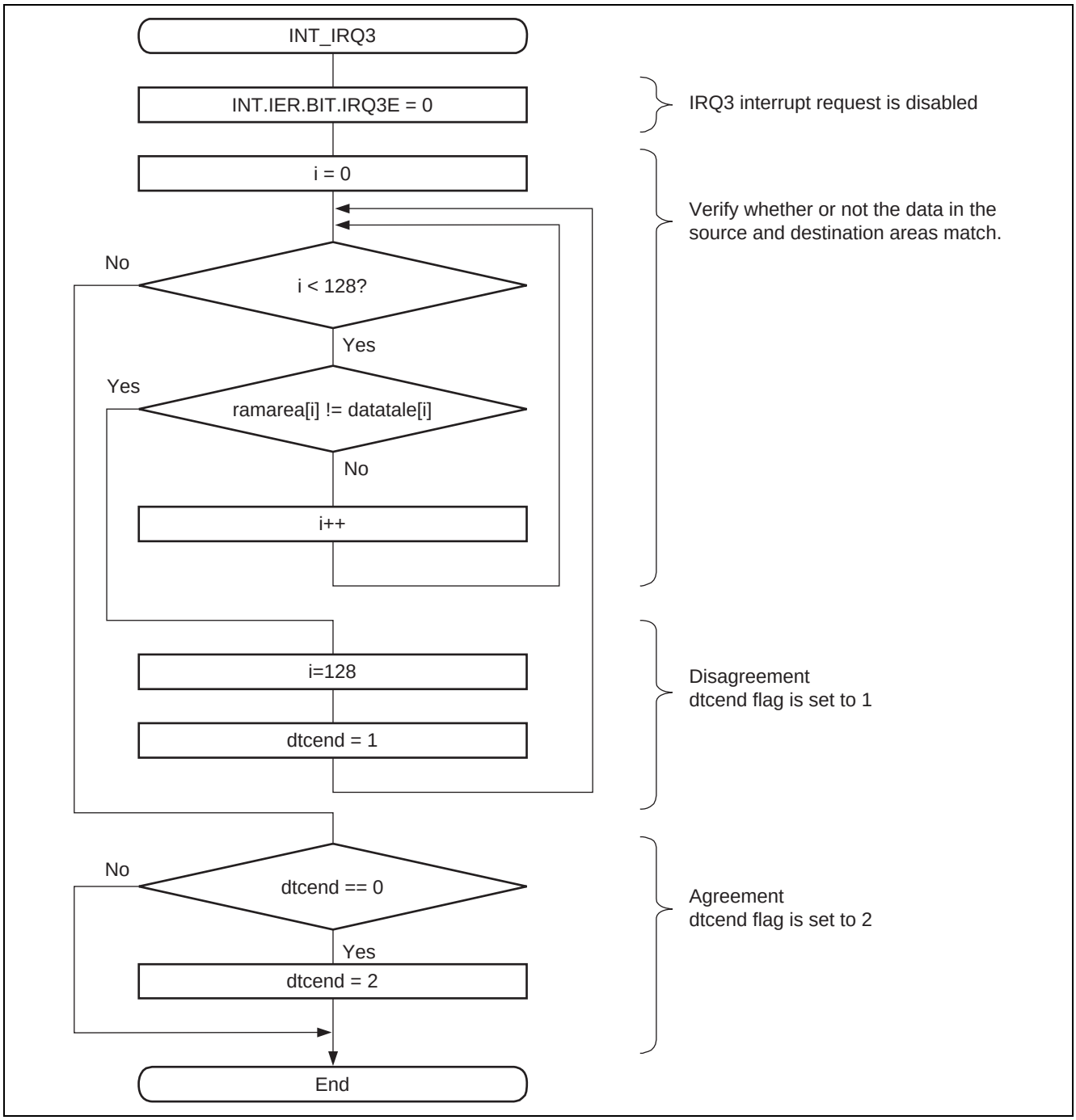


Figure 10 Flowchart

6. Documents for Reference

- Hardware Manual
  H8S/2472, H8S/2463, H8S/2462 Group Hardware Manual (REJ09B0403)
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package Ver.7.00 User's Manual (REJ10J2039)
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Technical News/Technical Updates
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