How to Design Bidirectional LVDS

Abstract

This application note explains how to connect two LVDS pairs (TX1-RX1 and TX2-RX2) to transfer data using the Renesas SLG47920/21 bidirectionally.

This application note comes complete with design files which can be found in section 9 References.

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1. Introduction

The Renesas SLG47920/21 supports six LVDS capable GPIOs (three true-LVDS pairs up to 100 Mbps). GPIOs with LVDS capability are comprised of a CMOS IO structure with 4 mA drive strength and with LVDS Tx/Rx cells. Since LVDS is differential and requires two lines, a pair of GPIOs are connected to the same LVDS Tx/Rx.

The structure of the pair of GPIO with LVDS capability is shown in Figure 1.

Each pair of GPIOs can be used as two independent CMOS GPIOs or can be used as a single LVDS differential line transceiver pair.

The following configuration options are available for each CMOS GPIO pin:

- Input
  - Simple CMOS input
- Push-pull output with single drive strength
  - 4 mA.

Also, two pull-up options are available (selected by ***Pull-Up Enable***):

- No pull-up
- 1x pull-up.

For GPIO pairs in LVDS mode (selected by the ***Enable*** option of the LVDS Pair element in the software), the following configurations are available:

- LVDS Tx (selected by ***Tx Vod Selection***)
  - Selectable VOD: 250 mV (typ), tunable range up to 390 mV
- LVDS Rx (fail-safe input) (selected by ***Rx Fail Safe Enable***).

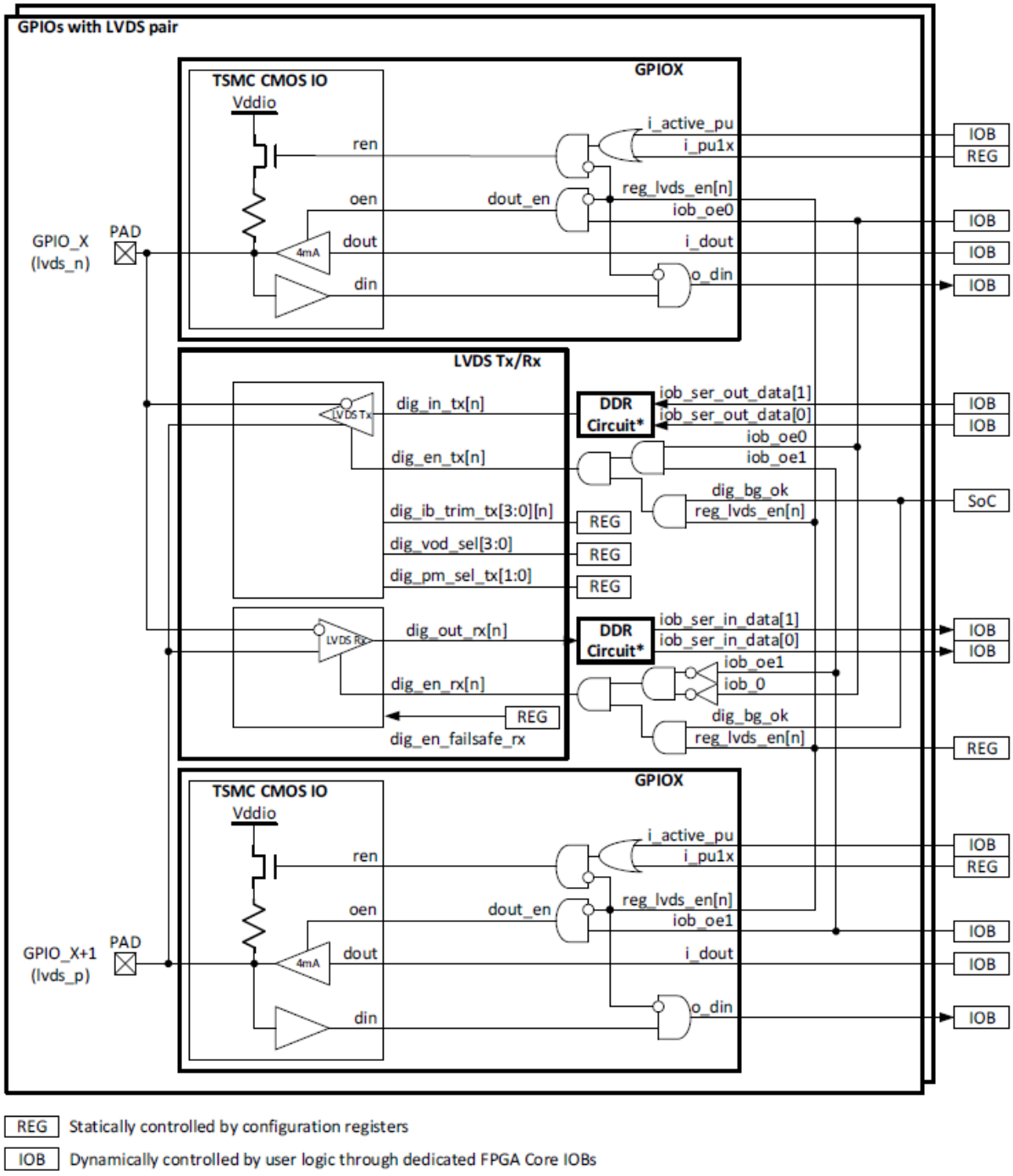

Figure 1. GPIOs Pair with LVDS Capability

LVDS Direction Controls

Whenever LVDS mode is enabled, the CMOS IO structure will force OE into a disabled state. LVDS Tx/Rx enable considers the controls of both GPIOs used when used as an LVDS pair.

GPIOs in LVDS mode allow bidirectional operation. However, setup time (T_{TX_SU} and T_{RX_SU}) is required to switch between Tx and Rx as shown in Figure 2.

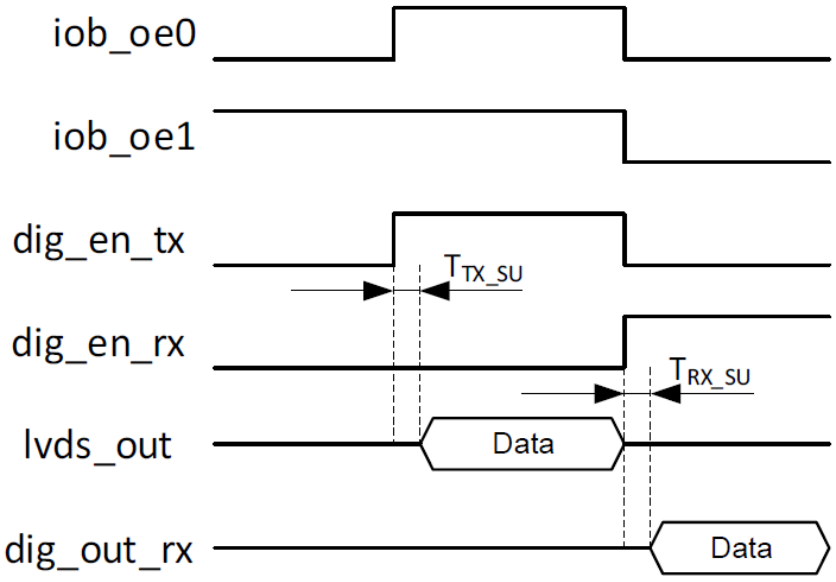

Figure 2. LVDS Bidirectional Operation

Table 1 lists the GPIOs in the SLG47920/21 and their respective LVDS Channels.

Table 1. LVDS Channels

Signal Name	Pin Function
GPIO18	LVDS Channel 0 OUT_N/IN_N
GPIO19	LVDS Channel 0 OUT_P/IN_P
GPIO20	LVDS Channel 1 OUT_N/IN_N
GPIO21	LVDS Channel 1 OUT_P/IN_P
GPIO22	LVDS Channel 2 OUT_N/IN_N
GPIO23	LVDS Channel 2 OUT_P/IN_P

In this application note, data is transferred between two setups (two boards) connecting the Txn and Rxn of the LVDS pair. LVDS Channel 1 and Channel 2 are used for this application.

Setup A and Setup B are connected to one another through cable wires connected between the LVDS PMOD header (see Figure 7).

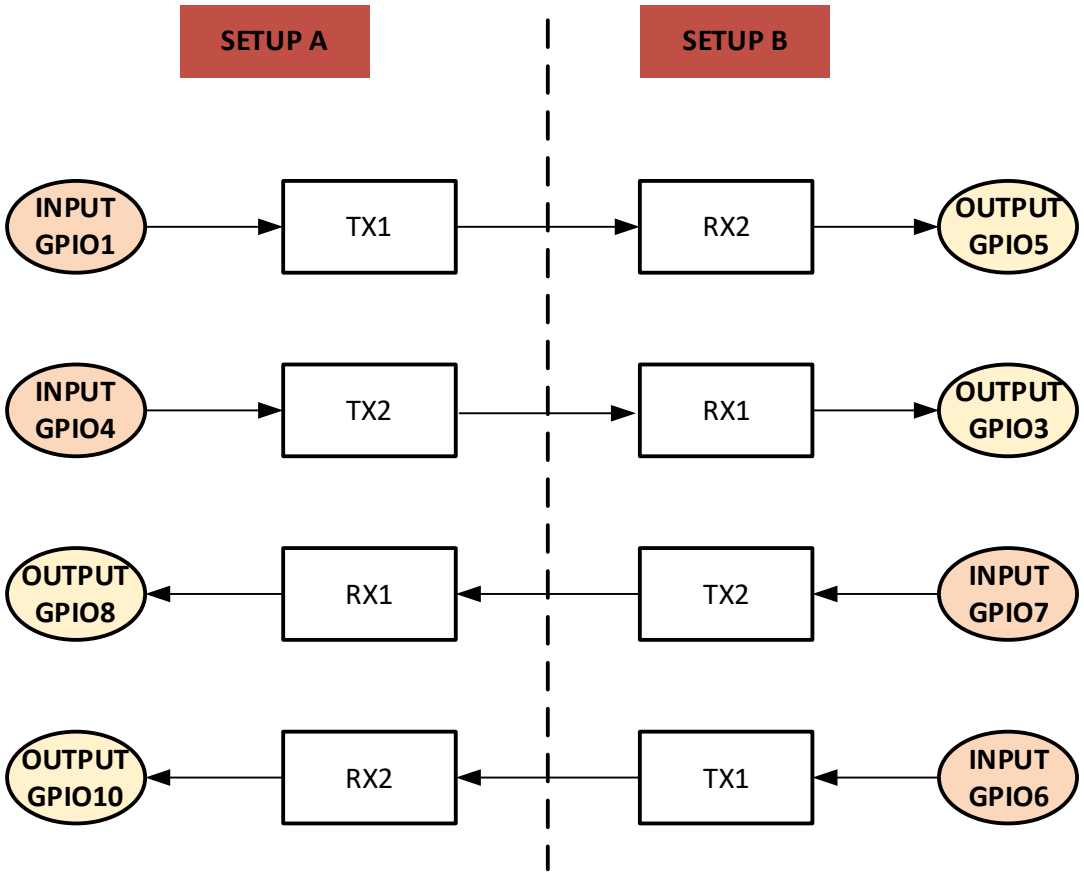

Figure 3. Bidirectional Connects between LVDS Channels

A common output enable (OE) signal is used to facilitate the input and output functions of the GPIO. GPIO2 of both the setups (boards) are connected with a wire.

2. Requirements

- SLG47921/20V device
- Two FPGA Deluxe Development Boards with USB cable and power supply
- Two FPGA Socket Adaptor Boards
- Connecting Wires
- Latest Revision of the ForgeFPGA Workshop software.

3. Verilog Code

The Verilog code for setup A is shown below. It contains the complete design for LVDS channels 1 and 2 for data transfer on setup A.

The links to download the design files for both Setup A and Setup B from the website are available in section 9 References.

```
/* we have two cases :
    OE = 1 ( handled externally)
    TX1 is used to transmitting and RX2 is used for receiving

 2. OE = 0 ( handled externally)
    TX2 is used to transmitting and RX1 is used for receiving

    ** connect LVDS pair 1 in one setup to LVDS pair 2 in another setup */

(* top *) module lvds_bidir_S1(
//tx1
  (* iopad_external_pin *) input        i_tx1_data,         // declare input port
for data from gpio 1
  (* iopad_external_pin *) output       o_lvds_tx1_data,     // declare output port
for data to lvds
  (* iopad_external_pin *) output [1:0] o_lvds_data_tx1_oe,  // declare output port
for
 //rx1
  (* iopad_external_pin *) input        i_lvds_rx1_data,    // receive data from rx
  (* iopad_external_pin *) output       o_rx1_data,         // observe data from rx
on gpio
  (* iopad_external_pin *) output       o_rx1_data_oe,      // OE for gpio

//rx2
  (* iopad_external_pin *) output [1:0] o_lvds_data_rx2_oe, // for rx OE
  (* iopad_external_pin *) input        i_lvds_rx2_data,    // receive data from rx
  (* iopad_external_pin *) output       o_rx2_data,         // observe data from rx
on gpio
  (* iopad_external_pin *) output       o_rx2_data_oe,      // OE for gpio
//tx2
  (* iopad_external_pin *) input        i_tx2_data,         // declare input port
for data from gpio 4
  (* iopad_external_pin *) output       o_lvds_tx2_data,    // declare output port
for data to lvds

  (* iopad_external_pin *) input        i_oe                // signal OE to assign
to tx and rx from gpio 2

);

  // The OE (output enable) is used to define whether the GPIO operates as an
output or an input
  // assign OE = 1 to function as an output
  // assign OE = 0 to function as an input. If not mentioned, then the default
value is 0
  // LVDS channel requires assign OE = 2'b11 to function as LVDS TX
  // LVDS channel 6equires assign OE = 2'b00 to function as LVDS RX

    assign o_lvds_data_tx1_oe =  {i_oe,i_oe} ;  // for tx to output data 2'b11
    assign o_lvds_data_rx2_oe = {~i_oe,~i_oe};  // for rx 2'b00

 // for rx to input data
```

```
    assign o_rx1_data_oe = 1;                   // for gpio to read rx data lvds pair 1
    assign o_rx2_data_oe = 1;                   // for gpio to read rx data lvds pair 2

// for lvds1 TX1 and RX1
    assign o_lvds_tx1_data = i_tx1_data;        // gpio data to lvds1
    assign o_rx1_data = i_lvds_rx1_data;        // lvds2 rx to gpio

// for lvds2 TX2 and RX2
    assign o_rx2_data = i_lvds_rx2_data;        // observe rx data on gpio
    assign o_lvds_tx2_data = i_tx2_data;        // gpio data to lvds2

endmodule
```

4. Floorplan

Figure 4. Floorplan for Setup A and Setup B

Figure 4 shows how LVDS Channel 1 and LVDS Channel 2 is being used in the Floorplan Tab of the software. The view can be zoomed in/out using the controls at the bottom or by pressing CTRL + Scroll on the mouse.

5. Design Steps

1. Launch the latest version of the Go Configure Software Hub. Select the SLG47921V device and the ForgeFPGA Workshop software will load.
2. Download the design example files (AN-FG-029 LVDS_BiDir_S1.ffpga and AN-FG-029 LVDS_BiDir_S2.ffpga) listed in section 9 References.
3. Open the files after downloading.
4. Open the FPGA editor and review the Verilog code. The top module names are *lvds_bidir_S1 and lvds_bidir_S2* which cover the operation of the LVDS pair and their connections for bidirectional data transfer.
5. Open the IO planner tab on the FPGA Editor and review the pin assignments. Verify the LVDS Channel 1 and Channel 2 signal placements (see Figure 5). Verify the same for Setup B.
6. Next click the Synthesize button on the lower left side of the FPGA Editor.
7. Click the Generate Bitstream button on the lower left side of the FPGA Editor. Check the Logger and Issues tabs to make sure that the Bitstream was generated correctly.
8. Now click on the Floorplan tab and see the CLB utilization (Figure 4). Press the Ctrl + scroll the mouse wheel to zoom-in. Confirm that the IOs selected in the IO Planner are shown in the Floorplan.

FUNCTION	DIRECTION	PORT	DESCRIPTION
LVDS_PAIR2_SER_OUT_DATA[0]	Output	o_lvds_tx2_data	LVDS Pair2: Serial Out Data 0 (rise edge when DDR)
LVDS_PAIR1_SER_OUT_DATA[0]	Output	o_lvds_tx1_data	LVDS Pair1: Serial Out Data 0 (rise edge when DDR)
LVDS_PAIR2_SER_IN_DATA[0]	Input	i_lvds_rx2_data	LVDS Pair2: Serial In Data 0 (rise edge or raw data)
LVDS_PAIR1_SER_IN_DATA[0]	Input	i_lvds_rx1_data	LVDS Pair1: Serial In Data 0 (rise edge or raw data)

Figure 5. IO Planner

9. In the Forge Workshop main window, click on LVDS Pair 1 and enable it from the properties panel on the left. Follow the same steps for LVDS Pair 2. Ensure that the same is done on Setup B (see Figure 6).

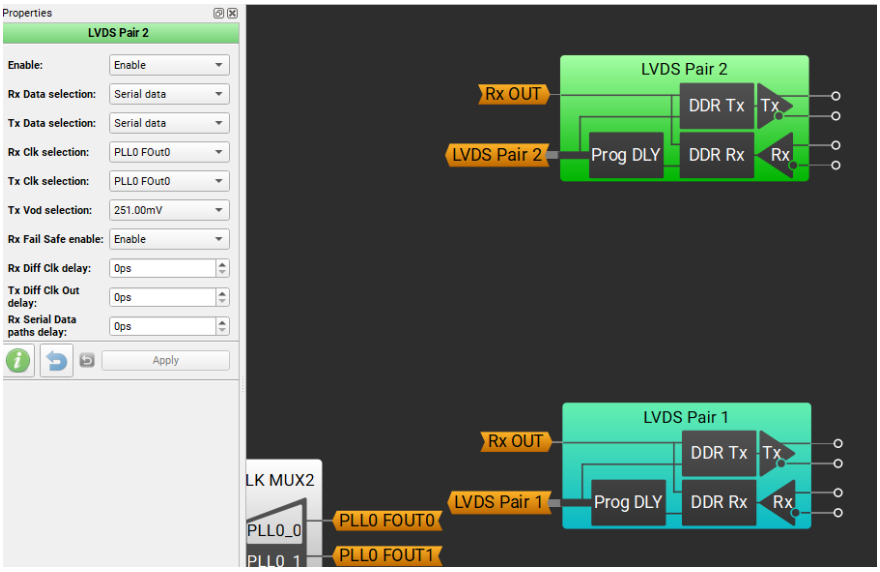

Figure 6. LVDS Properties

10. Connect the Synchronous Logic Generator to GP1O1 and GPIO4 and assign a signal as Txn data
11. Assign a button at GPIO2 to control the GPIOs inputs and outputs for data transfer (Tx and Rx). GPIO2 must also be connected to both Setup A and Setup B with a wire (see Figure 7 for setup).
12. Additionally, verify that both setups are connected through cable wires through the LVDS PMOD Header.
13. Connect the oscilloscope to GPIO 5 and GPIO 3 on Setup A to read waveforms from Setup B. Similarly, connect oscilloscope probes to GPIO10 and GPIO 8 in Setup B to read waveforms from Setup A.

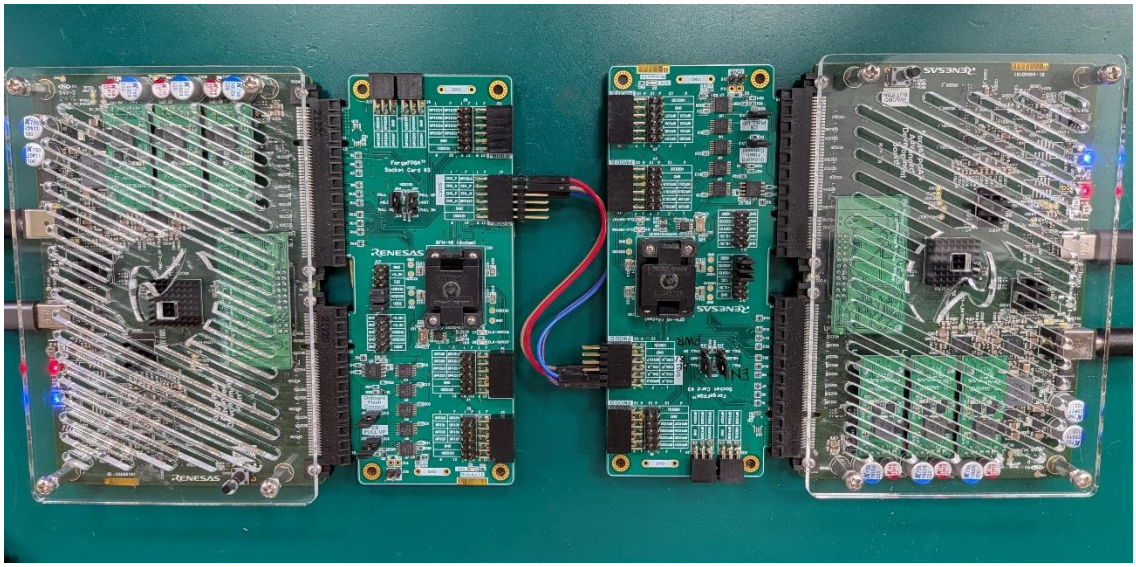

Figure 7. Connection between Setup A and Setup B

6. Results

Case I. Setup A, when OE = 0 (GPIO 2): Tx2 is applied on GPIO 4 (purple), and GPIOs 20 and 21 receive data from Setup B and is displayed on GPIO 3 (green) Rx1.

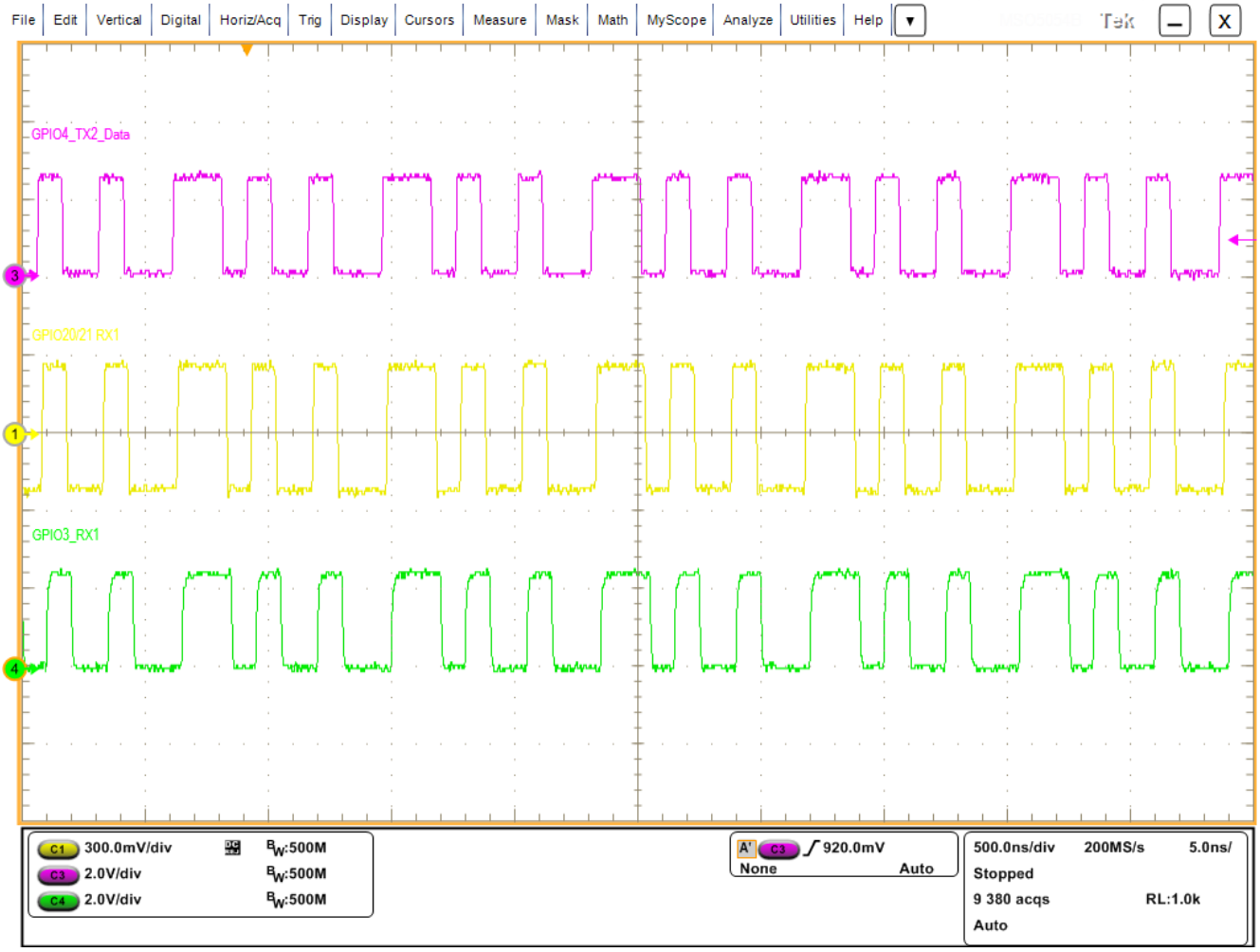

Figure 8. Setup A with OE = 0

Case II. Setup A when OE = 1 (GPIO 2): Tx1 is applied on GPIO 1 (purple) and data received from Setup B (Tx1) is displayed on GPIO 5 Rx2 (green).

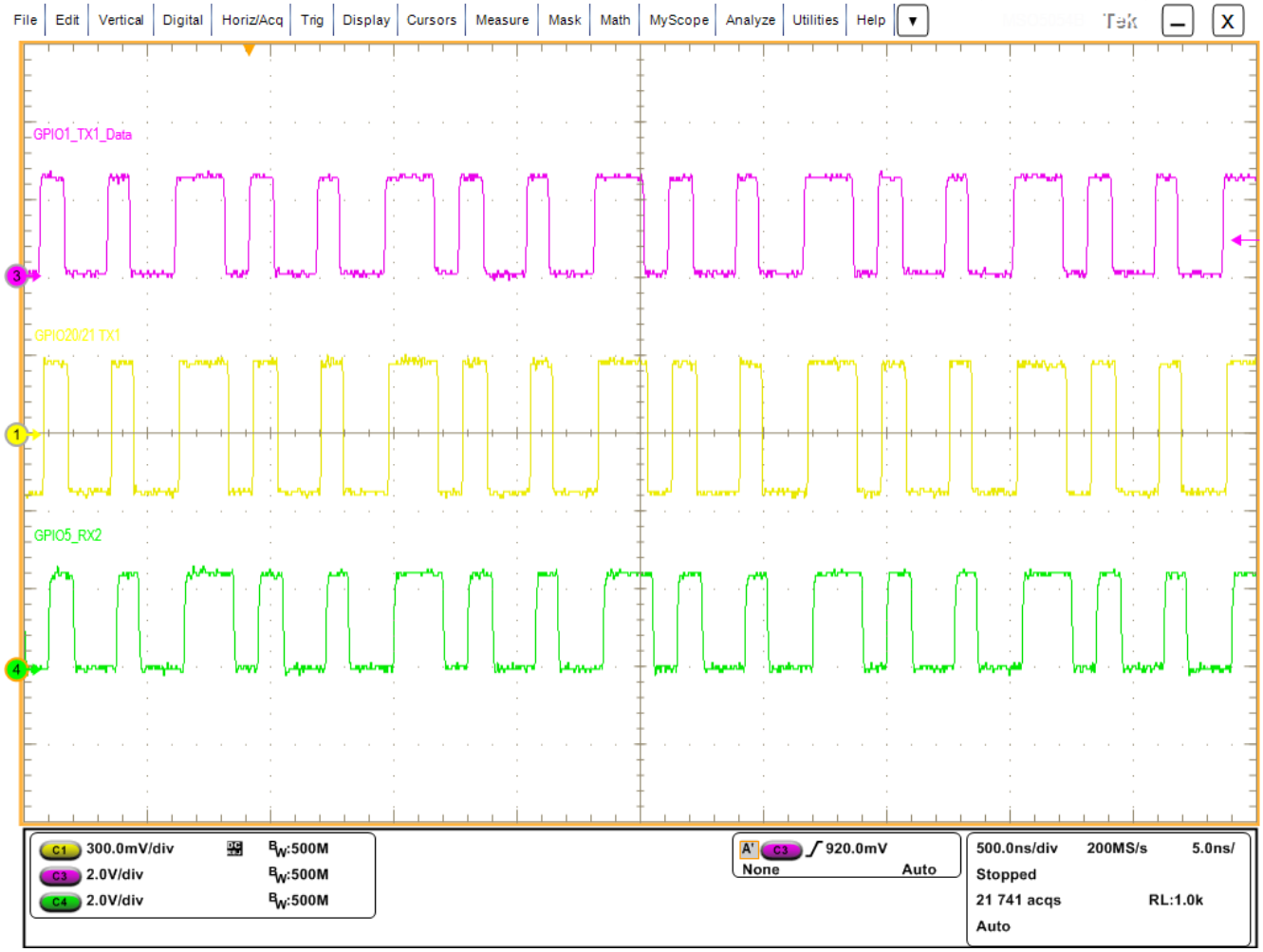

Figure 9. Setup A with OE = 1

Case III. Setup B when OE = 0 (GPIO 2): Tx2 is applied on GPIO 7 (purple) and GPIOs 20 and 21 receive data from Setup A and is displayed on GPIO 8 Rx1 (green).

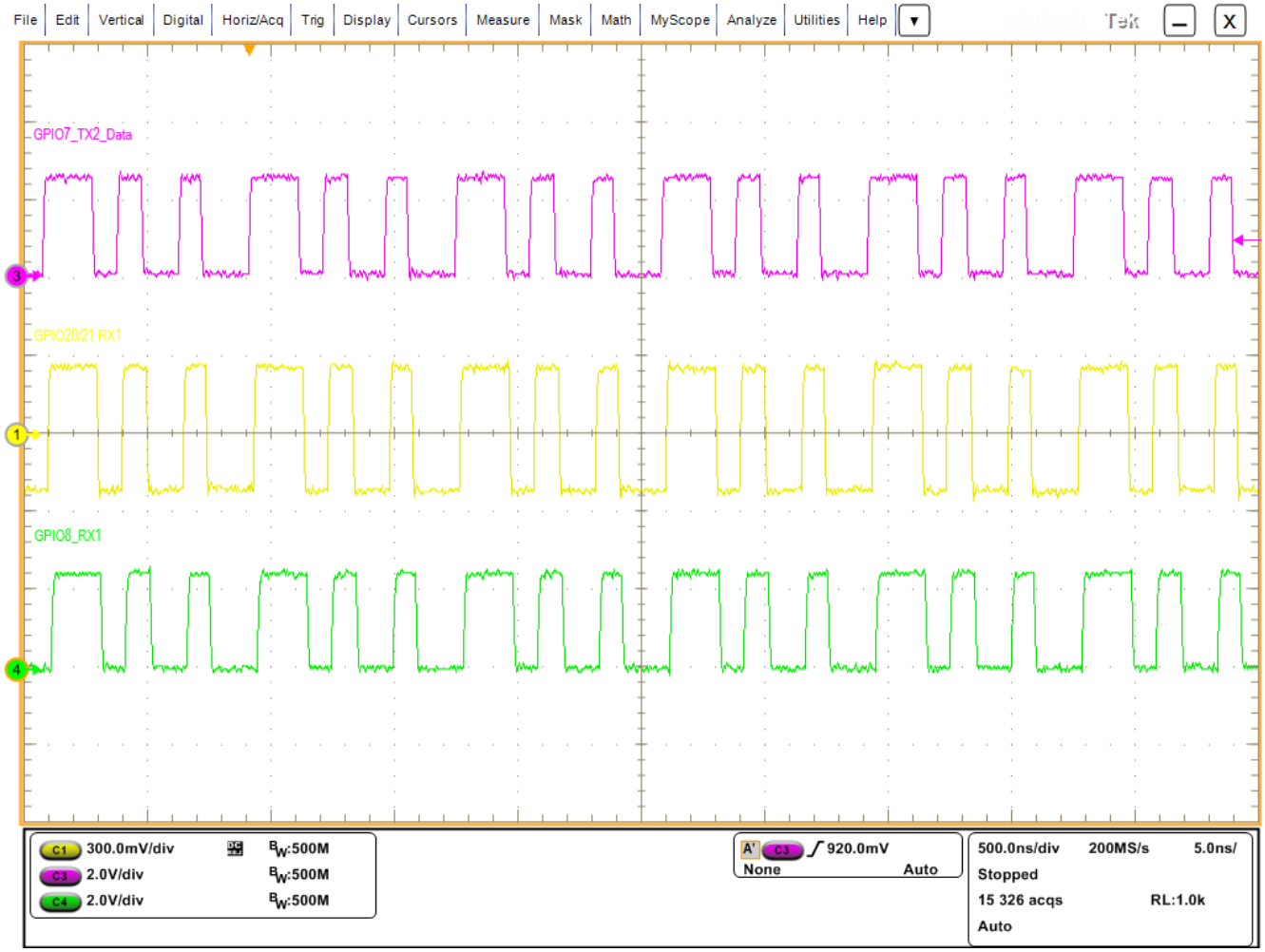

Figure 10. Setup B with OE = 0

Case IV. Setup B when OE = 1 (GPIO 2). Tx1 is applied on GPIO 6 (purple) and data received from Setup B (Tx1) is displayed on GPIO 10 Rx2 (green).

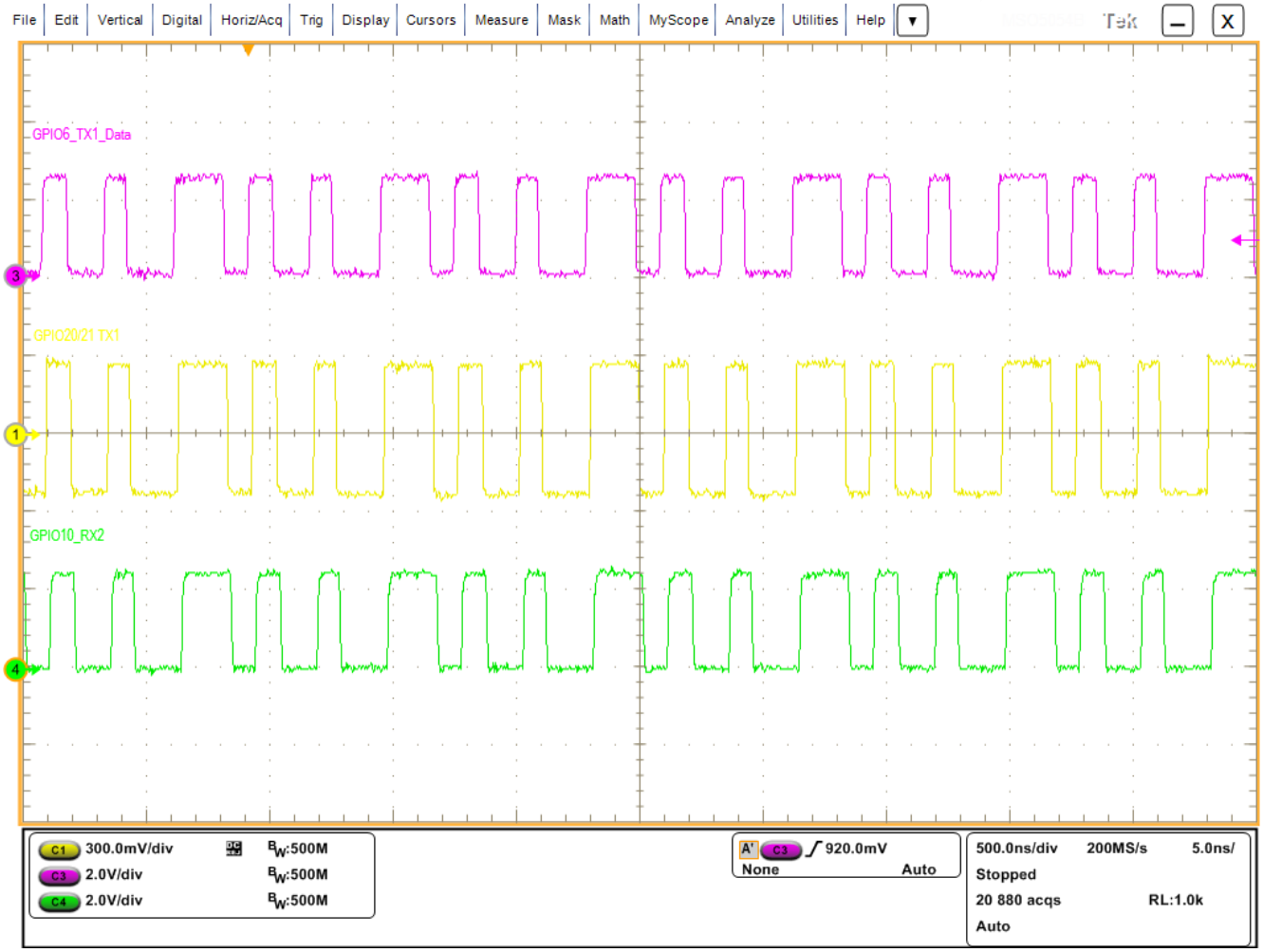

Figure 11. Setup B with OE = 1

7. Conclusion

This application note focuses on how to use the Renesas SLG47920/21 to send and receive data between two setups through LVDS Channels. Supporting waveforms can be found in this AN for more information. The two design files for Setup A and Setup B is available for download in section 9 References.

If interested, please contact the ForgeFPGA Business Support Team.

8. Terms and Definitions

CLB	Configuration Logic Block
HDL Editor	Workspace where Verilog code is entered
FPGA	Field Programmable Gate Array
FPGA Editor	Main FPGA design and simulation window
Go Configure Software Hub	Main window for device selection
ForgeFPGA Window	Main FPGA project window for debug and IO programming
OSC	Oscillator
LVDS	Low Voltage Differential Signaling

9. References

For related documents and software, please visit ForgeFPGA. Download our free ForgeFPGA™ Designer software [1] to open the. ffpga files [2] [3] and view the proposed circuit design.

[1] Go Configure Software Hub, Software Download and User Guide

[2] AN-FG-029 How_to_design_bidirectional_LVDS_S1.ffpga, ForgeFPGA Design File

[3] AN-FG-029 How_to_design_bidirectional_LVDS_S2.ffpga, ForgeFPGA Design File

[4] ForgeFPGA SLG47920/21, Datasheet, Renesas Electronics

[5] ForgeFPGA Workshop User Guide, Renesas Electronics

10. Revision History

Revision	Date	Description
1.00	Jan 13, 2026	Initial release