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H8/300L Super Low Power 系列

多倍精度 2 进制数的加法

要点

进行多倍精度 2 进制数的加法运算，并将加法结果保存到被加数的数据存储器。

动作确认器件

H8/38024

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1. 参数

	内容	保存位置	数据长度 (字节)
输入	加法数据的字节数	R0L	1
	被加数的起始地址	R3	2
	加数的起始地址	R4	2
输出	加法结果的起始地址	R3	2
	有无错误	Z 标志 (CCR)	—
	有无进位	C 标志 (CCR)	—

2. 内部寄存器变化和标志变化

R0		R1	
x	x	x	x
R2		R3	
x	x	○	
R4		R5	
x		x	
R6		R7	
•		•	

I	U	H	U
•	•	•	•
N	Z	V	C
x	○	x	○

•: 不变, x: 不定, ○: 结果

3. 程序设计

程序存储器 (字节)	42
数据存储器 (字节)	0
堆栈 (字节)	0
时钟周期数	7170
重入	可
再定位	可
中途中断	可

4. 注意事项

规格的时钟周期数是进行了 255 字节+255 字节运算时的值。

5. 说明

5.1 功能

(1) 参数的详细内容如下：

R0L：输入参数，用 2 位 16 进制数设定被加数和加数的字节数。

R3：设定被加数数据存储区的起始地址。

执行软件 ADD2 后，设定加法结果的起始地址。

R4：输入参数，设定加数数据存储区的起始地址。

Z 标志 (CCR)：输出参数，表示数据长度的设定错误。

Z 标志=0：表示数据的字节数 (R0L) 不是“0”。

Z 标志=1：表示数据的字节数 (R0L) 是“0”，为错误。

C 标志 (CCR)：输出参数，表示软件 ADD2 执行后有无进位。

C 标志=0：表示加法结果没有产生进位。

C 标志=1：表示加法结果产生进位 (参照图 17-2)。

(2) 软件 ADD2 的执行例子如图 17-1 所示。

一旦如①设定输入参数，就如②将加法结果设定到数据存储区。

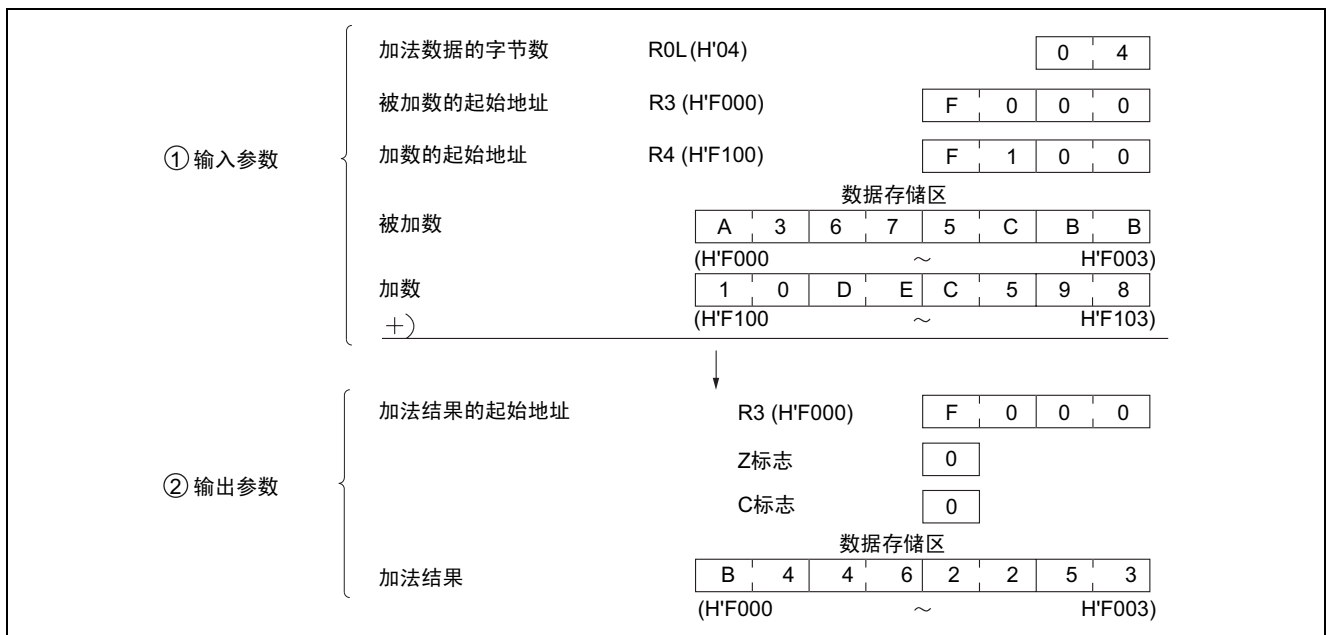


图 17-1 软件 ADD2 的执行例子

产生进位时的加法例子如图 17-2 所示。

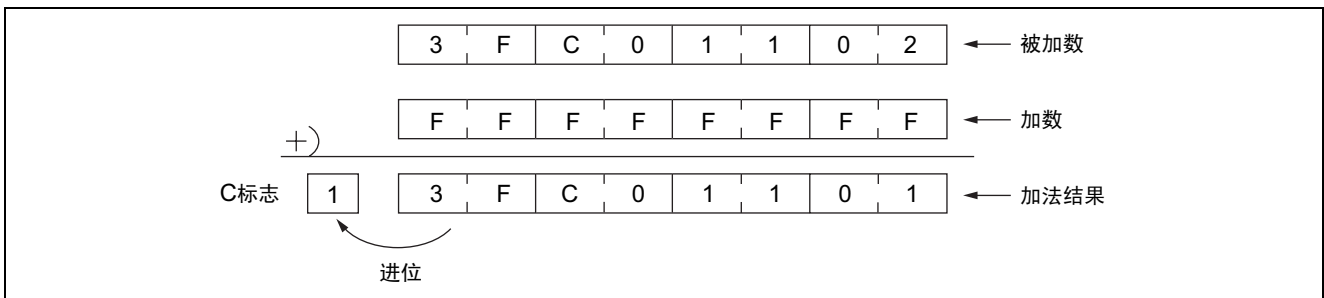


图 17-2 产生进位时的加法例子

5.2 使用时的注意

(1) 如图 17-3，如果不使用高位，就必须将不使用的位置“0”。

软件 ADD2 以 1 个字节为单位进行加法运算，如果不置“0”，因为进行含有被设定在高位的不定数据的加法运算，所以就得不到正确的加法结果。

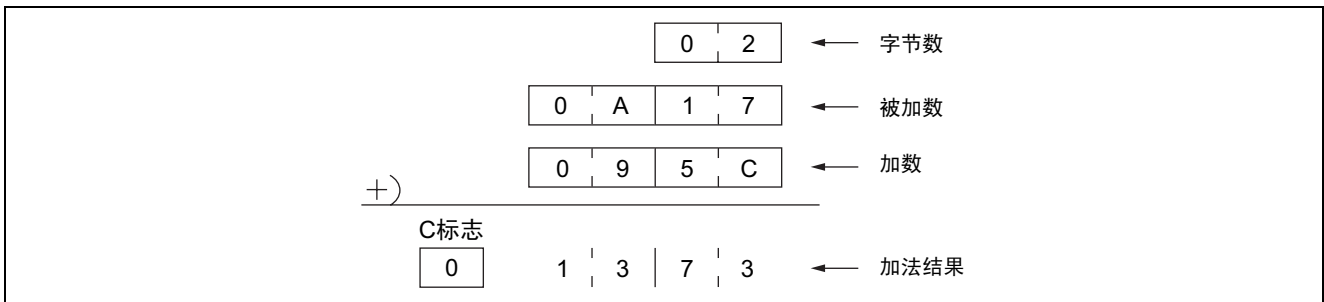


图 17-3 不使用高位的加法例子

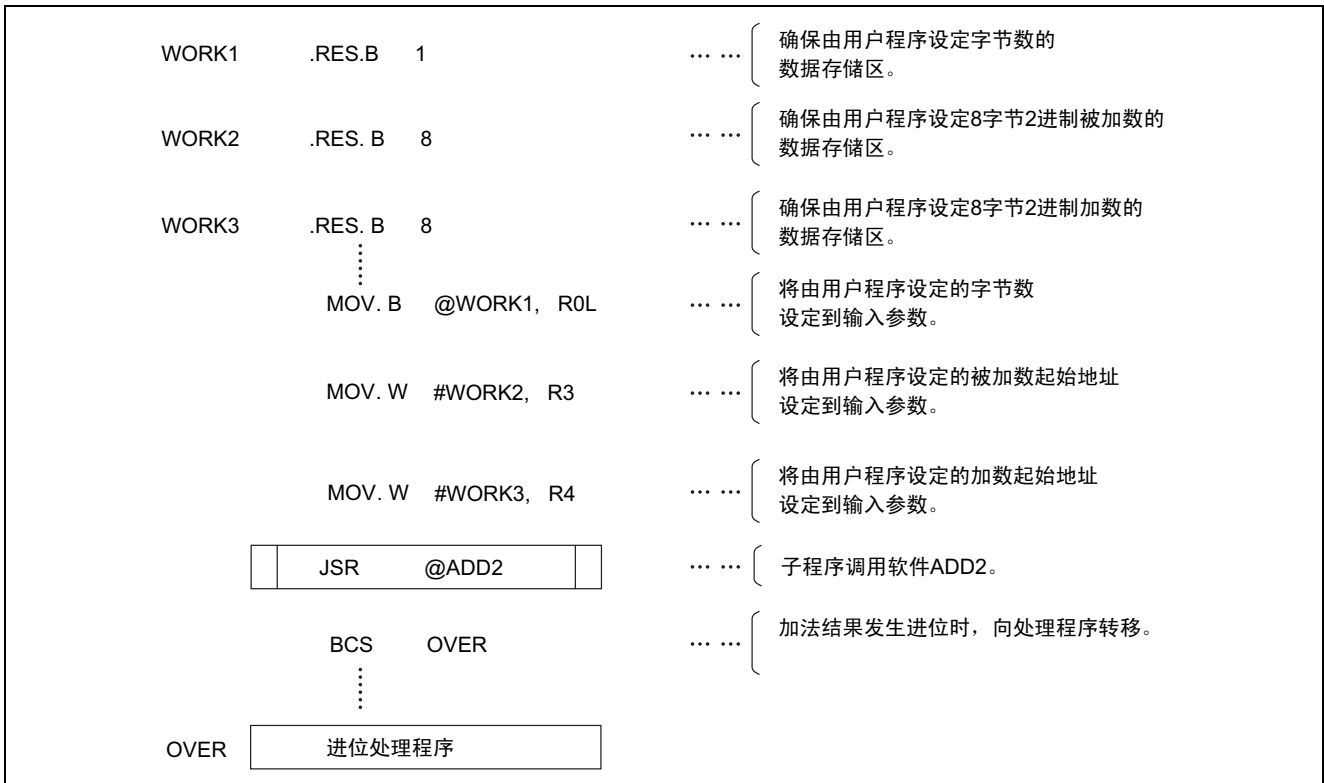
(2) 因为执行软件 ADD2 后加法结果被设定到被加数的数据存储区，所以将破坏被加数。如果执行后还需要被加数，就必须预先保存到存储器。

5.3 数据存储器的说明

软件 ADD2 不使用数据存储器。

5.4 使用例

下图表示加法数据为 8 个字节的使用例，将加法数据的字节数、保存被加数和加数的起始地址设定到寄存器，子程序调用软件 ADD2。



5.5 工作原理

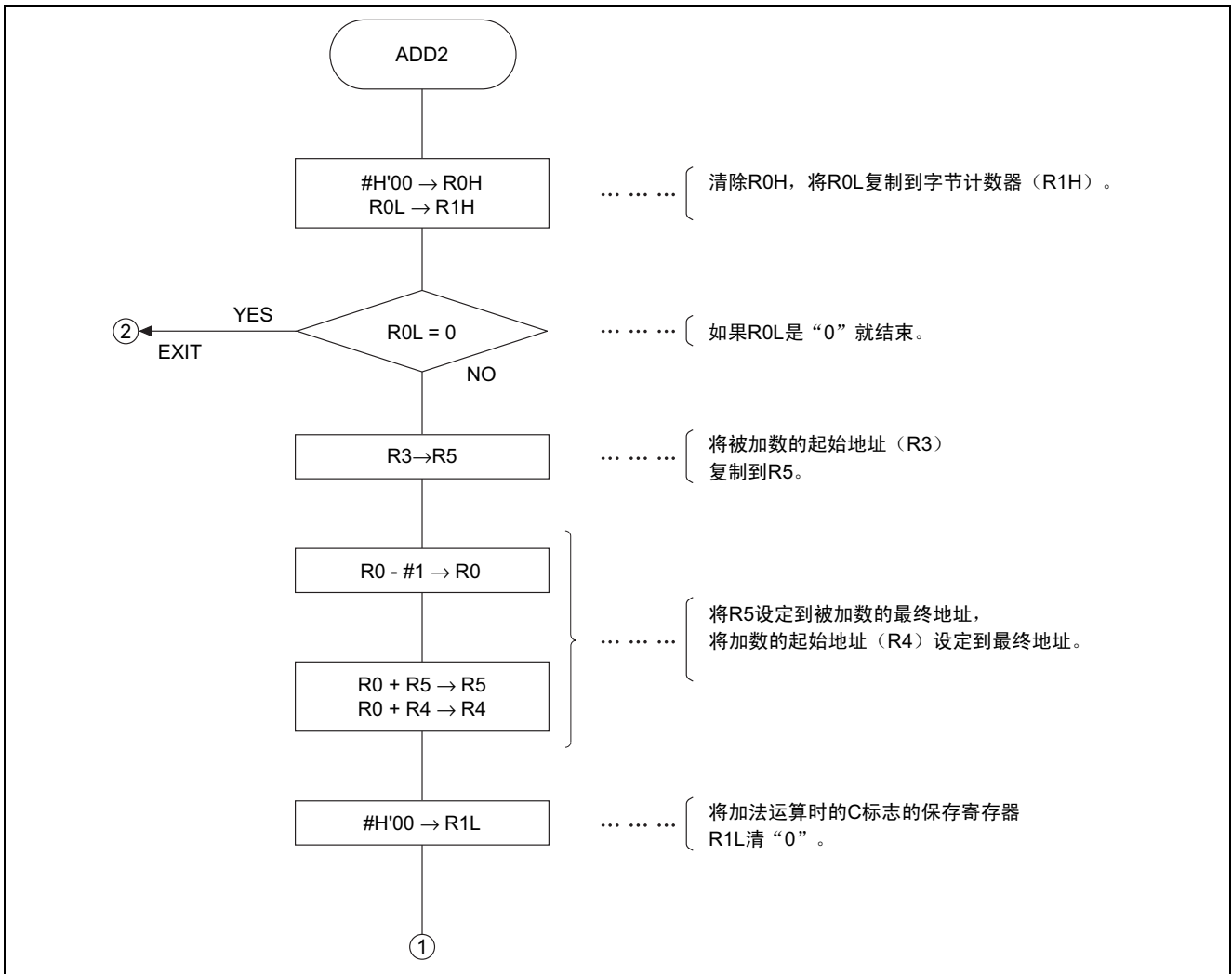
- (1) 因为在多倍精度 2 进制数加法中，以 1 个字节为单位保存被加数和加数的数据，所以能通过重复进行带进位标志的加法运算（ADDX.B 指令）实现。
- (2) 将被加数数据存储区的最后地址设定到 R3、加数数据存储区的最后地址设定到 R4。
- (3) 清除保存 C 标志的 R1L。
- (4) 从被加数和加数的最后字节开始，以 1 个字节为单位分别将数据装入到 R2L 和 R2H，执行（式 1）。

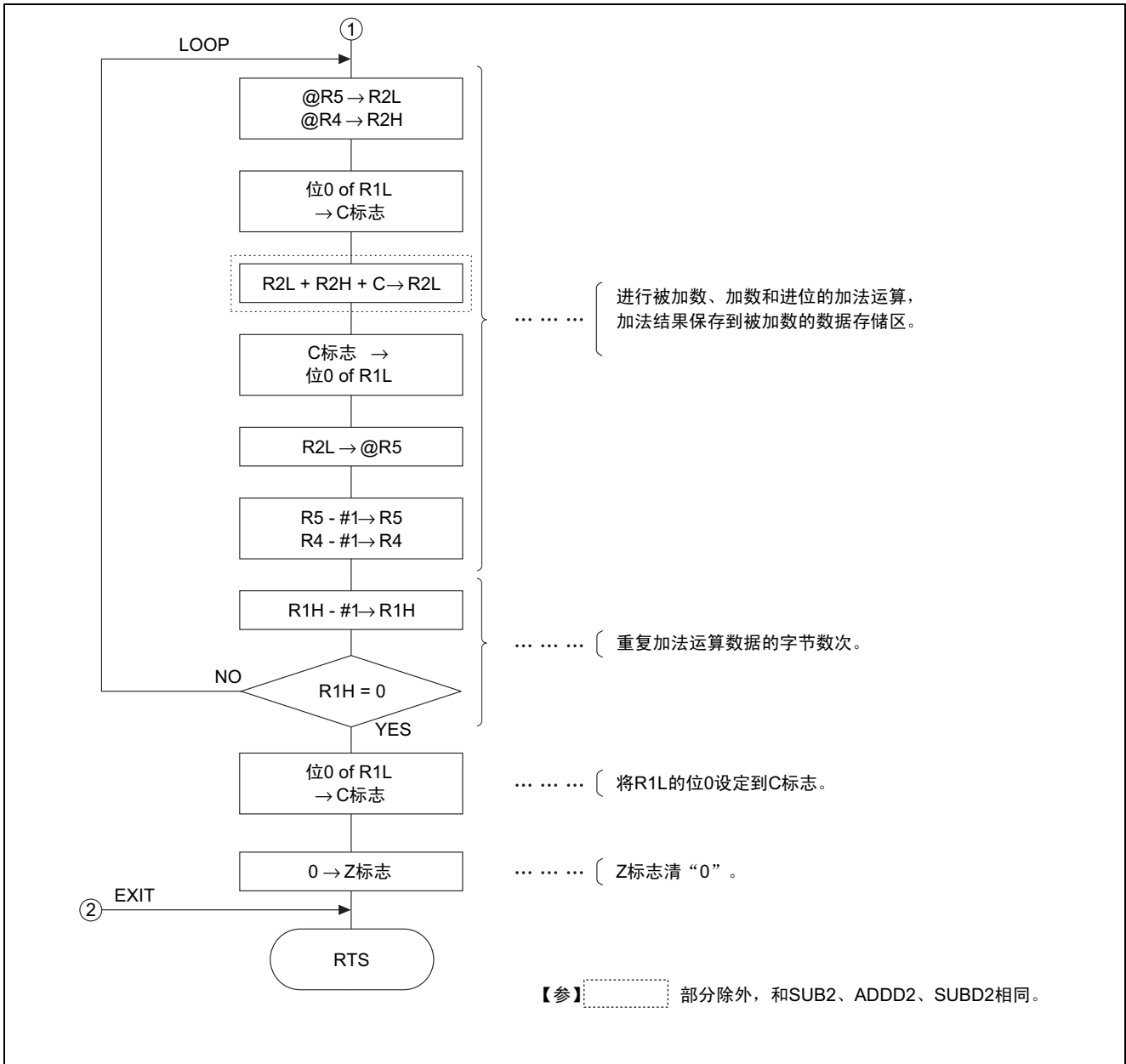
$$\left. \begin{array}{l} \text{被加数} + \text{加数} + C \rightarrow R2L \\ R2L \rightarrow @R3 \end{array} \right\} \dots \dots \dots \text{ (式1)}$$

在此，C 标志是由低位的加法结果所产生的进位。

- (5) 将(4)的加法结果保存到被加数的数据存储区。
- (6) 每次结束(4)和(5)时，R3、R4 和 R0L 递减，直到 R0L 为“0”重复此处理。

6. 流程图





7. 程序清单

```

*** H8/300 ASSEMBLER   VER 1.0B ** 08/18/92 09:59:33
PROGRAM NAME =
1                               ;*****
2                               ;*
3                               ;*   00 - NAME           :MULTIPLE PRECISION BINARY ADDITION
4                               ;*                               (ADD2)
5                               ;*
6                               ;*****
7                               ;*
8                               ;*   ENTRY           :R0L       (BYTE LENGTH OF ADDTION DATA)
9                               ;*                               R3       (START ADDRESS OF SUMMAND)
10                              ;*                               R4       (START ADDRESS OF ADDEND)
11                              ;*
12                              ;*   RETURNS          :R3       (START ADDRESS OF RESULT)
13                              ;*                               Z flag OF CCR (Z=0;TRUE , Z=1;FALSE)
14                              ;*                               C flag OF CCR (C=0;TRUE , C=1;OVER FLOW)
15                              ;*
16                              ;*****
17                              ;
18 ADD2_cod C 0000              .SECTION   ADD2_code, CODE, ALIGN=2
19                              .EXPORT    ADD2
20                              ;
21 ADD2_cod C 00000000 ADD2 .EQU    $           ;Entry point
22 ADD2_cod C 0000 F000        MOV.B   #H'00,R0H      ;Clear R0H
23 ADD2_cod C 0002 0C81        MOV.B   R0L,R1H      ;Set byte counter(R1H)
24 ADD2_cod C 0004 4722        BEQ     EXIT        ;Branch if R0L=0
25 ADD2_cod C 0006 0D35        MOV.W   R3,R5       ;R3 -> R5
26 ADD2_cod C 0008            MAIN
27 ADD2_cod C 0008 1B00        SUBS.W  #1,R0       ;Decrement R0
28 ADD2_cod C 000A 0905        ADD.W   R0,R5       ;Set start address of summand(R5)
29 ADD2_cod C 000C 0904        ADD.W   R0,R4       ;Set start address of addend(R4)
30 ADD2_cod C 000E F900        MOV.B   #H'00,R1L   ;Clear R1L
31 ADD2_cod C 0010            LOOP
32 ADD2_cod C 0010 685A        MOV.B   @R5,R2L     ;Load summand to R2L
33 ADD2_cod C 0012 6842        MOV.B   @R4,R2H     ;Load addend to R2H
34 ADD2_cod C 0014 7709        BLD     #0,R1L      ;Load bit 0 of R1L to C flag
35 ADD2_cod C 0016 0E2A        ADDX.B  R2H,R2L     ;Addition
36 ADD2_cod C 0018 6709        BST     #0,R1L      ;Store C flag to bit 0 of R1L
37 ADD2_cod C 001A 68DA        MOV.B   R2L,@R5     ;Store result
38 ADD2_cod C 001C 1B05        SUBS.W  #1,R5       ;Decrement summand address(R5)
39 ADD2_cod C 001E 1B04        SUBS.W  #1,R4       ;Decrement addend address(R4)
40 ADD2_cod C 0020 1A01        DEC.B   R1H         ;Decrement byte counter(R1H)
41 ADD2_cod C 0022 46EC        BNE     LOOP        ;Branch if Z=0
42                              ;
43 ADD2_cod C 0024 7709        BLD     #0,R1L      ;Load bit 0 of R1L to c flag
44 ADD2_cod C 0026 06FB        ANDC.B  #H'FB,CCR    ;Clear Z flag
45 ADD2_cod C 0028            EXIT
46 ADD2_cod C 0028 5470        RTS
47                              ;
48                              .END
****TOTAL ERRORS      0
****TOTAL WARNINGS    0

```

修订记录

Rev.	发行日	修订内容	
		页	修订要点
1.00	2005.07.29	—	初版发行

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