RX Family, H8S Family

H8S to RX Migration Guide: External Bus

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Summary

This application note explains how to migrate between the external bus functions of the RX Family and H8S Family.

Target Devices

- RX Family
- H8S Family

An example of migrating from the H8S Family to the RX Family is presented, with the RX Family represented by the RX231 Group and the H8S Family represented by the H8S/2378 Series. When using this application note with other microcontrollers, appropriate changes should be made to match the specifications of the microcontroller used and thorough evaluation should be performed.

Table Differences in Terminology between RX Family and H8S Family

Item	RX Family	H8S Family
Name of bus clock	BCLK	ϕ
Idle cycle	Recovery cycle	Idle cycle

Contents

1. Points of Difference between External Bus Functions

Table 1.1 Points of Difference between External Bus Functions (RX231 and H8S/2378)

Item	RX (RX231)		H8S (H8S/2378)
Memory size	16 MB (4 areas)		2 MB (8 area)
Bus type	Separate bus/multiplexed bus		Separate bus
Data bus width	8-bit/16-bit		8-bit/16-bit
Data bus width setting	Set in CSn control registers (n = 0 to 3)		Settable by area using bus width control register
Address buses	8 to 24, selectable		8 to 24, selectable*[1]
Chip select output	4		8
Endian setting	Each data area can be set as little-endian or big-endian.		Big-endian
Write access modes*[2]	Byte strobe mode	Pins used: WR0# and WR1#	By the following write signals: $\overline{HWR}$ and $\overline{LWR}$
	Single-write strobe mode	Pins used: BC0#, BC1#, and WR#	
Wait cycles	WAIT# pin		$\overline{WAIT}$ pin
Software wait time	Up to 31 cycles of wait time		Settable at 0 to 7 states by area
Idle cycles (recovery cycles)	Ability to insert up to 15 cycles (selectable among 8 patterns)		Ability to insert idle cycles of up to 2 states each (selectable among 3 patterns)
Page access	Available		Not available
Bus request ($\overline{BREQ}$)	Not available		Request signal asking that bus mastership be released to the external bus master
Bus request acknowledge ($\overline{BACK}$)	Not available		Acknowledge signal indicating that bus mastership was released to the external bus master
Bus request output ($\overline{BREQO}$)	Not available		External bus request signal to allow the internal bus master to access the external address space when the external bus is in the released state

Note 1. The number of usable buses is limited by the operating mode.

Note 2. For details, see 1.1.1, 16-Bit Bus Connection Examples.

1.1 External Bus Connection Examples

1.1.1 16-Bit Bus Connection Examples

Figure 1.1 and Figure 1.2 show examples of connection to external memory with byte selection on the H8S/2378 Series and RX231 Group.

In order to use byte strobe mode on the H8S/2378 Series or RX231 Group it is necessary to connect the read and write strobe signals to the $\overline{\text{WE}}$, $\overline{\text{LB}}$, and $\overline{\text{UB}}$ pins of the of the external memory, and a circuit must be configured for this purpose. On the RX231 Group it is not necessary to connect a circuit between the microcontroller and the external memory when single-write strobe mode is used as the write access mode.

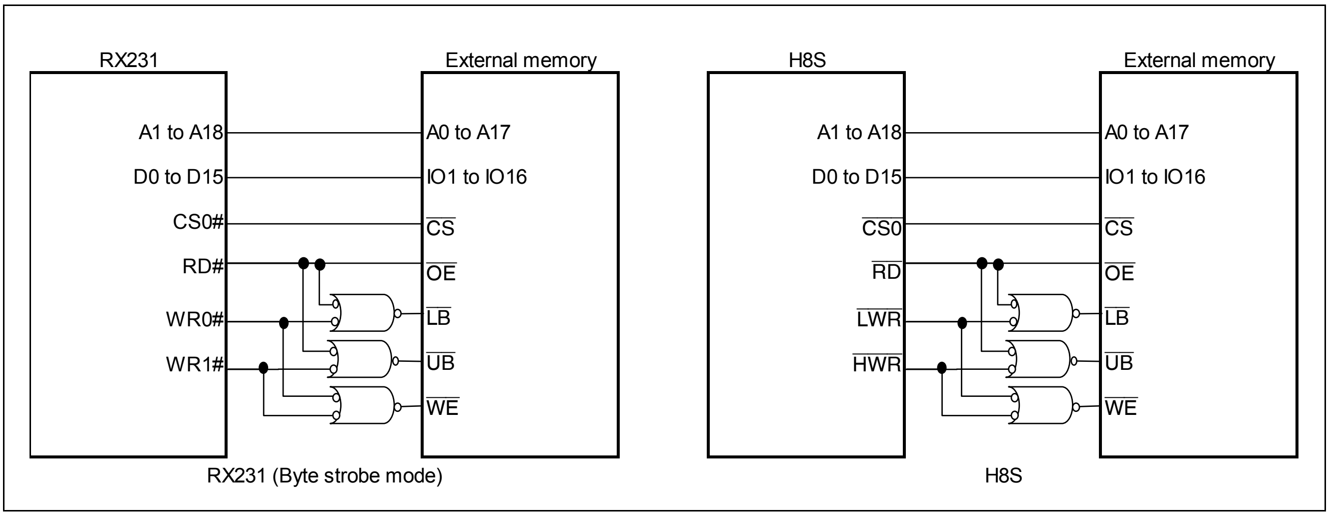


Figure 1.1 H8S/2378 Series and RX231 Group Connection Examples (Byte Strobe Mode)

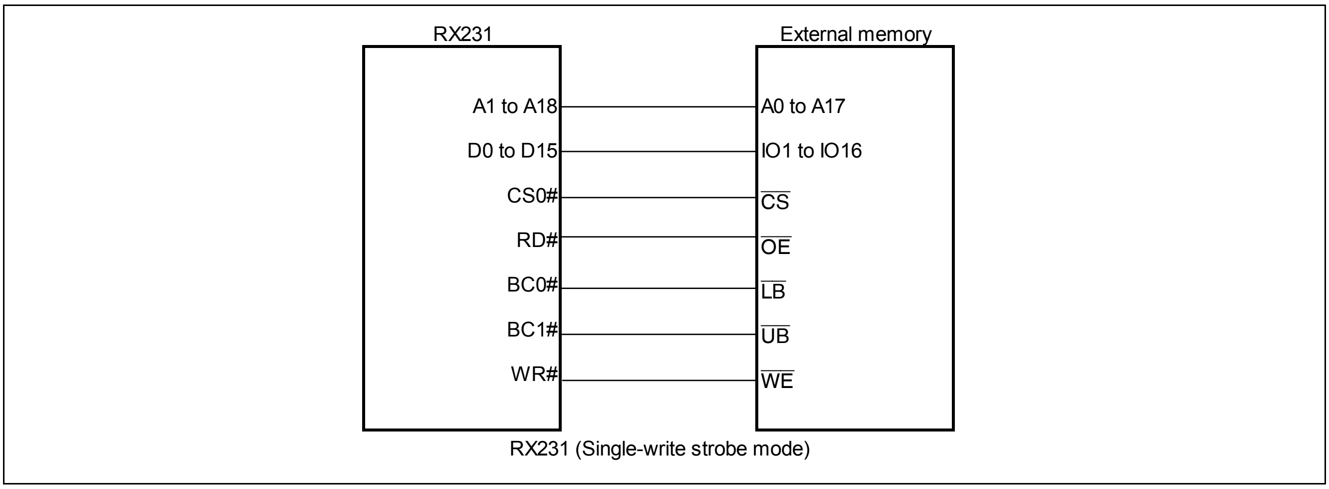


Figure 1.2 RX231 Group Connection Examples (Single-Write Strobe Mode)

1.1.2 8-Bit Bus Connection Examples

Figure 1.3 shows examples of connection via an 8-bit bus on the RX231 Group and H8S/2378 Series. On the RX231 Group the access mode should be set to byte strobe mode. In this case WR0# is enabled during write access. On the H8S/2378 Series $\overline{\text{HWR}}$ is enabled.

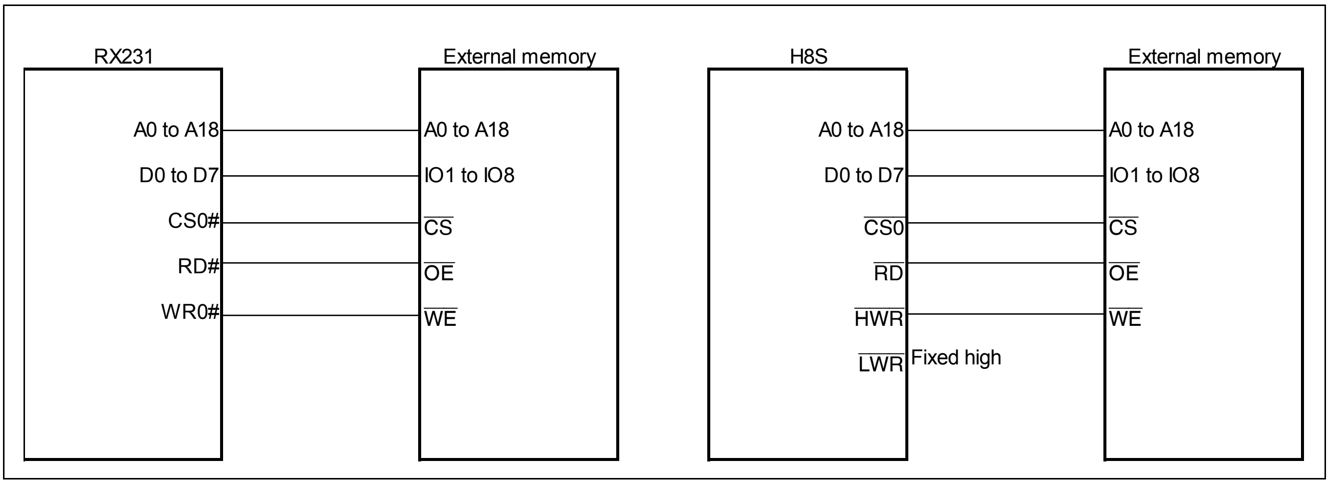


Figure 1.3 8-Bit Bus Connection Examples

1.2 Bus Timing Comparison

The bus timing on the basic bus interface of the H8S/2378 Series and RX231 Group is compared below.

The following example shows 3-state access on the H8S/2378 Series and single-write strobe mode on the RX231 Group. In both cases a 16-bit access space is used, and the big-endian setting is selected on the RX231 Group (the H8S/2378 Series supports big-endian order only). Note that the positions of valid data on the data bus are different when the little-endian setting is selected on the RX231 Group,

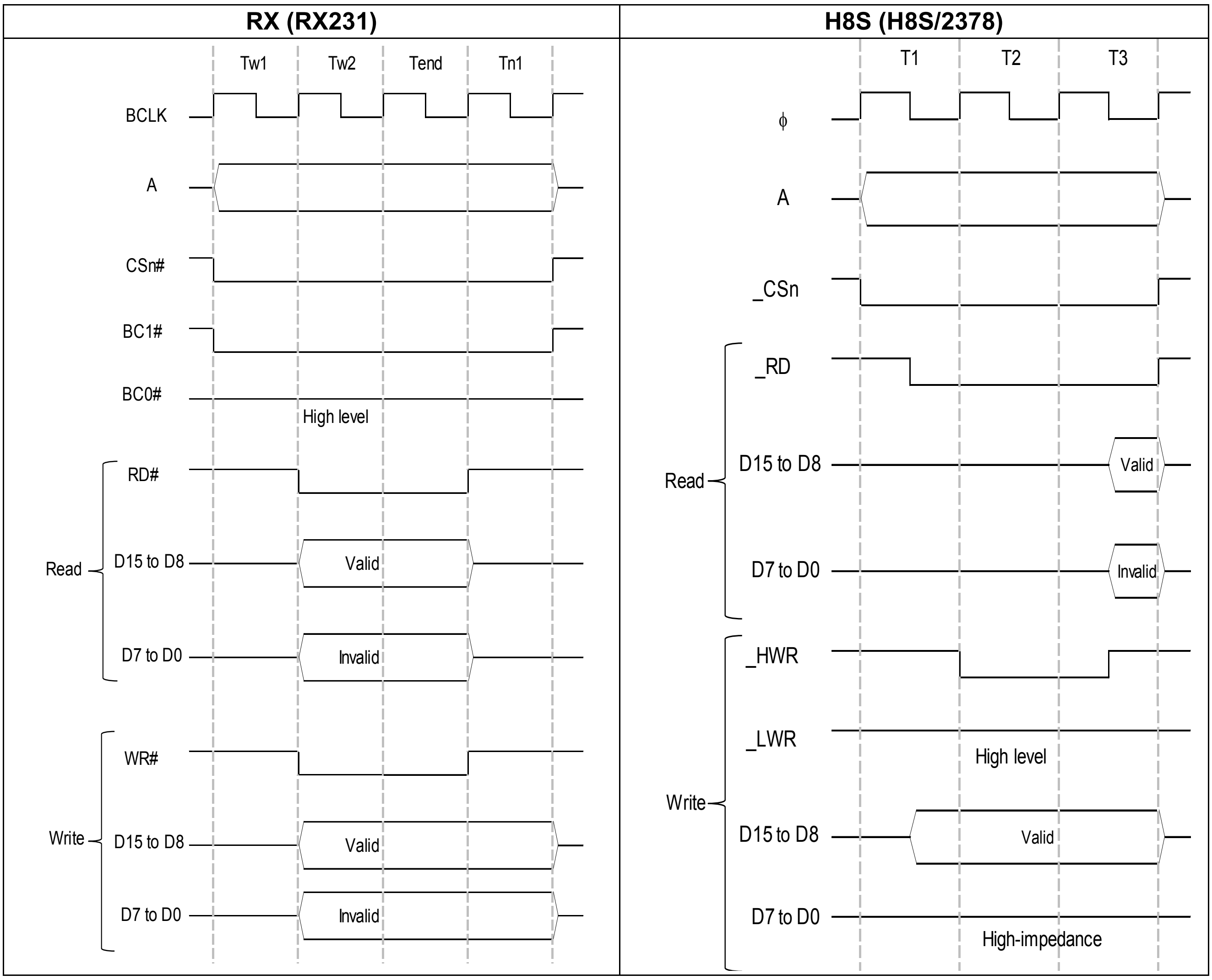


Figure 1.4 Access Timing in 16-Bit Access Space (Even-Number Addresses, Byte Access)

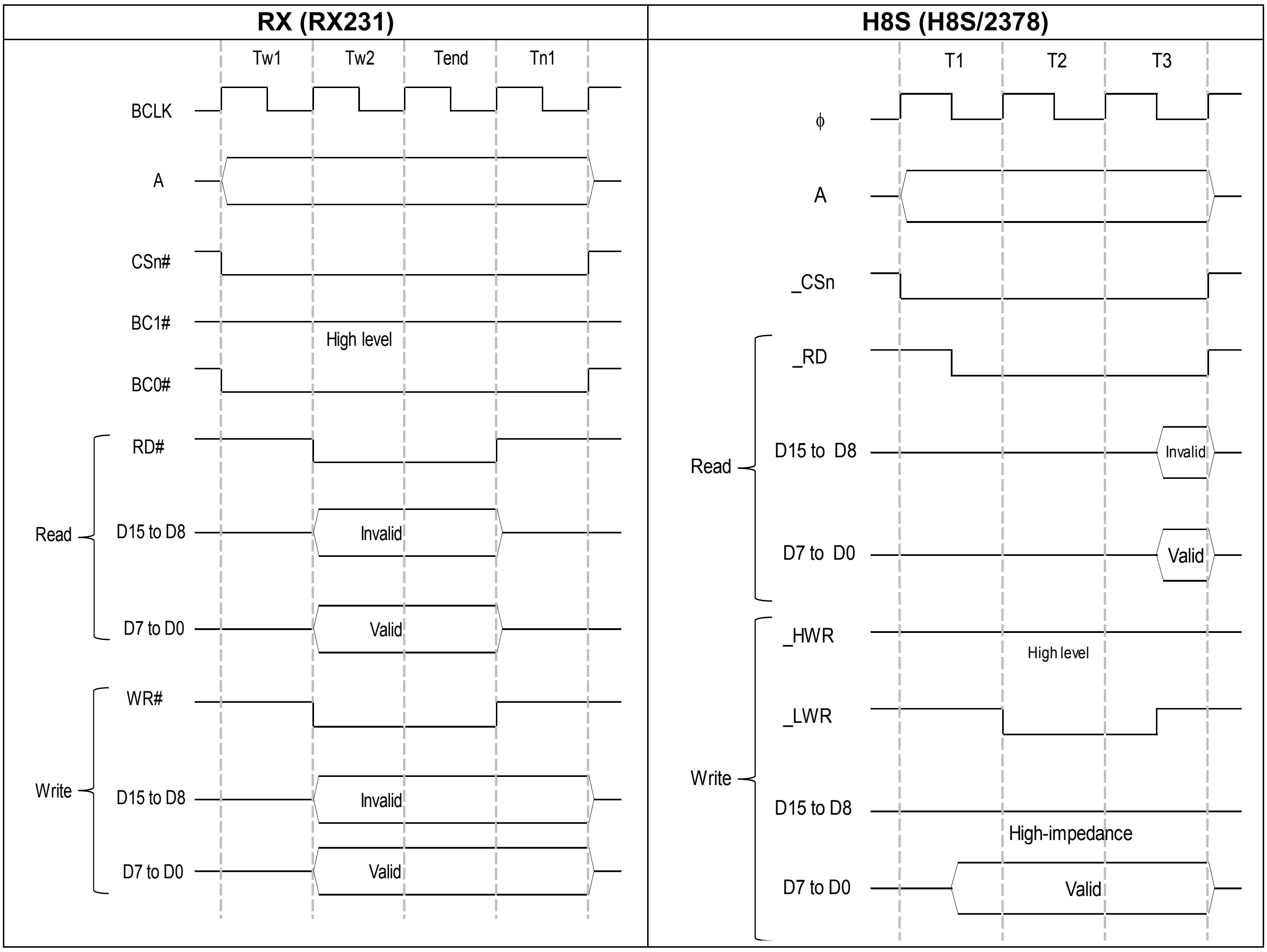


Figure 1.5 Access Timing in 16-Bit Access Space (Odd-Number Addresses, Byte Access)

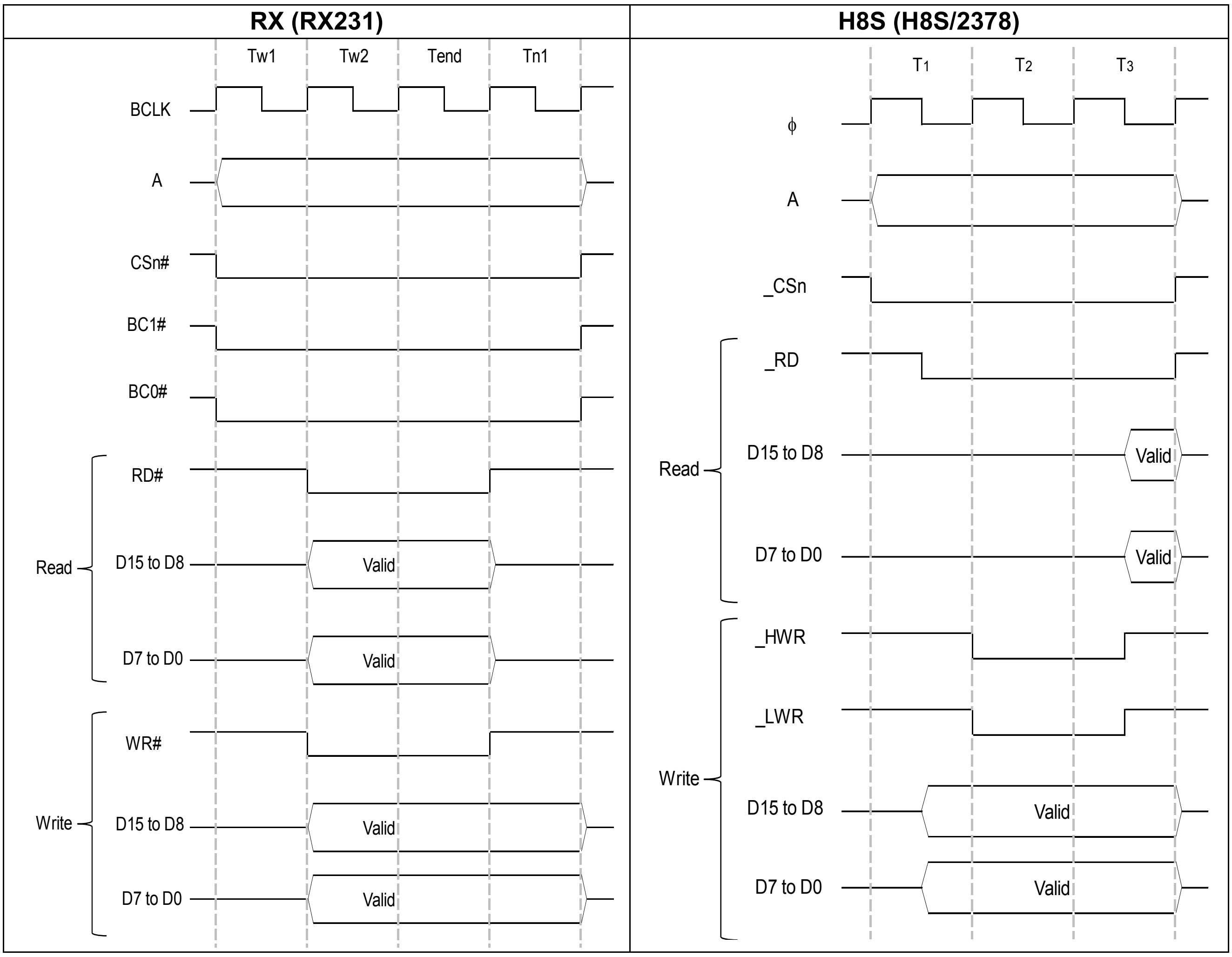


Figure 1.6 Access Timing in 16-Bit Access Space (Even-Number Addresses, Word Access)

When performing word access to odd-number addresses in the 16-bit access space on the RX231 Group, accesses require two bus cycles, in contrast to the above. For details, refer to “Endian and Data Alignment” in the section on buses in User’s Manual: Hardware.

Figure 1.7 compares the access timing when byte strobe mode is selected as the write access mode on the RX231 Group.

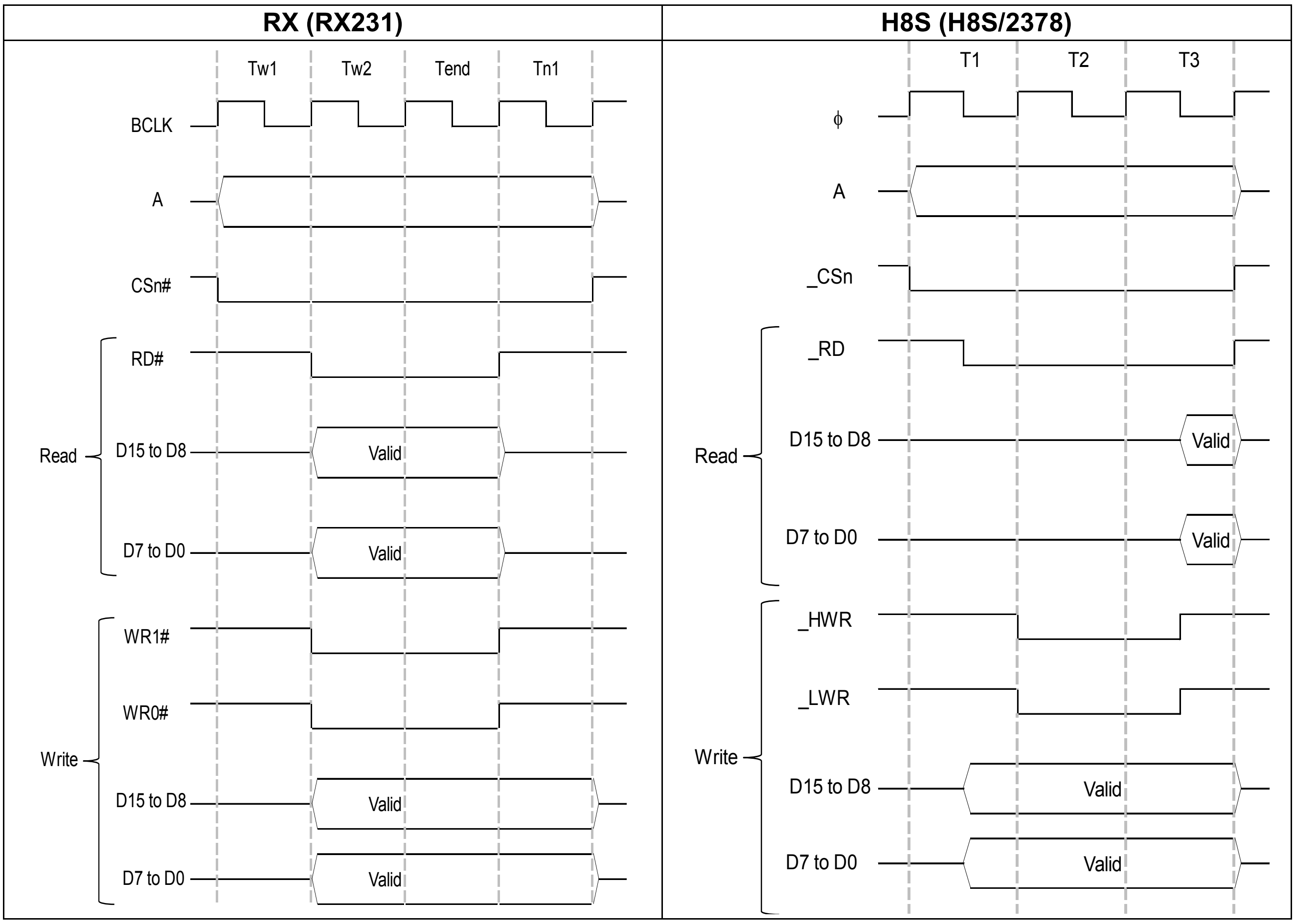


Figure 1.7 Access Timing in Byte Strobe Mode (16-Bit Access Space, Even-Number Addresses, Word Access)

1.3 Calculating Access Cycle Counts

1.3.1 Calculating Access Cycle Counts for Read Accesses

Points of difference between the bus timing settings on the H8S/2378 Series and RX231 Group are shown below, using Figure 1.8, Basic Bus Timing Example (Read Access), as an example.

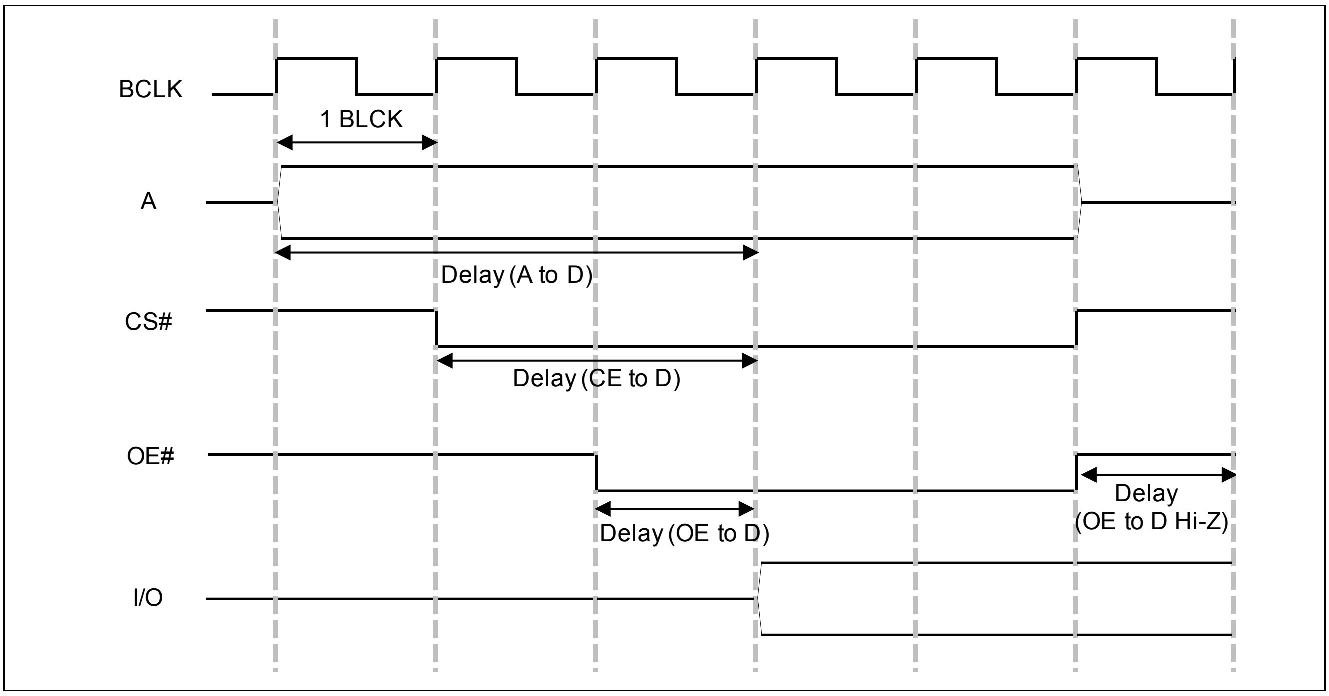


Figure 1.8 Basic Bus Timing Example (Read Access)

Table 1.2 Points of Difference between Bus Timing Related Settings (Read Access)

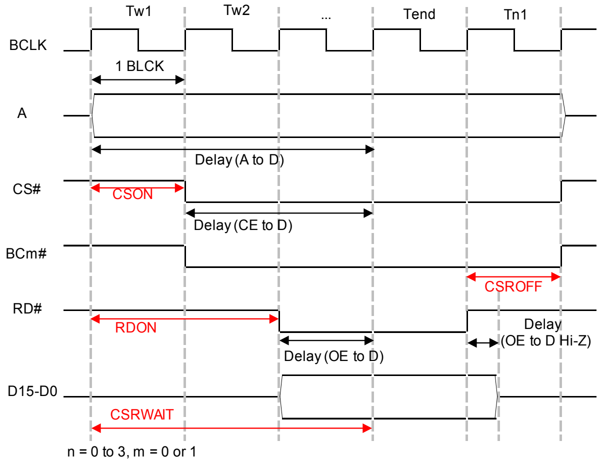
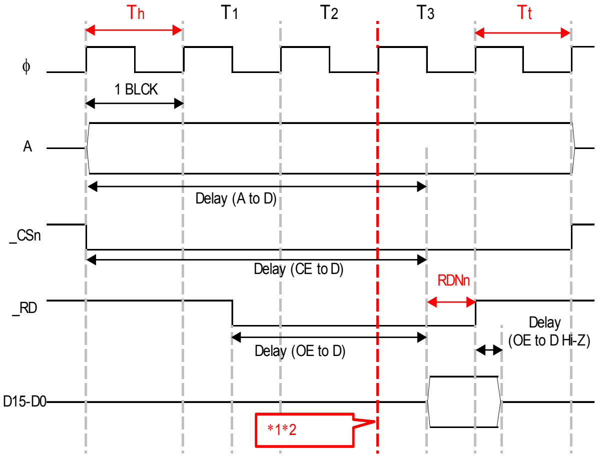
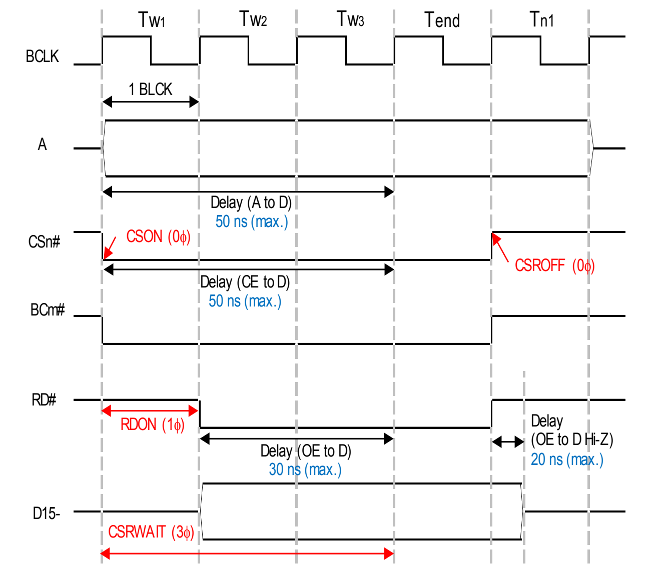
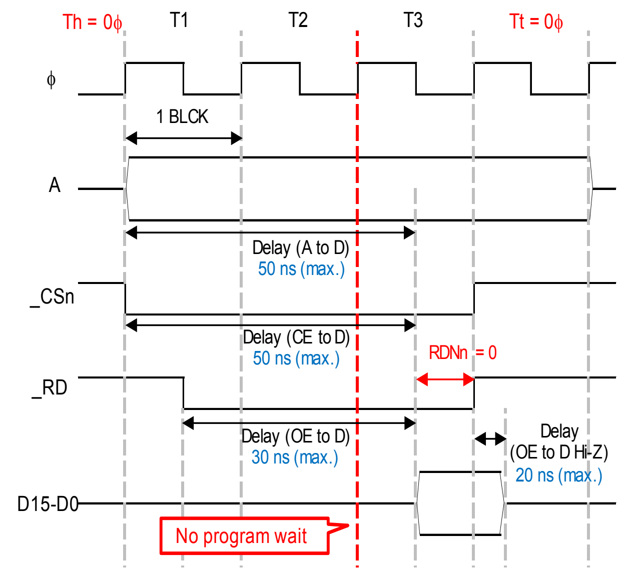
RX (RX231)		H8S (H8S/2378)	
 Tw1 Tw2 ... Tend Tn1 BCLK 1 BLCK A Delay (A to D) CS# CSON Delay (CE to D) BCm# CSROFF RD# RDON Delay (OE to D Hi-Z) Delay (OE to D) D15-D0 CSRWAIT n = 0 to 3, m = 0 or 1		 Th T1 T2 T3 Tt ϕ 1 BLCK A Delay (A to D) _CSn Delay (CE to D) RDNn _RD Delay (OE to D Hi-Z) Delay (OE to D) D15-D0 *1*2	
CSON	Specifies the number of wait cycles inserted before assertion of the CSn# signal.	T_h	Extension state specified before the basic bus cycle (preceding T_1). Set in the upper 8 bits of CSACR.
RDON	Specifies the number of wait cycles inserted before assertion of the RD# signal.	T_t	Extension state specified after the basic bus cycle (following T_3). Set in the lower 8 bits of CSACR.
CSRWAIT	Specifies the number of cycles inserted in the first access of a normal read cycle.	RDNn	Can be used to change the read strobe $\overline{\text{RD}}$ negation timing by one half-state.
CSROFF	Specifies the number of cycles between negation of the RD# signal and negation of the CSn# signal during read access.	Note 1. Program wait A wait (set in WTCRA and WTCRB) can be inserted by a program after the T_2 state.	
		Note 2. Pin wait insertion When the external address area is accessed while the WAITE bit in BCR is set to 1, a pin wait is inserted at the fall of the last program wait state if the $\overline{\text{WAIT}}$ pin is low level.	

Table 1.3 lists the register setting values on the H8S/2378 Series and RX231 Group when the characteristics of the connected external memory are as follows:

- Delay (A to D) = 50 ns (max.)
- Delay (CE to D) = 50 ns (max.)
- Delay (OE to D) = 30 ns (max.)
- Delay (OE to D Hi_Z) = 20 ns (max.)

Table 1.3 Points of Difference between External Bus Register Setting Values (Example for Read Access, BCLK = 32 MHz)

RX (RX231)		H8S (H8S/2378)	
 Tw1 Tw2 Tw3 Tend Tn1 BCLK 1 BLCK A Delay (A to D) 50 ns (max.) CSn# CSON (0ϕ) CSROFF (0ϕ) Delay (CE to D) 50 ns (max.) BCm# RD# RDON (1ϕ) Delay (OE to D) 30 ns (max.) Delay (OE to D Hi-Z) 20 ns (max.) D15- CSRWAIT (3ϕ) n = 0 to 3, m = 0 or 1		 Th = 0ϕ T1 T2 T3 Tt = 0ϕ ϕ 1 BLCK A Delay (A to D) 50 ns (max.) _CSn Delay (CE to D) 50 ns (max.) RDNn = 0 _RD Delay (OE to D) 30 ns (max.) Delay (OE to D Hi-Z) 20 ns (max.) D15-D0 No program wait	
CSON	BSC.CS0WCR2.BIT.CSON = 0;*[1]	Th	BSC.CSACR.BIT.CSXH0 = 0;
RDON	BSC.CS0WCR2.BIT.RDON = 1;*[1]	Tt	BSC.CSACR.BIT.CSXT0 = 0;
CSRWAIT	BSC.CS0WCR1.BIT.CSRWAIT = 3;*[1]	RDNn	BSC.RDNCR.BIT.RDN0 = 0;
CSROFF	BSC.CS0WCR2.BIT.CSROFF = 0;	Program wait	BSC.WCR.BIT.W0 = 000b;*[2]

Note 1. Make settings such that value of CSnWCR2.CSON bits ≤ value of CSnWCR2.RDON bits ≤ value of CSnWCR1.CSRWAIT bits.

Note 2. Program wait is enabled only when 3-state access space (ASTCR.BIT.AST0 = 1) is selected.

Note 3. The register setting examples use register and bit field names that apply when making settings for the CS0 area.

Note 4. The register and bit field names are macro names defined by the development environment. (Register names may differ in some cases.)

1.3.2 Calculating Access Cycle Counts for Write Accesses

Points of difference between the bus timing settings on the H8S/2378 Series and RX231 Group are shown below, using Figure 1.9, Basic Bus Timing Example (Write Access), as an example.

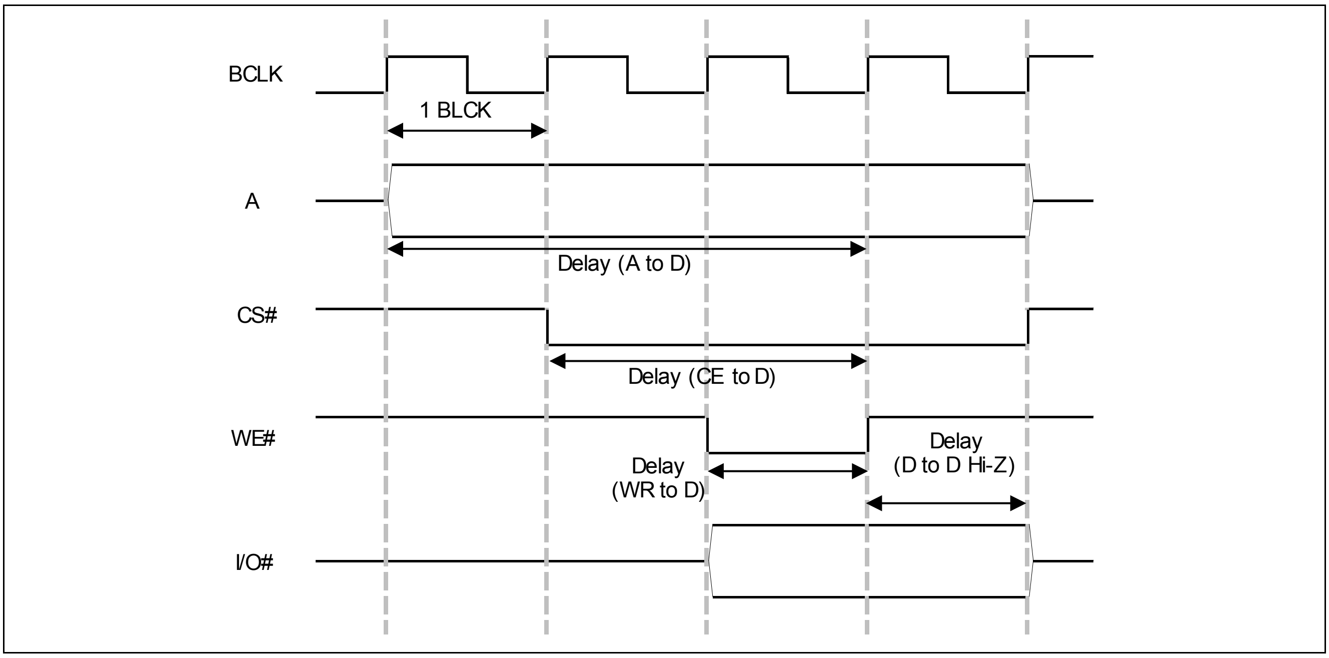


Figure 1.9 Basic Bus Timing Example (Write Access)

Table 1.4 Points of Difference between Bus Timing Related Settings (Write Access)

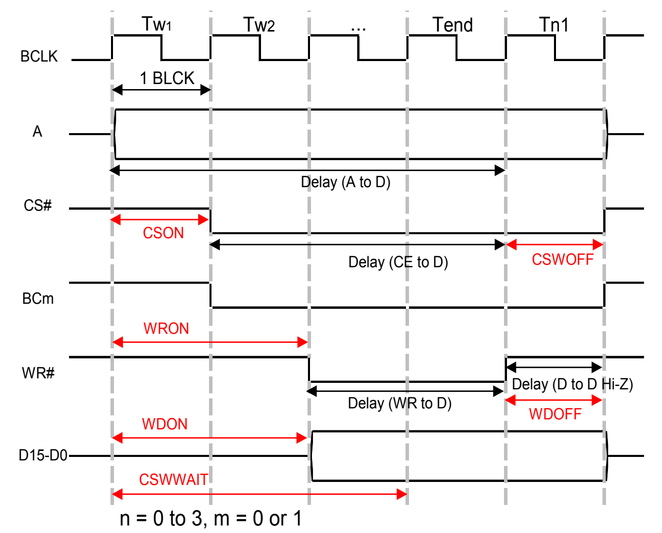
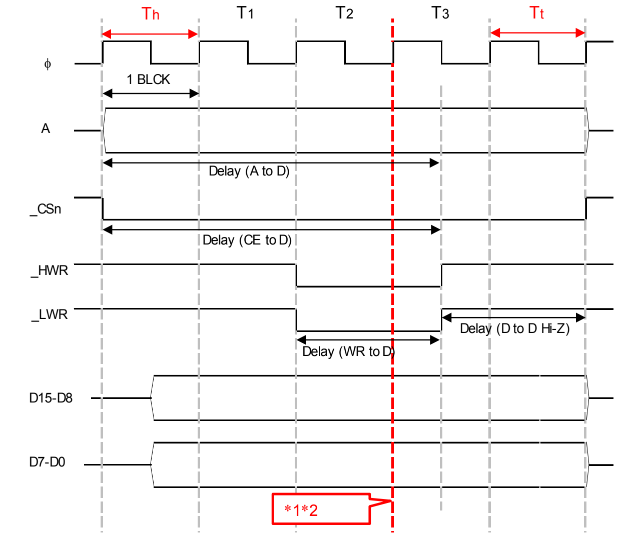
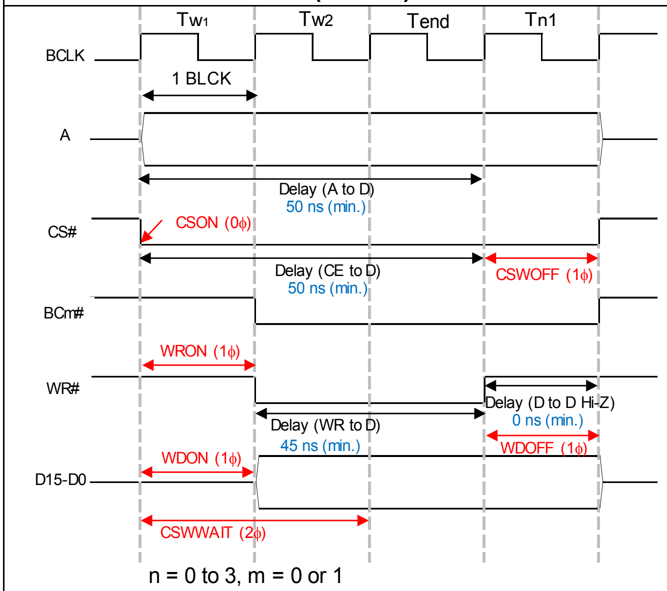
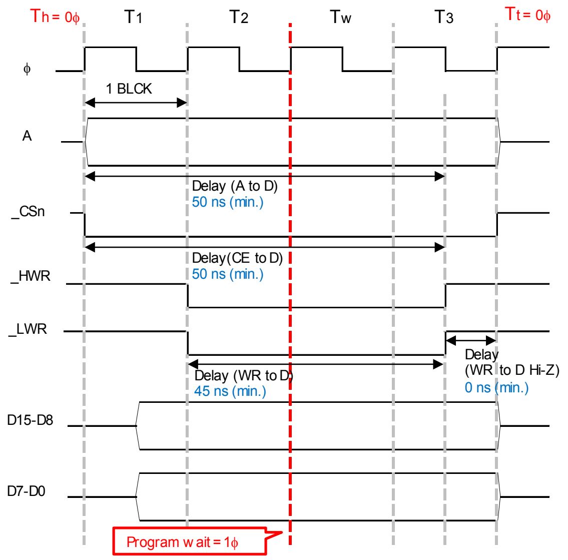
RX (RX231)		H8S (H8S/2378)	
 Tw1 Tw2 ... Tend Tn1 BCLK 1 BLCK A Delay (A to D) CS# CSON Delay (CE to D) CSWOFF BCm WRON WR# Delay (D to D Hi-Z) Delay (WR to D) WDOFF WDON D15-D0 CSWWAIT n = 0 to 3, m = 0 or 1		 Th T1 T2 T3 Tt ϕ 1 BLCK A Delay (A to D) _CSn Delay (CE to D) _HWR _LWR Delay (D to D Hi-Z) Delay (WR to D) D15-D8 D7-D0 *1*2	
CSON	Specifies the number of wait cycles inserted before assertion of the CSn# signal.	T_h	Extension state specified before the basic bus cycle (preceding T_1). Set in the upper 8 bits of CSACR.
WDON	Specifies the number of wait cycles inserted before output of write data.	T_t	Extension state specified after the basic bus cycle (following T_3). Set in the lower 8 bits of CSACR.
WRON	Specifies the number of wait cycles inserted before assertion of the WR# signal.	Note 1. Program wait A wait (set in WTCRA and WTCRB) can be inserted by a program after the T_2 state. Note 2. Pin wait insertion When the external address area is accessed while the WAITE bit in BCR is set to 1, a pin wait is inserted at the fall of the last program wait state if the $\overline{\text{WAIT}}$ pin is low level.	
WDOFF	Specifies the number of cycles between negation of the WR# signal and completion of write data output during write access.		
CSWWAIT	Specifies the number of cycles inserted in the first access of a normal write cycle.		
CSWOFF	Specifies the number of cycles between negation of the WR# signal and negation of the CSn# signal during write access.		

Table 1.5 lists the register setting values on the H8S/2378 Series and RX231 Group when the characteristics of the connected external memory are as follows:

- Delay (A to D) = 50 ns (min.)
- Delay (CE to D) = 50 ns (min.)
- Delay (WR to D) = 45 ns (min.)
- Delay (D to D Hi_Z) = 0 ns (min.)

Table 1.5 Points of Difference between External Bus Register Setting Values (Example for Write Access, BCLK = 32 MHz)

RX (RX231)		H8S (H8S/2378)	
 Tw1 Tw2 Tend Tn1 BCLK 1 BLCK A Delay (A to D) 50 ns (min.) CS# CSON (0ϕ) Delay (CE to D) 50 ns (min.) CSWOFF (1ϕ) BCm# WRON (1ϕ) WR# Delay (D to D Hi-Z) 0 ns (min.) Delay (WR to D) 45 ns (min.) WDOFF (1ϕ) WDON (1ϕ) D15-D0 CSWWAIT (2ϕ) n = 0 to 3, m = 0 or 1		 Th = 0ϕ T1 T2 Tw T3 Tt = 0ϕ ϕ 1 BLCK A Delay (A to D) 50 ns (min.) _CSn Delay(CE to D) 50 ns (min.) _HWR _LWR Delay (WR to D) 45 ns (min.) Delay (WR to D Hi-Z) 0 ns (min.) D15-D8 D7-D0 Program w ait = 1ϕ	
CSON	BSC.CS0WCR2.BIT.CSON = 0;*[1]	T_h	BSC.CSACR.BIT.CSXH0 = 0;
WDON	BSC.CS0WCR2.BIT.WDON = 1;*[1]	T_t	BSC.CSACR.BIT.CSXT0 = 0;
WRON	BSC.CS0WCR2.BIT.WRON = 1;*[1]	Program wait	BSC.WCR.BIT.W0 = 001b;*[3]
WDOFF	BSC.CS0WCR2.BIT.WDOFF = 1;*[2]		
CSWWAIT	BSC.CS0WCR1.BIT.CSWWAIT = 2;*[1]		
CSWOFF	BSC.CS0WCR2.BIT.CSWOFF = 1;*[2]		

Note 1. Make settings such that 1 ≤ value of CSnWCR2.WDON bits ≤ value of CSnWCR2.WRON bits ≤ value of CSnWCR1.CSWWAIT bits and value of CSnWCR2.CSON bits ≤ value of CSnWCR2.WRON bits ≤ value of CSnWCR1.CSWWAIT bits.

Note 2. Make settings such that value of CSnWCR2.WDOFF bits ≤ value of CSnWCR2.CSWOFF bits.

Note 3. Program wait is enabled only when 3-state access space (ASTCR.BIT.AST0 = 1) is selected.

Note 4. The register setting examples use register and bit field names that apply when making settings for the CS0 area.

Note 5. The register and bit field names are macro names defined by the development environment. (Register names may differ in some cases.)

1.3.3 Idle Cycles (Recovery Cycles)

On the H8S/2378 Series and RX231 Group the specification for idle cycles (called recovery cycles on the RX231 Group) extends the period following CS negation.

On the H8S/2378 Series idle cycles of one or two states each can be inserted. The insertion condition can be selected among the following three patterns:

- When consecutive external read cycles are performed in different areas
- When an external read cycle and external write cycle are performed consecutively
- When an external write cycle and external read cycle are performed consecutively

On the RX231 Group a recovery cycle of one to 15 cycles can be inserted. The insertion condition can be selected among the following eight options:

- When, after a read access to the external bus, a read access is made to the same external bus area
- When, after a read access to the external bus, a write access is made to the same external bus area
- When, after a read access to the external bus, a read access is made to a different external bus area
- When, after a read access to the external bus, a write access is made to a different external bus area
- When, after a write access to the external bus, a read access is made to the same external bus area
- When, after a write access to the external bus, a write access is made to the same external bus area
- When, after a write access to the external bus, a read access is made to a different external bus area
- When, after a write access to the external bus, a write access is made to a different external bus area

2. Operating Modes

2.1 Comparison of Operating Modes

On the H8S/2378 Series the microcontroller's operating mode is specified as 1 to 5 or 7 by the setting of the mode pins (MD2 to MD0). In addition, external bus mode can be specified by a program by setting the EXPE bit (external bus mode enable) in SYSCR.

On the RX231 Group boot mode (USB/SCI) or single-chip mode are selected by the state of the mode setting pins (MD and UB), and after a reset the device starts in a state in which the on-chip ROM is enabled and the external bus is disabled. In either of these modes the on-chip ROM and the external bus can be enabled or disabled by a program by setting the ROME bit (on-chip ROM enable/disable bit) and EXBE bit (external bus enable/disable bit) in SYSCR0.

Table 2.1 lists the H8S/2378 Series mode pin settings and corresponding operating modes after a reset. In external extended mode each area of the external bus can be set to either 8-bit or 16-bit width by setting the bus controller's ABWCR (bus width control register).

Table 2.1 H8S/2378 Series Mode Pin Settings and Operating Modes (After a Reset)

MD[2:0]	Operating Mode		On-Chip ROM	External Bus
001b	1	On-chip ROM disabled extended mode	Disabled	Enabled (16-bit)
010b	2	On-chip ROM disabled extended mode		Enabled (8-bit)
011b	3	Boot mode	Enabled	Disabled*[1]
100b	4	On-chip ROM enabled extended mode		Enabled (8-bit)
101b	5	User boot mode		Disabled*[1]
111b	7	Single-chip mode		Disabled*[1]

Note 1. Setting the EXPE bit in SYSCR to 1 enables external extended mode and enables the external address space.

Note 2. The state of pins MD2 to MD0 must not be changed while the microcontroller is operating.

Table 2.2 lists the RX231 Group mode setting pin settings and corresponding operating modes after a reset, and Table 2.3 lists the settings that can be used by programs to enable or disable the ROM and external bus. By making the settings shown in Table 2.3 after the microcontroller starts in single-chip mode, a program can put the device into on-chip ROM enabled extended mode or on-chip ROM disabled extended mode.

Table 2.2 RX231 Group Mode Setting Pin Settings and Operating Modes (After a Reset)

MD	UB	Operating Mode	On-Chip ROM	External Bus
0	0	Boot mode (USB interface)	Enabled	Disabled
0	1	Boot mode (SCI interface)		
1	1	Single-chip mode		

Note: The state of the MD pins must not be changed while the microcontroller is operating.

Table 2.3 RX231 Group Operating Modes and Program Settings

Item	Program Setting
Single-chip mode	None
On-chip ROM enabled extended mode	Set SYSCR0.ROME bit to 1b and SYSCR0.EXBE bit to 1b.
On-chip ROM disabled extended mode	Set SYSCR0.ROME bit to 0b and SYSCR0.EXBE bit to 1b.*[2]

Note 1. The bus width setting is made in the bus control register (CSnCR).

Note 2. This register setting should be made for areas outside the external memory and ROM.

2.2 Functional Points of Difference between Operating Modes

Table 2.4 lists functional points of difference between operating modes when using external memory and on-chip memory on the RX231 Group and H8S/2378 Series, and Table 2.5 lists functional points of difference between operating modes when using external memory only on the RX231 Group and H8S/2378 Series.

Table 2.4 Functional Points of Difference between Operating Modes when Using External Memory and On-Chip Memory (RX231 Group and H8S/2378 Series)

	RX (RX231)	**H8S (H8S/2378)**
Item	**On-Chip ROM Enabled Extended Mode**	**Mode 4** **(On-Chip ROM Enabled Extended Mode)**
Access areas	I/O registers, on-chip RAM, on-chip ROM, external area	I/O registers, on-chip RAM*[1], on-chip ROM, external area
External memory areas	0500 0000h to 07FF FFFFh (CS1 to CS3)	080000h to FF3FFFh FF4000h to FFBFFFh*[2] FFD000h to FFFBFFh FFFF00h to FFFF1Fh

Note 1. Enabled only when RAME bit in SYSCR is set to 1.
Note 2. External address space when RAME bit in SYSCR is cleared to 0.

Table 2.5 Functional Points of Difference between Operating Modes when Using External Memory Only (RX231 Group and H8S/2378 Series)

	RX (RX231)	**H8S (H8S/2378)**
Item	**On-Chip ROM Disabled Extended Mode**	**Mode 1 and 2** **(On-Chip ROM Disabled Extended Mode)**
Access areas	I/O registers, on-chip RAM, on-chip ROM*[1], external area	I/O registers, on-chip RAM*[2], external area
External memory areas	0500 0000h to 07FF FFFFh (CS1 to CS3) FF00 0000h to FFFF FFFFh (CS0)	000000h to FF3FFFh FF4000h to FFBFFFh*[3] FFD000h to FFFBFFh FFFF00h to FFFF1Fh

Note 1. Enabled at startup only.
Note 2. Enabled only when RAME bit in SYSCR is set to 1.
Note 3. External address space when RAME bit in SYSCR is cleared to 0.

3. External Bus Setting Examples

Table 3.1 lists examples of external bus use in different operating modes.

Table 3.1 External Bus Use in Different Operating Modes

	RX (RX231)	H8S (H8S/2378)		
No.	**Mode**	**Mode**	**Operation Example**	**Reference**
1	On-chip ROM enabled extended mode	On-chip ROM enabled extended mode	Reading of data in external memory by a program in on-chip ROM	3.1
2	On-chip ROM disabled extended mode	On-chip ROM disabled extended mode	Reading of data in external memory by a program in external memory	3.2

3.1 Points of Difference between Setting Procedures (On-Chip ROM Enabled Extended Mode Settings)

Table 3.2 lists points of difference between the setting procedures for on-chip ROM enabled extended mode (16-bit bus width), and Table 3.3 lists points of difference between the setting procedures for on-chip ROM enabled extended mode (8-bit bus width).

Table 3.2 Points of Difference between Setting Procedures for On-Chip ROM Enabled Extended Mode (16-Bit Bus Width) (When Accessing CS1 Area*[1])

Procedure		RX (RX231)	H8S (H8S/2378)
1	Pin settings	High-level input to MD pin	100b input to MD[2:0] pins
2	Reset cancelation	Low-level → high-level input to RESET pin (RES#)	Low-level → high-level input to RESET pin ($\overline{\text{RES}}$)
3	Clock setting	Set the clock frequency to be used for operation.	

4	External wait setting
	Write access mode and page access settings*[2]
		BSC.CS1MOD.BIT.EWENB = 0;
		BSC.CS1MOD.BIT.WRMOD = 0;
		BSC.CS1MOD.BIT.PRENB = 0;
		BSC.CS1MOD.BIT.PWENB = 0;
			BSC.BCR.BIT.WAITE = 0;

5	Bus timing settings (common to read and write)	BSC.CS1WCR2.BIT.CSON = 0;	BSC.CSACR.BIT.CSXH1 = 1;
			BSC.CSACR.BIT.CSXT1 = 1;
			BSC.WCR.BIT.W1 = 000b;

6	Bus timing settings (write)	BSC.CS1WCR1.BIT.CSWWAIT = 2;
		BSC.CS1WCR2.BIT.CSWOFF = 1;
		BSC.CS1WCR2.BIT.WDON = 0;
		BSC.CS1WCR2.BIT.WRON = 1;
		BSC.CS1WCR2.BIT.WDOFF = 1;
			None

7	Bus timing settings (read)	BSC.CS1WCR1.BIT.CSRWAIT = 2;
		BSC.CS1WCR2.BIT.CSROFF = 1;
		BSC.CS1WCR2.BIT.RDON = 0;
			BSC.RDNCR.BIT.RDN1 = 0;

8	Idle (recovery) cycle settings	BSC.CS1REC.BIT.RRCV = 0;
		BSC.CS1REC.BIT.WRCV = 0;
		BSC.CSRECEN.WORD = 0x0000;
			BSC.BCR.BIT.ICIS1 = 0;
			BSC.BCR.BIT.ICIS0 = 0;
			BSC.BCR.BIT.ICIS2 = 0;

Procedure		RX (RX231)	H8S (H8S/2378)

9	Bus pin settings	MPC.PFCSE.BIT.CS1E = 1;
		MPC.PFAOE0.BYTE = 0xFF;
		MPC.PFAOE1.BYTE = 0x0F;
		MPC.PFBCR0.BYTE = 0x11;
			BSC.PFCR0.BIT.CS1E = 1;
			BSC.PFCR2.BIT.ASOR = 1;
			BSC.PFCR2.BIT.LWROE = 1;
			BSC.PFCR1.BYTE = 0x0F;
			PA.DDR = 0x0F;
			PB.DDR = 0xFF;
			PC.DDR = 0xFF;
			PF.DDR = 0x80;
			PG.DDR = 0x02;

10	Bus width setting
	Endian setting, bus interface, and operation enabled/disabled settings*[2]
		BSC.CS1CR.BIT.BSIZE = 0;
		BSC.CS1CR.BIT.EMODE = 0;*[3]
		BSC.CS1CR.BIT.MPXEN = 0;
		BSC.CS1CT.BIT.EXENB = 1;
			BSC.ABWCR.BIT.ABW1 = 0;

11	Operating mode switching	SYSTEM.PRCR.WORD = 0xA502;*[4]
		SYSTEM.SYSCR0.WORD = 0x5A03;
		SYSTEM.PRCR.WORD = 0xA500;*[4]
			None

Note 1. On the RX231 Group the CS0 area is disabled in on-chip ROM enabled extended mode.

Note 2. RX231 Group only.

Note 3. Endian settings are made by means of the MDE.MDE[2:0] bits and CSnCR.EMODE bit in the option setting memory.

Note 4. The SYSCR0 register is protected by the write protection function, so it is necessary to disable write protection before overwriting the register and then re-enable write protection afterward. (For more information, see 4.1.4, Register Write Protection Function.)

Note 5. The register and bit field names are macro names defined by the development environment. (Register names may differ in some cases.)

Table 3.3 Points of Difference between Setting Procedures for On-Chip ROM Enabled Extended Mode (8-Bit Bus Width) (When Accessing CS1 Area1*[1])

Procedure		RX (RX231)	H8S (H8S/2378)
1	Pin settings	High-level input to MD pin	100b input to MD[2:0] pins
2	Reset cancelation	Low-level → high-level input to RESET pin (RES#)	Low-level → high-level input to RESET pin ($\overline{\text{RES}}$)
3	Clock setting	Set the clock frequency to be used for operation.	

4	External wait setting
	Write access mode and page access settings*[2]
		BSC.CS1MOD.BIT.EWENB = 0;
		BSC.CS1MOD.BIT.WRMOD = 0;
		BSC.CS1MOD.BIT.PRENB = 0;
		BSC.CS1MOD.BIT.PWENB = 0;
			BSC.BCR.BIT.WAITE = 0;

5	Bus timing settings (common to read and write)	BSC.CS1WCR2.BIT.CSON = 0;	BSC.CSACR.BIT.CSXH1 = 1;
			BSC.CSACR.BIT.CSXT1 = 1;
			BSC.WCR.BIT.W1 = 000b;

6	Bus timing settings (write)	BSC.CS1WCR1.BIT.CSWWAIT = 2;
		BSC.CS1WCR2.BIT.CSWOFF = 1;
		BSC.CS1WCR2.BIT.WDON = 0;
		BSC.CS1WCR2.BIT.WRON = 1;
		BSC.CS1WCR2.BIT.WDOFF = 1;
			None

7	Bus timing settings (read)	BSC.CS1WCR1.BIT.CSRWAIT = 2;
		BSC.CS1WCR2.BIT.CSROFF = 1;
		BSC.CS1WCR2.BIT.RDON = 0;
			BSC.RDNCR.BIT.RDN1 = 0;

8	Idle (recovery) cycle settings	BSC.CS1REC.BIT.RRCV = 0;
		BSC.CS1REC.BIT.WRCV = 0;
		BSC.CSRECEN.WORD = 0x0000;
			BSC.BCR.BIT.ICIS1 = 0;
			BSC.BCR.BIT.ICIS0 = 0;
			BSC.BCR.BIT.ICIS2 = 0;

9	Bus pin settings	MPC.PFCSE.BIT.CS1E = 1;
		MPC.PFAOE0.BYTE = 0xFF;
		MPC.PFAOE1.BYTE = 0x0F;
		MPC.PFBCR0.BYTE = 0x01;
			BSC.PFCR0.BIT.CS1E = 1;
			BSC.PFCR2.BIT.ASOR = 1;
			BSC.PFCR2.BIT.LWROE = 1;
			BSC.PFCR1.BYTE = 0x0F;
			PA.DDR = 0x0F;
			PB.DDR = 0xFF;
			PC.DDR = 0xFF;
			PF.DDR = 0x80;
			PG.DDR = 0x02;

10	Bus width setting
	Endian setting, bus interface, and operation enabled/disabled settings*[2]
		BSC.CS1CR.BIT.BSIZE = 2;
		BSC.CS1CR.BIT.EMODE = 0;*[3]
		BSC.CS1CR.BIT.MPXEN = 0;
		BSC.CS1CT.BIT.EXENB = 1;
			None
			(The initial bus width setting is 8-bit.)

11	Operating mode switching	SYSTEM.PRCR.WORD = 0xA502;*[4]
		SYSTEM.SYSCR0.WORD = 0x5A03;
		SYSTEM.PRCR.WORD = 0xA500;*[4]
			None

Note 1. On the RX231 Group the CS0 area is disabled in on-chip ROM enabled extended mode.

Note 2. RX231 Group only.

Note 3. Endian settings are made by means of the MDE.MDE[2:0] bits and CSnCR.EMODE bit in the option setting memory.

Note 4. The SYSCR0 register is protected by the write protection function, so it is necessary to disable write protection before overwriting the register and then re-enable write protection afterward. (For more information, see 4.1.4, Register Write Protection Function.)

Note 5. The register and bit field names are macro names defined by the development environment. (Register names may differ in some cases.)

3.2 Points of Difference between Setting Procedures (On-Chip ROM Disabled Extended Mode Settings)

Table 3.4 lists points of difference between the setting procedures for on-chip ROM disabled extended mode (16-bit bus width), and Table 3.5 lists points of difference between the setting procedures for on-chip ROM disabled extended mode (8-bit bus width).

Table 3.4 Points of Difference between Setting Procedures for On-Chip ROM Disabled Extended Mode (16-Bit Bus Width) (When Accessing CS0 Area)

Procedure		RX (RX231)	H8S (H8S/2378)
1	Pin settings	High-level input to MD pin	001b input to MD[2:0] pins
2	Reset cancelation	Low-level → high-level input to RESET pin (RES#)	Low-level → high-level input to RESET pin ($\overline{\text{RES}}$)

3	External wait setting
	Write access mode and page access settings*[1]
		BSC.CS0MOD.BIT.EWENB = 0;
		BSC.CS0MOD.BIT.WRMOD = 0;
		BSC.CS0MOD.BIT.PRENB = 0;
		BSC.CS0MOD.BIT.PWENB = 0;
			BSC.BCR.BIT.WAITE = 0;
			*[3]

4	Bus timing settings (common to read and write)	BSC.CS0WCR2.BIT.CSON = 0;	BSC.ASTCR.BYTE = 0xFF;
			BSC.WCR.WORD.A = 0x7777;(WTCRA)
			BSC.WCR.WORD.B = 0x7777;(WTCRB)
			BSC.CSACR.WORD = 0x0000;
			*[3]

5	Bus timing settings (write)	BSC.CS0WCR1.BIT.CSWWAIT = 2;
		BSC.CS0WCR2.BIT.CSWOFF = 1;
		BSC.CS0WCR2.BIT.WDON = 0;
		BSC.CS0WCR2.BIT.WRON = 1;
		BSC.CS0WCR2.BIT.WDOFF = 1;
			None

6	Bus timing settings (read)	BSC.CS0WCR1.BIT.CSRWAIT = 2;
		BSC.CS0WCR2.BIT.CSROFF = 1;
		BSC.CS0WCR2.BIT.RDON = 0;
			BSC.RDNCR.BYTE = 0x00;
			*[3]

7	Idle (recovery) cycle settings	BSC.CS0REC.BIT.RRCV = 0;
		BSC.CS0REC.BIT.WRCV = 0;
		BSC.CSRECEN.WORD = 0x0000;
			BSC.BCR.BIT.IDLC = 1;
			BSC.BCR.BIT.ICIS1 = 1;
			BSC.BCR.BIT.ICIS0 = 1;
			BSC.BCR.BIT.ICIS2 = 0;
			*[3]

8	Bus pin settings	MPC.PFCSE.BIT.CS0E = 1;
		MPC.PFAOE0.BYTE = 0xFF;
		MPC.PFAOE1.BYTE = 0x0F;
		MPC.PFBCR0.BYTE = 0x11;
			BSC.PFCR0.BYTE = 0xFF;
			BSC.PFCR2.BYTE = 0x0E;
			BSC.PFCR1.BYTE = 0xFF;
			PA.DDR = 0x00;
			PB.DDR = 0x00;
			PC.DDR = 0x00;
			PD.DDR = 0x00;
			PE.DDR = 0x00;
			PF.DDR = 0x80;
			PG.DDR = 0x01;
			PH.DDR = 0x00;
			*[3]

9	Bus width setting
	Endian setting, bus
		BSC.CS1CR.BIT.BSIZE = 0;
		BSC.CS1CR.BIT.EMODE = 0;*[2]
			BSC.ABWCR.BYTE = 0x00;
			*[3]

Procedure		RX (RX231)	H8S (H8S/2378)

	interface, and operation enabled/disabled settings*[1]	BSC.CS1CR.BIT.MPXEN = 0;
		BSC.CS1CT.BIT.EXENB = 1;	

10	RAM program execution	Transfer to RAM the program that performs processing steps 11 and 12, and jump to it.	None

11	Operating mode switching	SYSTEM.PRCR.WORD = 0xA502;*[4]
		SYSTEM.SYSCR0.WORD = 0x5A02;
		SYSTEM.PRCR.WORD = 0xA500;*[4]
			None

12	Jump to first program in external memory to be run	Jump to the previously determined address in external memory.	Read the reset vector (address 0) from external memory and jump to the specified address.
—	Bus settings for accessing external memory	Access the CS0 area in the specified cycle.	Access CS0 using the initial access timing value.
—	Clock setting	Set the clock frequency to be used for operation.	

Note 1. RX231 Group only.

Note 2. Endian settings are made by means of the MDE.MDE[2:0] bits and CSnCR.EMODE bit in the option setting memory.

Note 3. Values shown for each register are initial values. Each register remains set to its initial value when operation starts.

Note 4. The SYSCR0 register is protected by the write protection function, so it is necessary to disable write protection before overwriting the register and then re-enable write protection afterward. (For more information, see 4.1.4, Register Write Protection Function.)

Note 5. The register and bit field names are macro names defined by the development environment. (Register names may differ in some cases.)

Table 3.5 Points of Difference between Setting Procedures for On-Chip ROM Disabled Extended Mode (8-Bit Bus Width) (When Accessing CS0 Area)

Procedure		RX (RX231)	H8S (H8S/2378)
1	Pin settings	High-level input to MD pin	010b input to MD[2:0] pins
2	Reset cancelation	Low-level → high-level input to RESET pin (RES#)	Low-level → high-level input to RESET pin ($\overline{\text{RES}}$)

3	External wait setting
	Write access mode and page access settings
		BSC.CS0MOD.BIT.EWENB = 0;
		BSC.CS0MOD.BIT.WRMOD = 0;
		BSC.CS0MOD.BIT.PRENB = 0;
		BSC.CS0MOD.BIT.PWENB = 0;
			BSC.BCR.BIT.WAITE = 0;
			*3

4	Bus timing settings (common to read and write)	BSC.CS0WCR2.BIT.CSON = 0;	BSC.ASTCR.BYTE = 0xFF;
			BSC.WCR.WORD.A = 0x7777;(WTCRA)
			BSC.WCR.WORD.B = 0x7777;(WTCRB)
			BSC.CSACR.WORD = 0x0000;
			*3

5	Bus timing settings (write)	BSC.CS0WCR1.BIT.CSWWAIT = 2;
		BSC.CS0WCR2.BIT.CSWOFF = 1;
		BSC.CS0WCR2.BIT.WDON = 0;
		BSC.CS0WCR2.BIT.WRON = 1;
		BSC.CS0WCR2.BIT.WDOFF = 1;
			None

6	Bus timing settings (read)	BSC.CS0WCR1.BIT.CSRWAIT = 2;
		BSC.CS0WCR2.BIT.CSROFF = 1;
		BSC.CS0WCR2.BIT.RDON = 0;
			BSC.RDNCR.BYTE = 0x00;
			*3

7	Idle (recovery) cycle settings	BSC.CS0REC.BIT.RRCV = 0;
		BSC.CS0REC.BIT.WRCV = 0;
		BSC.CSRECEN.WORD = 0x0000;
			BSC.BCR.BIT.IDLC = 1;
			BSC.BCR.BIT.ICIS1 = 1;
			BSC.BCR.BIT.ICIS0 = 1;
			BSC.BCR.BIT.ICIS2 = 0;
			*3

8	Bus pin settings	MPC.PFCSE.BIT.CS0E = 1;
		MPC.PFAOE0.BYTE = 0xFF;
		MPC.PFAOE1.BYTE = 0x0F;
		MPC.PFBCR0.BYTE = 0x01;
			BSC.PFCR0.BYTE = 0xFF;
			BSC.PFCR2.BYTE = 0x0E;
			BSC.PFCR1.BYTE = 0xFF;
			PA.DDR = 0x00;
			PB.DDR = 0x00;
			PC.DDR = 0x00;
			PD.DDR = 0x00;
			PE.DDR = 0x00;
			PF.DDR = 0x80;
			PG.DDR = 0x01;
			PH.DDR = 0x00;
			*3

9	Bus width setting
	Endian setting, bus interface, and operation enabled/disabled settings*1
		BSC.CS1CR.BIT.BSIZE = 2;
		BSC.CS1CR.BIT.EMODE = 0;*2
		BSC.CS1CR.BIT.MPXEN = 0;
		BSC.CS1CT.BIT.EXENB = 1;
			BSC.ABWCR.BYTE = 0xFF;
			*3

10	RAM program execution	Transfer to RAM the program that performs processing steps 11 and 12, and jump to it.	None

Procedure		RX (RX231)	H8S (H8S/2378)

11	Operating mode switching	SYSTEM.PRCR.WORD = 0xA502;*[4]
		SYSTEM.SYSCR0.WORD = 0x5A02;
		SYSTEM.PRCR.WORD = 0xA500;*[4]
			None

12	Jump to first program in external memory to be run	Jump to the previously determined address in external memory.	Read the reset vector (address 0) from external memory and jump to the specified address.
—	Bus settings for accessing external memory	Access the CS0 area in the specified cycle.	Access CS0 using the initial access timing value.
—	Clock setting	Set the clock frequency to be used for operation.	

Note 1. RX231 Group only.

Note 2. Endian settings are made by means of the MDE.MDE[2:0] bits and CSnCR.EMODE bit in the option setting memory.

Note 3. Values shown for each register are initial values. Each register remains set to its initial value when operation starts.

Note 4. The SYSCR0 register is protected by the write protection function, so it is necessary to disable write protection before overwriting the register and then re-enable write protection afterward. (For more information, see 4.1.4, Register Write Protection Function.)

Note 5. The register and bit field names are macro names defined by the development environment. (Register names may differ in some cases.)

4. Appendix

4.1 Key Points when Migrating from H8S to RX

Some points to keep in mind when migrating from the H8S/2378 Series to the RX231 Group are described below.

4.1.1 Interrupts

Interrupts can be accepted on the RX231 Group when the following conditions are met:

- The I flag (PSW.I bit) is set to 1.
- The interrupt is enabled in the IER and IPR registers of the ICU.
- Interrupt requests are enabled by the corresponding peripheral function interrupt request enable bit.

Table 4.1 is a comparative listing of the interrupt generation conditions on the RX231 Group and H8S/2378 Series.

Table 4.1 Comparative Listing of Interrupt Generation Conditions on RX231 Group and H8S/2378 Series

Item	RX (RX231)	H8S (H8S/2378)
Interrupt enable bit	Setting the I flag in the PSW register to 1 (enabled) enables acceptance of maskable interrupts.	In interrupt control mode 0, setting the I flag to 0 (enabled) in the CCR register enables acceptance of maskable interrupts. In interrupt control mode 2 the I flag in the CCR register is not used.
Processor interrupt priority level	Only interrupt requests with a higher priority level than that indicated by the IPL[3:0] bits in the PSW register are accepted.	In interrupt control mode 2 only interrupt requests with a higher priority level than that indicated by bits I2 to I0 in the EXR register are accepted. In interrupt control mode 0 the bits I2 to I0 in the EXR register is not used.
Interrupt request flag	The interrupt controller manages all interrupt status flags for peripheral functions, external pins, NMI interrupts, etc.	The interrupt controller manages interrupt status flags for external interrupts, and interrupt status flags for internal interrupt sources are managed within each on-chip peripheral function.
Interrupt priority level	Set in the IPR register.	In interrupt control mode 0 the default settings are used. In interrupt control mode 2 the IPR register settings are used.
Interrupt request enable	Set in the IER register for maskable interrupts and in the NMIER register for non-maskable interrupts.	IRQ interrupts are enabled by settings in the IER register.
Peripheral function interrupt enable	Interrupts can be enabled or disabled by each peripheral function.	

For details, refer to the sections on the interrupt controller (ICU), CPU, and peripheral functions in User's Manual: Hardware.

4.1.2 I/O Ports

On the RX231 Group it is necessary to make settings to the MPC in order to assign peripheral function I/O signals to pins.

The following two settings should be made before performing pin I/O control on the RX231 Group:

- PFS register of MPC: Selection of peripheral function to be assigned to the relevant pin
- PMR register of I/O port: Selection of whether the relevant pin will be assigned to a general I/O port or to a peripheral function

Table 4.2 is a comparative listing of peripheral function pin I/O settings on the RX231 Group and H8S/2378 Series.

Table 4.2 Comparative Listing of Peripheral Function Pin I/O Settings on RX231 Group and H8S/2378 Series

Function	RX (RX231)	H8S (H8S/2378)
Pin function selection	I/O pins for peripheral functions can be assigned from a selection of multiple pins by making settings in the PFS register.	Pins can be switched between general I/O port and peripheral function settings and pin functions selected through combinations of the MCU operating mode, the setting of the SYSCR.EXPE bit, the PFCR registers, the DDR registers, and the settings of the various peripheral functions.
General I/O port/peripheral function switching	Settings in the PMR register can be used to select whether specific pins are used as I/O ports or as peripheral functions.	

For details, refer to the sections on the multifunction pin controller (MPC) and I/O ports in User's Manual: Hardware.

4.1.3 Module Stop Function

On the RX231 Group it is possible to halt the functioning of individual peripheral modules.

Power consumption can be reduced by transitioning unused modules to the module stop state.

Most modules are in the module stop state after a reset.

It is not possible to read or write to the registers of a module when it is in the module stop state.

For details, refer to the section on low power consumption functions in User's Manual: Hardware.

4.1.4 Register Write Protection Function

On the RX231 Group it is possible to protect important registers from being overwritten if program runaway occurs. The protect register (PRCR) is used to specify the registers that are protected by this function.

For details, refer to the section on the register write protection function in User's Manual: Hardware.

4.2 I/O Register Macros

The macro definitions listed below are contained in the I/O register definition file (iodefine.h) of the RX231 Group. Using macro definitions can make program code easier to read. Table 4.3 lists macro usage examples.

Table 4.3 Macro Usage Examples

Macro	Usage Example
IR(“module name”,”bit name”)	IR(MTU0,TGIA0) = 0; Clears the IR bit corresponding to TGIA0 of MTU0 to 0 (clear interrupt request).
DTCE(”module name”,”bit name”)	DTCE(MTU0,TGIA0) = 1; Sets the DTCE bit corresponding to TGIA0 of MTU0 to 1 (enable DTC start).
IEN(“module name”,”bit name”)	IEN(MTU0,TGIA0) = 1; Sets the IEN bit corresponding to TGIA0 of MTU0 to 1 (enable interrupt).
IPR(“module name”,”bit name”)	IPR(MTU0,TGIA0) = 0x02; Sets the IPR bits corresponding to TGIA0 of MTU0 to 2 (interrupt priority level 2).
MSTP(“module name”)	MSTP(MTU) = 0; Clears the module stop setting bit of MTU0 to 0 (cancel module stop state).
VECT(“module name”,”bit name”)	#pragma interrupt(Excep_MTU0_TGIA0(vect=VECT(MTU0,TGIA0))) Declares the interrupt function corresponding to TGIA0 of MTU0.

4.3 Interrupt Functions

On the RX231 Group interrupt functions are provided to implement control register settings or special instructions. To use these interrupt functions, include the file machine.h.

Table 4.4 lists (examples of) points of difference between control register settings and special instructions on the RX231 Group and H8S/2378 Series.

Table 4.4 Points of Difference between Control Register Settings and Special Instructions on RX231 Group and H8S/2378 Series

	Format	
Item	RX (RX231)	H8S (H8S/2378)
Set I flag to 1.	setpsw_i(); *[1]	set_imask_ccr(1); *[1]*[2]
Clear I flag to 0.	clrpsw_i(); *[1]	set_imask_ccr(0); *[1]*[2]
Expand to WAIT instruction.	wait(); *[1]	None
Expand to NOP instruction.	nop(); *[1]	nop(); *[1]

Note 1. It is necessary to include the file machine.h.

Note 2. I = 1 means enable interrupts on the RX231 Group, and I = 1 means mask interrupts on the H8S/2378 Series.

5. Reference Documents

User’s Manual: Hardware

H8S/2378 Group, H8S/2378R Group Hardware Manual Rev.7.00 (REJ09B0109-0700)
RX230 Group and RX231 Group User’s Manual: Hardware Rev.1.10 (R01UH0496EJ0110)
(The latest versions can be downloaded from the Renesas Electronics website.)

Application Note

RX Family, M16C Family Migrating From the M16C Family to the RX Family: External Bus Rev.1.00 (R01AN2100EJ0100)
(The latest versions can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest versions can be downloaded from the Renesas Electronics website.)

User’s Manual: Development Environment

CC-RX Compiler User’s Manual Rev.1.04 (R20UT3248EJ0104)
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package Ver.6.01 User’s Manual (REJ10B0161-0100)
(The latest versions can be downloaded from the Renesas Electronics website.)

Website and Support

Renesas Electronics Website
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Revision History

		Description	
Rev.	Date	Page	Summary
1.00	Nov. 8, 2017	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

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