RX Family, H8S Family

H8S to RX Migration Guide: Timer

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Summary

This application note explains how to migrate from the TPU of the H8S Family to the TPU of the RX Family, or from the TPU of the H8S Family to the MTU of the RX Family.

Target Devices

- RX Family
- H8S Family

An example of migrating from the H8S Family to the RX Family is presented, with the RX Family represented by the RX231 Group and the H8S Family represented by the H8S/2378 Group. When using this application note with other microcontrollers, appropriate changes should be made to match the specifications of the microcontroller used and thorough evaluation should be performed.

Devices on Which Operation Has Been Confirmed

- RX Family: RX231
- H8S Family: H8S/2378

Some terminology differs between the RX Family and the H8S Family. Differences in timer-related terminology are listed in the table below.

Table Differences in Terminology between RX Family and H8S Family

Item	RX Family	H8S Family
Names of timer modules	16-bit timer pulse unit (TPUa) Watchdog timer (WDTA)	16-bit timer pulse unit (TPU) Watchdog timer (WDT)
Channel names (TPU)	TPUm (m: channel number)	Channel m (m: channel number)
Register names (TGRA)	TPUm.TGRA (m: channel number)	TGRA_m (m: channel number)
Pin names (TIOCA)	TPUm.TIOCA (m: channel number)	TIOCAm (m: channel number)
Peripheral function operating clock	Peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD)	ϕ
Timer operating clock (count clock)	Counter clock	Counter input clock

Contents

1. Timer Comparison

1.1 Timer Functions of Each Microcontroller

Table 1.1 lists points of difference between the timer functions of the H8S/2378 Group and RX231 Group.

Table 1.1 Points of Difference between Timer Functions of H8S/2378 Group and RX231 Group

RX (RX231)	H8S (H8S/2378)
8-bit timer (TMR)	8-bit timer (TMR)
16-bit timer pulse unit (TPUa)	16-bit timer pulse unit (TPU)
Multi-function timer pulse unit 2 (MTU2a)	Not available
Port output enable 2 (POE2a)	
Compare match timer (CMT)	
Low-power timer (LPT)	
Watchdog timer (WDTA)	Watchdog timer (WDT)
Independent watchdog timer (IWDTa)	Not available

As shown in Table 1.1, the following options are available when migrating from the timer functions of the H8S/2378 Group to the RX231 Group:

- Switching from TPU of H8S/2378 Group to TPUa (TPU) of RX231 Group
- Switching from TPU of H8S/2378 Group to MTU2a (MTU) of RX231 Group

This document presents points of difference and points requiring caution when switching from TPU to TPU or from TPU to MTU.

1.2 Comparison of TPU Functions

Table 1.2 lists points of difference between the TPU functions of the H8S/2378 Group and RX231 Group.

Table 1.2 Points of Difference between TPU Functions of H8S/2378 Group and RX231 Group

Item	RX (RX231)	H8S (H8S/2378)
Pulse input/output	Maximum 16	
Count clocks	7 or 8 clocks per channel	8 clocks per channel
Available operations	• Waveform output at compare match • Input capture function • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 15-phase PWM output in combination with synchronous operation • Cascade connection operation	
TPU0, TPU3	Ability to specify buffer operation	
TPU1, TPU2, TPU4, TPU5	Ability to specify phase counting mode	
Interrupt sources	26	
Buffer operation	Automatic transfer of register data	
A/D converter trigger generation	A/D converter start triggers can be generated. (TPU0 to TPU4)	A/D converter start triggers can be generated. (Channels 0 to 5)
PPG trigger generation	Not available	Programmable pulse generator (PPG) output trigger generation is available. (Channels 0 to 3)
Low power consumption function	Module stop state can be set.	
Noise filtering function	Settable by input capture	Not available

1.3 Comparison of TPU and MTU Functions

Table 1.3 lists points of difference between the TPU functions of the H8S/2378 Group and the MTU functions of the RX231 Group.

Table 1.4 lists points of difference between the TPU channels of the H8S/2378 Group and the MTU channels of the RX231 Group.

Table 1.3 Points of Difference between TPU Functions of H8S/2378 Group and MTU Functions of RX231 Group

Item	RX (RX231)	H8S (H8S/2378)
Pulse input/output	Maximum 16	
Pulse input	3	Not available
Count clocks	7 or 8 clocks per channel (4 clocks for MTU5)	8 clocks per channel
Available operations	MTU0 to MTU4 • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation MTU0, MTU3, and MTU4 • Ability to specify buffer operation • Ability to select between 2 types of waveform output (chopping and level) for AC synchronous motor (brushless DC motor) drive mode using complementary PWM output or reset-synchronized PWM output MTU1 and MTU2 • Ability to specify phase counting mode independently • Cascade connection operation MTU3 and MTU4 • A total of 6 layers of waveform output, including 3 phases each for positive and negative complementary PWM or reset PWM output, by interlocking operation MTU5 • Dead time compensation counter function • Input capture function (noise filter setting) • Counter clear operation	Channels 0 to 5 • Waveform output at compare match • Input capture function • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 15-phase PWM output in combination with synchronous operation Channels 0 and 3 • Ability to specify buffer operation Channels 1, 2, 4, and 5 • Ability to specify phase counting mode

Item	RX (RX231)	H8S (H8S/2378)
Complementary PWM modes	• Interrupts at counter peak and trough • A/D converter start trigger skipping function	Not available
Interrupt sources	28	26
Buffer operation	Automatic transfer of register data	
A/D converter trigger generation	A/D converter start triggers can be generated. (MTU0 to MTU4)	A/D converter start triggers can be generated. (Channels 0 to 5)
PPG trigger generation	Not available	Programmable pulse generator (PPG) output trigger generation is available.
Low power consumption function	Module stop state can be set.	

Table 1.4 Points of Difference between TPU Channels of H8S/2378 Group and MTU Channels of RX231 Group

Item		Channel 0	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5
Compare match output	H8S	○	○	○	○	○	○
	RX	○	○	○	○	○	—
Input capture function	H8S	○	○	○	○	○	○
	RX	○	○	○	○	○	○
Synchronous operation	H8S	○	○	○	○	○	○
	RX	○	○	○	○	○	—
PWM mode 1	H8S	○	○	○	○	○	○
	RX	○	○	○	○	○	—
PWM mode 2	H8S	○	○	○	○	○	○
	RX	○	○	○	—	—	—
Phase counting mode	H8S	—	○	○	—	○	○
	RX	—	○	○	—	—	—
Buffer operation	H8S	○	—	—	○	—	—
	RX	○	—	—	○	○	—
Complementary PWM modes	H8S	Not available					
	RX	—	—	—	○	○	—
Reset-synchronized PWM	H8S	Not available					
	RX	—	—	—	○	○	—
AC synchronous motor drive mode	H8S	Not available					
	RX	○	—	—	○	○	—
Dead time compensation counter function	H8S	Not available					
	RX	—	—	—	—	—	○

2. TPU to TPU Migration

2.1 Register Comparison

Table 2.1 lists the TPU registers of the RX231 Group and H8S/2378 Group.

Table 2.1 TPU Registers of RX231 Group and H8S/2378 Group

RX (RX231)	H8S (H8S/2378)
Timer control register (TCR)	Timer control register (TCR)
Timer mode register (TMDR)	Timer mode register (TMDR)
Timer I/O control register (TIOR)	Timer I/O control register (TIOR)
Timer interrupt enable register (TIER)	Timer interrupt enable register (TIER)
Timer status register (TSR)	Timer status register (TSR)
Timer counter (TCNT)	Timer counter (TCNT)
Timer general register (TGR)	Timer general register (TGR)
Timer start register (TSTR)	Timer start register (TSTR)
Timer synchronous register (TSYR)	Timer synchronous register (TSYR)
Noise filter control register (NFCR)	Not available

Table 2.2 lists the points of difference between the TPU registers of the RX231 Group and H8S/2378 Group.

Points of difference between registers with equivalent functions, among the registers listed in Table 2.1, are listed. Registers and bit functions not listed in Table 2.2 are identical on the RX231 Group and H8S/2378 Group.

Table 2.2 Points of Difference between TPU Registers of H8S/2378 Group and RX231 Group

	Bit Name		Description	
Register Name	RX (RX231)	H8S (H8S/2378)	RX (RX231)	H8S (H8S/2378)
Timer control register (TCR)	CKEG[1:0]	CKEG1 CKEG0	Input clock edge select bits These bits select the input clock edge. When the internal clock is counted using both edges, the input clock period is halved (e.g., both edges of PCLK/4 = rising edge of PCLK/2). Internal clock edge selection is valid when the input clock is PCLK/4 or slower. This setting is ignored if the input clock is PCLK/1, or when overflow or underflow of another channel is selected. Input clock: Internal clock 00: Count at falling edge. 01: Count at rising edge. 10: Count at both edges. 11: Count at both edges. Input clock: External clock 00: Count at rising edge. 01: Count at falling edge. 10: Count at both edges. 11: Count at both edges.	Clock edge 1 and 0 These bits select the input clock edge. When the internal clock is counted using both edges, the input clock period is halved (e.g., both edges of ϕ/4 = rising edge of ϕ/2). If phase counting mode is used on channels 1, 2, 4, and 5, this setting is ignored and the phase counting mode setting has priority. Internal clock edge selection is valid when the input clock is ϕ/4 or slower. This setting is ignored if the input clock is ϕ/1, or when overflow or underflow of another channel is selected. 00: Count at rising edge. 01: Count at falling edge. 1X: Count at both edges. X: Don't care
Timer mode register (TMDR)	ICSELD	Not available	TGRD input capture input select bit Selects the input capture input for the TPUm.TGRD register (m = 0 or 3). This function allows measurement of the high-level width and period of the input pulse on a TIOCCn input pin. 0: Input capture input source is TIOCDn pin. 1: Input capture input source is TIOCCn pin. (n = 0 or 3)	—
Timer mode register (TMDR)	ICSELB	Not available	TGRB input capture input select bit Selects the input capture input for the TPUm.TGRB register (m = 0 to 5). This function allows measurement of the high-level width and period of the input pulse on a TIOCAn input pin. 0: Input capture input source is TIOCBn pin. 1: Input capture input source is TIOCAn pin. (n = 0 to 5)	—

Register Name		Bit Name RX (RX231)	Bit Name H8S (H8S/2378)	Description RX (RX231)	Description H8S (H8S/2378)
Timer I/O control register (TIOR)	Channel 0 TIORH	IOB[3:0]	IOB3 IOB2 IOB1 IOB0	TGRB register control bits 0000: Output prohibited 0001: Initial output is low; low output at compare match. 0010: Initial output is low; high output at compare match. 0011: Initial output is low; toggle output at compare match. 0100: Output prohibited 0101: Initial output is high; low output at compare match. 0110: Initial output is high; high output at compare match. 0111: Initial output is high; toggle output at compare match. 1000: Capture input source is TIOCB0/TIOCA0 pin; input capture at rising edge. 1001: Capture input source is TIOCB0/TIOCA0 pin; input capture at falling edge. 101X: Capture input source is TIOCB0/TIOCA0 pin; input capture at both edges. 11XX: Capture input source is TPU1 count clock; input capture at TPU1.TCNT count-up/count-down. X: Don’t care	I/O control B3 to B0 0000: Output prohibited 0001: Initial output is 0 output; 0 output at compare match. 0010: Initial output is 0 output; 1 output at compare match. 0011: Initial output is 0 output; toggle output at compare match. 0100: Output prohibited 0101: Initial output is 1 output; 0 output at compare match. 0110: Initial output is 1 output; 1 output at compare match. 0111: Initial output is 1 output; toggle output at compare match. 1000: Capture input source is TIOCB0 pin; input capture at rising edge. 1001: Capture input source is TIOCB0 pin; input capture at falling edge. 101X: Capture input source is TIOCB0 pin; input capture at both edges. 11XX: Capture input source is channel 1/count clock; input capture at TCNT_1 count-up/count-down. X: Don’t care

Register Name		Bit Name RX (RX231)	Bit Name H8S (H8S/2378)	Description RX (RX231)	Description H8S (H8S/2378)
Timer I/O control register (TIOR)	Channel 0 TIORL	IOD[3:0]	IOD3 IOD2 IOD1 IOD0	TGRD register control bits 0000: Output prohibited 0001: Initial output is low; low output at compare match. 0010: Initial output is low; high output at compare match. 0011: Initial output is low; toggle output at compare match. 0100: Output prohibited 0101: Initial output is high; low output at compare match. 0110: Initial output is high; high output at compare match. 0111: Initial output is high; toggle output at compare match. 1000: Capture input source is TIOCD0/TIOCC0 pin; input capture at rising edge. 1001: Capture input source is TIOCD0/TIOCC0 pin; input capture at falling edge. 101X: Capture input source is TIOCD0/TIOCC0 pin; input capture at both edges. 11XX: Capture input source is TPU1 count clock; input capture at TPU1.TCNT count-up/count-down. X: Don’t care	I/O control D3 to D0 0000: Output prohibited 0001: Initial output is 0 output; 0 output at compare match. 0010: Initial output is 0 output; 1 output at compare match. 0011: Initial output is 0 output; toggle output at compare match. 0100: Output prohibited 0101: Initial output is 1 output; 0 output at compare match. 0110: Initial output is 1 output; 1 output at compare match. 0111: Initial output is 1 output; toggle output at compare match. 1000: Capture input source is TIOCD0 pin; input capture at rising edge. 1001: Capture input source is TIOCD0 pin; input capture at falling edge. 101X: Capture input source is TIOCD0 pin; input capture at both edges. 11XX: Capture input source is channel 1/count clock; input capture at TCNT_1 count-up/count-down. X: Don’t care

Register Name		Bit Name RX (RX231)	Bit Name H8S (H8S/2378)	Description RX (RX231)	Description H8S (H8S/2378)
Timer I/O control register (TIOR)	Channel 1 TIOR	IOB[3:0]	IOB3 IOB2 IOB1 IOB0	TGRB register control bits 0000: Output prohibited 0001: Initial output is low; low output at compare match. 0010: Initial output is low; high output at compare match. 0011: Initial output is low; toggle output at compare match. 0100: Output prohibited 0101: Initial output is high; low output at compare match. 0110: Initial output is high; high output at compare match. 0111: Initial output is high; toggle output at compare match. 1000: Capture input source is TIOCB1/TIOCA1 pin; input capture at rising edge. 1001: Capture input source is TIOCB1/TIOCA1 pin; input capture at falling edge. 101X: Capture input source is TIOCB1/TIOCA1 pin; input capture at both edges. 11XX: Capture input source is TPU0.TGRC register compare match/input capture; input capture at generation of TPU0.TGRC register compare match/input capture. X: Don’t care	I/O control B3 to B0 0000: Output prohibited 0001: Initial output is 0 output; 0 output at compare match. 0010: Initial output is 0 output; 1 output at compare match. 0011: Initial output is 0 output; toggle output at compare match. 0100: Output prohibited 0101: Initial output is 1 output; 0 output at compare match. 0110: Initial output is 1 output; 1 output at compare match. 0111: Initial output is 1 output; toggle output at compare match. 1000: Capture input source is TIOCB1 pin; input capture at rising edge. 1001: Capture input source is TIOCB1 pin; input capture at falling edge. 101X: Capture input source is TIOCB1 pin; input capture at both edges. 11XX: Capture input source is TGRC_0 compare match/input capture; input capture at generation of TGRC_0 compare match/input capture. X: Don’t care

Register Name		Bit Name RX (RX231)	Bit Name H8S (H8S/2378)	Description RX (RX231)	Description H8S (H8S/2378)
Timer I/O control register (TIOR)	Channel 2 TIOR	IOB[3:0]	IOB3 IOB2 IOB1 IOB0	TGRB register control bits 0000: Output prohibited 0001: Initial output is low; low output at compare match. 0010: Initial output is low; high output at compare match. 0011: Initial output is low; toggle output at compare match. 0100: Output prohibited 0101: Initial output is high; low output at compare match. 0110: Initial output is high; high output at compare match. 0111: Initial output is high; toggle output at compare match. 1X00: Capture input source is TIOCB2/TIOCA2 pin; input capture at rising edge. 1X01: Capture input source is TIOCB2/TIOCA2 pin; input capture at falling edge. 1X1X: Capture input source is TIOCB2/TIOCA2; input capture at both edges. X: Don’t care	I/O control B3 to B0 0000: Output prohibited 0001: Initial output is 0 output; 0 output at compare match. 0010: Initial output is 0 output; 1 output at compare match. 0011: Initial output is 0 output; toggle output at compare match. 0100: Output prohibited 0101: Initial output is 1 output; 0 output at compare match. 0110: Initial output is 1 output; 1 output at compare match. 0111: Initial output is 1 output; toggle output at compare match. 1X00: Capture input source is TIOCB2 pin; input capture at rising edge. 1X01: Capture input source is TIOCB2 pin; input capture at falling edge. 1X1X: Capture input source is TIOCB2; input capture at both edges. X: Don’t care

Register Name		Bit Name RX (RX231)	Bit Name H8S (H8S/2378)	Description RX (RX231)	Description H8S (H8S/2378)
Timer I/O control register (TIOR)	Channel 3 TIORH	IOB[3:0]	IOB3 IOB2 IOB1 IOB0	TGRB register control bits 0000: Output prohibited 0001: Initial output is low; low output at compare match. 0010: Initial output is low; high output at compare match. 0011: Initial output is low; toggle output at compare match. 0100: Output prohibited 0101: Initial output is high; low output at compare match. 0110: Initial output is high; high output at compare match. 0111: Initial output is high; toggle output at compare match. 1000: Capture input source is TIOCB3/TIOCA3 pin; input capture at rising edge. 1001: Capture input source is TIOCB3/TIOCA3 pin; input capture at falling edge. 101X: Capture input source is TIOCB3/TIOCA3 pin; input capture at both edges. 11XX: Capture input source is TPU4 count clock; input capture at TPU4.TCNT count-up/count-down. X: Don’t care	I/O control B3 to B0 0000: Output prohibited 0001: Initial output is 0 output; 0 output at compare match. 0010: Initial output is 0 output; 1 output at compare match. 0011: Initial output is 0 output; toggle output at compare match. 0100: Output prohibited 0101: Initial output is 1 output; 0 output at compare match. 0110: Initial output is 1 output; 1 output at compare match. 0111: Initial output is 1 output; toggle output at compare match. 1000: Capture input source is TIOCB3 pin; input capture at rising edge. 1001: Capture input source is TIOCB3 pin; input capture at falling edge. 101X: Capture input source is TIOCB3 pin; input capture at both edges. 11XX: Capture input source is channel 4/count clock; input capture at TCNT_4 count-up/count-down. X: Don’t care

Register Name		Bit Name RX (RX231)	Bit Name H8S (H8S/2378)	Description RX (RX231)	Description H8S (H8S/2378)
Timer I/O control register (TIOR)	Channel 3 TIORL	IOD[3:0]	IOD3 IOD2 IOD1 IOD0	TGRD register control bits 0000: Output prohibited 0001: Initial output is low; low output at compare match. 0010: Initial output is low; high output at compare match. 0011: Initial output is low; toggle output at compare match. 0100: Output prohibited 0101: Initial output is high; low output at compare match. 0110: Initial output is high; high output at compare match. 0111: Initial output is high; toggle output at compare match. 1000: Capture input source is TIOCD3/TIOCC3 pin; input capture at rising edge. 1001: Capture input source is TIOCD3/TIOCC3 pin; input capture at falling edge. 101X: Capture input source is TIOCD3/TIOCC3 pin; input capture at both edges. 11XX: Capture input source is TPU4 count clock; input capture at TPU4.TCNT count-up/count-down. X: Don’t care	I/O control D3 to D0 0000: Output prohibited 0001: Initial output is 0 output; 0 output at compare match. 0010: Initial output is 0 output; 1 output at compare match. 0011: Initial output is 0 output; toggle output at compare match. 0100: Output prohibited 0101: Initial output is 1 output; 0 output at compare match. 0110: Initial output is 1 output; 1 output at compare match. 0111: Initial output is 1 output; toggle output at compare match. 1000: Capture input source is TIOCD3 pin; input capture at rising edge. 1001: Capture input source is TIOCD3 pin; input capture at falling edge. 101X: Capture input source is TIOCD3 pin; input capture at both edges. 11XX: Capture input source is channel 4/count clock; input capture at TCNT_4 count-up/count-down. X: Don’t care

Register Name		Bit Name RX (RX231)	Bit Name H8S (H8S/2378)	Description RX (RX231)	Description H8S (H8S/2378)
Timer I/O control register (TIOR)	Channel 4 TIOR	IOB[3:0]	IOB3 IOB2 IOB1 IOB0	TGRB register control bits 0000: Output prohibited 0001: Initial output is low; low output at compare match. 0010: Initial output is low; high output at compare match. 0011: Initial output is low; toggle output at compare match. 0100: Output prohibited 0101: Initial output is high; low output at compare match. 0110: Initial output is high; high output at compare match. 0111: Initial output is high; toggle output at compare match. 1000: Capture input source is TIOCB4/TIOCA4 pin; input capture at rising edge. 1001: Capture input source is TIOCB4/TIOCA4 pin; input capture at falling edge. 101X: Capture input source is TIOCB4/TIOCA4 pin; input capture at both edges. 11XX: Capture input source is TPU3.TGRC register compare match/input capture; input capture at generation of TPU3.TGRC register compare match/input capture. X: Don’t care	I/O control B3 to B0 0000: Output prohibited 0001: Initial output is 0 output; 0 output at compare match. 0010: Initial output is 0 output; 1 output at compare match. 0011: Initial output is 0 output; toggle output at compare match. 0100: Output prohibited 0101: Initial output is 1 output; 0 output at compare match. 0110: Initial output is 1 output; 1 output at compare match. 0111: Initial output is 1 output; toggle output at compare match. 1000: Capture input source is TIOCB4 pin; input capture at rising edge. 1001: Capture input source is TIOCB4 pin; input capture at falling edge. 101X: Capture input source is TIOCB4 pin; input capture at both edges. 11XX: Capture input source is TGRC_3 compare match/input capture; input capture at generation of TGRC_3 compare match/input capture. X: Don’t care

Register Name		Bit Name RX (RX231)	Bit Name H8S (H8S/2378)	Description RX (RX231)	Description H8S (H8S/2378)
Timer I/O control register (TIOR)	Channel 5 TIOR	IOB[3:0]	IOB3 IOB2 IOB1 IOB0	TGRB register control bits 0000: Output prohibited 0001: Initial output is low; low output at compare match. 0010: Initial output is low; high output at compare match. 0011: Initial output is low; toggle output at compare match. 0100: Output prohibited 0101: Initial output is high; low output at compare match. 0110: Initial output is high; high output at compare match. 0111: Initial output is high; toggle output at compare match. 1X00: Capture input source is TIOCB5/TIOCA5 pin; input capture at rising edge. 1X01: Capture input source is TIOCB5/TIOCA5 pin; input capture at falling edge. 1X1X: Capture input source is TIOCB5/TIOCA5 pin; input capture at both edges. X: Don’t care	I/O control B3 to B0 0000: Output prohibited 0001: Initial output is 0 output; 0 output at compare match. 0010: Initial output is 0 output; 1 output at compare match. 0011: Initial output is 0 output; toggle output at compare match. 0100: Output prohibited 0101: Initial output is 1 output; 0 output at compare match. 0110: Initial output is 1 output; 1 output at compare match. 0111: Initial output is 1 output; toggle output at compare match. 1X00: Capture input source is TIOCB5 pin; input capture at rising edge. 1X01: Capture input source is TIOCB5 pin; input capture at falling edge. 1X1X: Capture input source is TIOCB5 pin; input capture at both edges. X: Don’t care

Register Name	Bit Name RX (RX231)	Bit Name H8S (H8S/2378)	Description RX (RX231)	Description H8S (H8S/2378)
Timer status register (TSR)	TCFU		Underflow flag Status flag that indicates that TPUm.TCNT (m = 1, 2, 4, or 5) underflow has occurred. [Setting condition] • When the TPUm.TCNT value underflows (0000h → FFFFh) [Clearing condition] • When 0 is written to the TCFU flag after reading TCFU as 1	Underflow flag Status flag that indicates that TCNT underflow has occurred on channel 1, 2, 4, or 5 in phase counting mode. [Setting condition] • When the TCNT value underflows (0000h → FFFFh) [Clearing condition] • When 0 is written to TCFU after reading TCFU as 1
	TGFA		Input capture /output compare flag A [Setting conditions] • When TPUm.TCNT = TPUm.TGRA while TPUm.TGRA is functioning as an output compare register • When the TPUm.TCNT value is transferred to TPUm.TGRA by an input capture signal while TPUm.TGRA is functioning as an input capture register [Clearing conditions] • When the DTC is activated by a TGImA interrupt while the DTC.MRB.DISEL bit is cleared to 0 • When 0 is written to the TGFA flag after reading TGFA as 1	Input capture /output compare flag A [Setting conditions] • When TCNT = TGRA while TGRA is functioning as an output compare register • When the TCNT value is transferred to TGRA by an input capture signal while TGRA is functioning as an input capture register [Clearing conditions] • When the DTC is activated by a TGIA interrupt while the DISEL bit in MRB of the DTC is cleared to 0 • When the DMAC is activated by a TGIA interrupt while the DTE bit in DMABCR of the DMAC is cleared to 0 • When 0 is written to TGFA after reading TGFA as 1

2.2 Waveform Output Operation Using Compare Match

Points of difference in compare match operation on the RX231 Group and H8S/2378 Group are described below.

Table 2.3 lists preconditions for compare match operation on the RX231 Group and H8S/2378 Group.

Table 2.3 Conditions for Compare Match Operation

	Operation Conditions	
Item	**RX (RX231)**	**H8S (H8S/2378)**
Peripheral function operating clock	PCLKB: 24 MHz	ϕ: 20 MHz
Channels used	TPU0	Channel 3 of TPU
Pins used	TIOCA0: PA0 TIOCB0: P17	TIOCA3: P20 TIOCB3: P21
Clearing of TCNT register	None (free-running count operation)	
Pin output	High output at compare match A Low output at compare match B	

2.2.1 Operation

Figure 2.1 shows an example of waveform output operation on the H8S/2378 Group and RX231 Group.

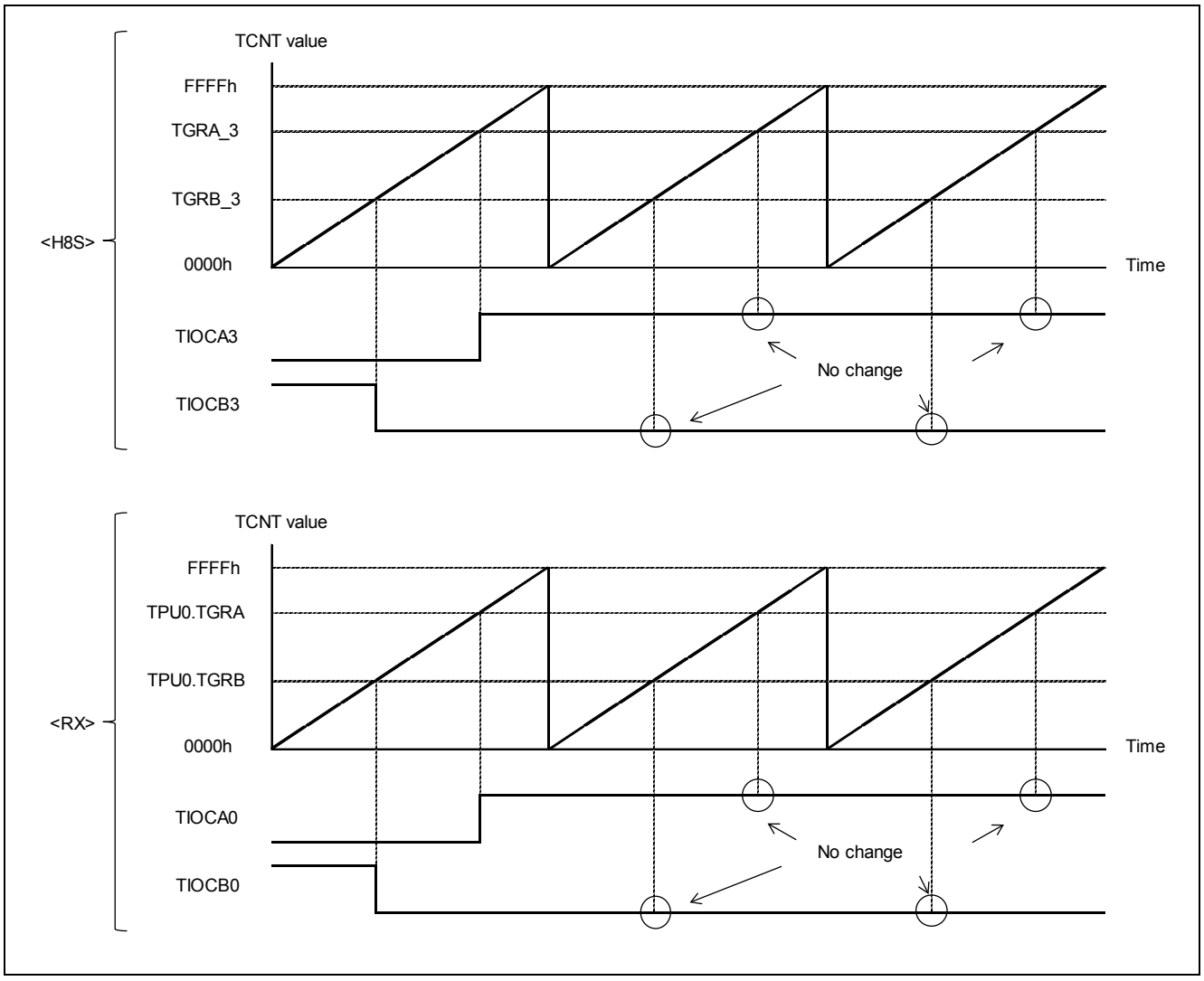

Figure 2.1 Example of Waveform Output Operation on H8S/2378 Group and RX231 Group

2.2.2 Points of Difference in Setting Procedure

Table 2.4 lists points of difference in the initial setting procedure for compare match operation. The initial setting procedure for the H8S/2378 Group is that used for interrupt control mode 2.

If interrupts are used, interrupt settings are required.

Table 2.4 lists the setting procedure when interrupts are used.

Table 2.4 Points of Difference in Initial Setting Procedure for Compare Match Operation

Procedure		RX (RX231)	H8S (H8S/2378)
1	Cancel the module stop state.*1	SYSTEM.PRCR.WORD = 0xA502; MSTP(TPU) = 0; SYSTEM.PRCR.WORD = 0xA500;	MSTPCR.BIT._TPU = 0;
2	Disable interrupts.	IEN(TPU0,TGIA0) = 0; IEN(TPU0,TGIB0) = 0; TPU0.TIER.BIT.TGIEA = 0; TPU0.TIER.BIT.TGIEB = 0;	TPU3.TIER.BIT.TGIEA = 0; TPU3.TIER.BIT.TGIEB = 0;
3	Stop count operation.	TPU.TSTR.BIT.CST0 = 0;	TPU.TSTR.BIT.CST3 = 0;
4	Clear counter.	TPU0.TCNT = 0x0000;	TPU3.TCNT= 0x0000;
5	Make I/O port function settings.*2	PORTA.PMR.BIT.B0 = 0; PORT1.PMR.BIT.B7 = 0; PORTA.PDR.BIT.B0 = 0; PORT1.PDR.BIT.B7 = 0; MPC.PWPR.BIT.B0WI = 0; MPC.PWPR.BIT.PFSWE = 1; MPC.PA0PFS.BYTE = 0x03; MPC.P17PFS.BYTE = 0x03; MPC.PWPR.BIT.PFSWE = 0; MPC.PWPR.BIT.B0WI = 1; PORTA.PMR.BIT.B0 = 1; PORT1.PMR.BIT.B7 = 1;	— (No processing)
6	Make count clock setting.	TPU0.TCR.BIT.TPSC = 000b;	TPU3.TCR.BIT.TPSC = 000b;
7	Make counter clear setting.	TPU0.TCR.BIT.CCLR = 000b;	TPU3.TCR.BIT.CCLR = 000b;
8	Make operation mode setting.	TPU0.TMDR.BIT.MD = 0000b;	TPU3.TMDR.BIT.MD = 0000b;
9	Set counter to independent operation.	TPU.TSYR.BIT.SYNC0 = 0;	TPU.TSYR.BIT.SYNC3 = 0;
10	Make waveform output mode settings.	TPU0.TIORH.BIT.IOA = 0010b; TPU0.TIORH.BIT.IOB = 0101b;	TPU3.TIOR.BIT.IOA = 0010b; TPU3.TIOR.BIT.IOB = 0101b;
11	Make output timing settings.	TPU0.TGRA = 0xC000; TPU0.TGRB = 0x4000;	TPU3.TGRA = 0xC000; TPU3.TGRB = 0x4000;
12	Make interrupt control mode setting.*3	— (No processing)	INTC.INTCR.BIT.INTM = 10b;
13	Make interrupt priority level setting.*4	IPR(TPU0,TGIA0) = 0x01; IPR(TPU0,TGIB0) = 0x01;	INTC.IPRG.BIT._TPU3 = 001b;
14	Clear peripheral function interrupt requests.	TPU0.TSR.BIT.TGFA = 0; TPU0.TSR.BIT.TGFB = 0;	TPU3.TSR.BIT.TGFA = 0; TPU3.TSR.BIT.TGFB = 0;
15	Clear interrupt requests.	IR(TPU0,TGIA0) = 0; IR(TPU0,TGIB0) = 0;	— (No processing)
16	Enable peripheral function interrupt requests.	TPU0.TIER.BIT.TGIEA = 1; TPU0.TIER.BIT.TGIEB = 1;	TPU3.TIER.BIT.TGIEA = 1; TPU3.TIER.BIT.TGIEB = 1;

Procedure		RX (RX231)	H8S (H8S/2378)
17	Enable interrupt requests.*[5]	IEN(TPU0,TGIA0) = 1; IEN(TPU0,TGIB0) = 1;	— (No processing)
18	Make processor interrupt priority level setting.	— (No processing)	set_imask_exr(0);
19	Enable maskable interrupts.	setpsw_i();	— (No processing)
20	Start count operation.	TPU.TSTR.BIT.CST0 = 1;	TPU.TSTR.BIT.CST3 = 1;

Note 1. For information on the module stop function, refer to section 5, Module Stop Function.

Note 2. On the RX231 Group peripheral function pin settings are made in the MPC. For details, refer to 7.1, I/O Ports.

Note 3. The RX231 Group has no interrupt control mode. For details, refer to section 4, Points of Difference between Interrupts.

Note 4. For details of the interrupt priority level setting method, refer to section 4, Points of Difference between Interrupts.

Note 5. The methods of enabling interrupt requests differ. For details, refer to section 4, Points of Difference between Interrupts.

3. TPU to MTU Migration

3.1 Register Comparison

Table 3.1 lists the TPU registers of the H8S/2378 Group and the MTU registers of the RX231 Group.

The MTU functions of the RX231 Group differ among the channels. For details, refer to the section on multi-function timer pulse unit 2 (MTU2a) in User's Manual: Hardware.

Table 3.1 TPU Registers H8S/2378 Group and MTU Registers the RX231 Group

RX (RX231)	H8S (H8S/2378)
Timer control register (TCR)	Timer control register (TCR)
Timer mode register (TMDR)	Timer mode register (TMDR)
Timer I/O control register (TIOR)	Timer I/O control register (TIOR)
Timer compare match clear register (TCNTCMPCLR)	Not available
Timer interrupt enable register (TIER)	Timer interrupt enable register (TIER)
Timer status register (TSR)	Timer status register (TSR)
Timer buffer operation transfer mode register (TBTM)	Not available
Timer input capture control register (TICCR)	
Timer A/D converter start request control register (TADCR)	
Timer A/D converter start request cycle set registers A and B (TADCORA/TADCORB)	
Timer A/D converter start request cycle set buffer registers A and B (TADCOBRA/TADCOBRB)	
Timer counter (TCNT)	Timer counter (TCNT)
Timer general register (TGR)	Timer general register (TGR)
Timer start register (TSTR)	Timer start register (TSTR)
Timer synchronous register (TSYR)	Timer synchronous register (TSYR)
Timer read/Write enable register (TRWER)	Not available
Timer output master enable register (TOER)	
Timer output control register 1 (TOCR1)	
Timer output control register 2 (TOCR2)	
Timer output level buffer register (TOLBR)	
Timer gate control register (TGCR)	
Timer subcounter (TCNTS)	
Timer dead time data register (TDDR)	
Timer cycle data register (TCDR)	
Timer cycle buffer register (TCBR)	
Timer interrupt skipping set register (TITCR)	
Timer interrupt skipping counter (TITCNT)	
Timer buffer transfer set register (TBTER)	
Timer dead time enable register (TDER)	
Timer waveform control register (TWCR)	
Noise filter control register (NFCR)	

3.2 Peripheral Functions Used

Table 3.2 lists the peripheral functions and modes used in the TPU and MTU operation examples.

Table 3.2 Peripheral Functions and Modes Used in TPU and MTU Operation Examples

		RX (RX231)		H8S (H8S/2378)		
No.	Operation Example	Peripheral Function	Mode	Peripheral Function	Mode	Reference
1	Waveform output operation using compare match	MTU	Normal mode	TPU	Normal mode	3.3
2	Input capture operation					3.4
3	PWM mode 1		PWM mode 1		PWM mode 1	3.5
4	PWM mode 2		PWM mode 2		PWM mode 2	3.6

3.3 Waveform Output Operation Using Compare Match

Points of difference in compare match operation on the RX231 Group and H8S/2378 Group are described below.

Table 3.3 lists preconditions for compare match operation on the RX231 Group and H8S/2378 Group.

Table 3.3 Conditions for Compare Match Operation

	Operation Conditions	
Item	**RX (RX231)**	**H8S (H8S/2378)**
Peripheral function operating clock	PCLKA: 24 MHz	ϕ: 20 MHz
Channels used	MTU0	Channel 3 of TPU
Pins used	MTIOC0A: P34 MTIOC0B: P15	TIOCA3: P20 TIOCB3: P21
Clearing of TCNT register	None (free-running count operation)	
Pin output	High output at compare match A Low output at compare match B	

3.3.1 Operation

Figure 3.1 shows an example of waveform output operation on the H8S/2378 Group and RX231 Group.

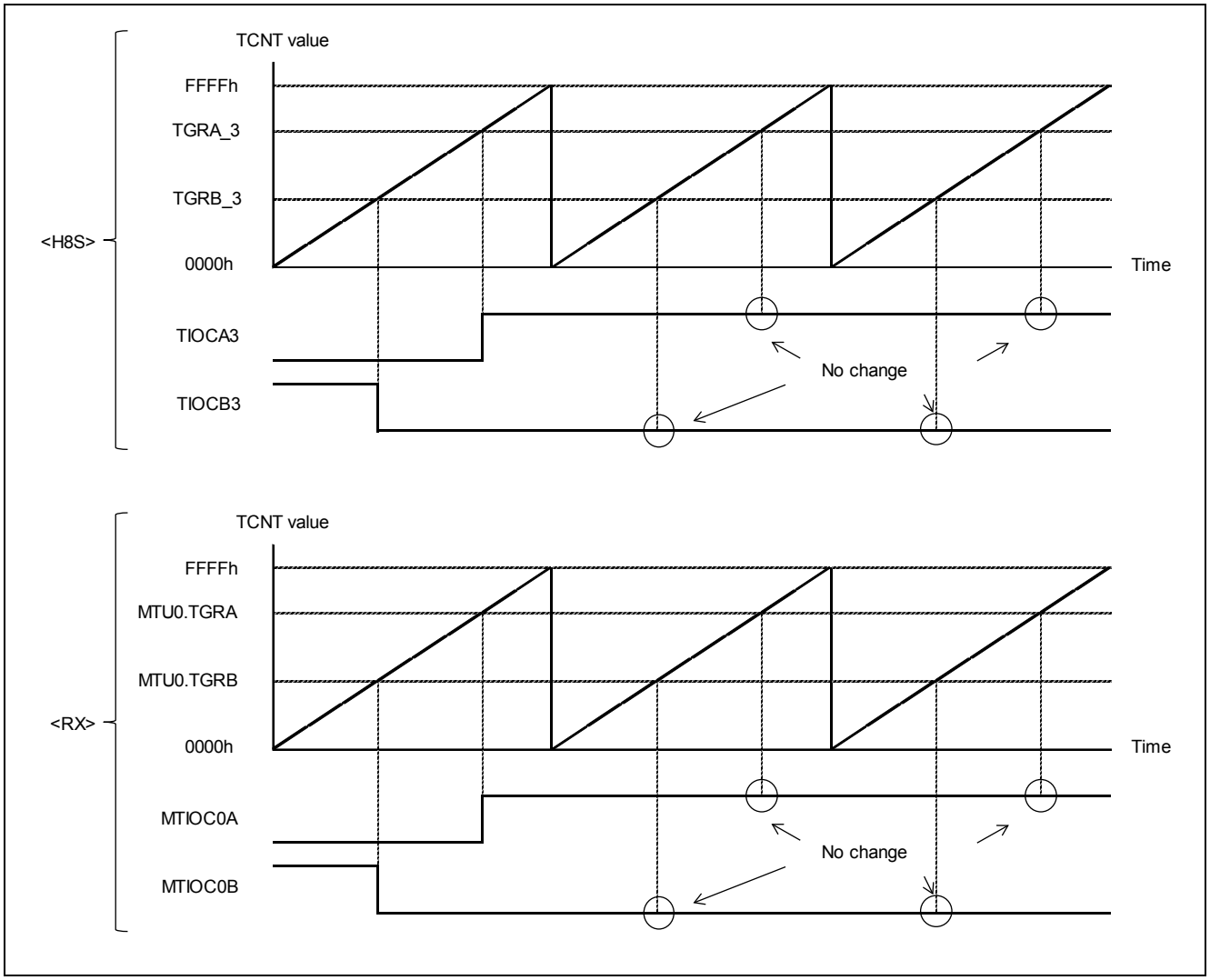

Figure 3.1 Example of Waveform Output Operation on H8S/2378 Group and RX231 Group

3.3.2 Points of Difference in Setting Procedure

Table 3.4 lists points of difference in the initial setting procedure for compare match operation. The initial setting procedure for the H8S/2378 Group is that used for interrupt control mode 2.

If interrupts are used, interrupt settings are required.

Table 3.4 lists the setting procedure when interrupts are used.

Table 3.4 Points of Difference in Initial Setting Procedure for Compare Match Operation

Procedure		RX (RX231)	H8S (H8S/2378)
1	Cancel the module stop state.*1	SYSTEM.PRCR.WORD = 0xA502; MSTP(MTU) = 0; SYSTEM.PRCR.WORD = 0xA500;	MSTPCR.BIT._TPU = 0;
2	Disable interrupts.	IEN(MTU0,TGIA0) = 0; IEN(MTU0,TGIB0) = 0; MTU0.TIER.BIT.TGIEA = 0; MTU0.TIER.BIT.TGIEB = 0;	TPU3.TIER.BIT.TGIEA = 0; TPU3.TIER.BIT.TGIEB = 0;
3	Stop count operation.	MTU.TSTR.BIT.CST0 = 0;	TPU.TSTR.BIT.CST3 = 0;
4	Clear counter.	MTU0.TCNT = 0x0000;	TPU3.TCNT= 0x0000;
5	Make I/O port function settings.*2	PORT3.PMR.BIT.B4 = 0; PORT1.PMR.BIT.B5 = 0; PORT3.PDR.BIT.B4 = 0; PORT1.PDR.BIT.B5 = 0; MPC.PWPR.BIT.B0WI = 0; MPC.PWPR.BIT.PFSWE = 1; MPC.P34PFS.BYTE = 0x01; MPC.P15PFS.BYTE = 0x01; MPC.PWPR.BIT.PFSWE = 0; MPC.PWPR.BIT.B0WI = 1; PORT3.PMR.BIT.B4 = 1; PORT1.PMR.BIT.B5 = 1;	— (No processing)
6	Make count clock setting.	MTU0.TCR.BIT.TPSC = 000b;	TPU3.TCR.BIT.TPSC = 000b;
7	Make counter clear setting.	MTU0.TCR.BIT.CCLR = 000b;	TPU3.TCR.BIT.CCLR = 000b;
8	Make operation mode setting.	MTU0.TMDR.BIT.MD = 0000b;	TPU3.TMDR.BIT.MD = 0000b;
9	Set counter to independent operation.	MTU.TSYR.BIT.SYNC0 = 0;	TPU.TSYR.BIT.SYNC3 = 0;
10	Make waveform output mode settings.	MTU0.TIORH.BIT.IOA = 0010b; MTU0.TIORH.BIT.IOB = 0101b;	TPU3.TIOR.BIT.IOA = 0010b; TPU3.TIOR.BIT.IOB = 0101b;
11	Make output timing settings.	MTU0.TGRA = 0xC000; MTU0.TGRB = 0x4000;	TPU3.TGRA = 0xC000; TPU3.TGRB = 0x4000;
12	Make interrupt control mode setting.*3	— (No processing)	INTC.INTCR.BIT.INTM = 10b;
13	Make interrupt priority level settings.*4	IPR(MTU0,TGIA0) = 0x01; IPR(MTU0,TGIB0) = 0x01;	INTC.IPRG.BIT._TPU3 = 001b;
14	Clear peripheral function interrupt requests.	— (No processing)*5	TPU3.TSR.BIT.TGFA = 0; TPU3.TSR.BIT.TGFB = 0;
15	Clear interrupt requests.	IR(MTU0,TGIA0) = 0; IR(MTU0,TGIB0) = 0;	— (No processing)
16	Enable peripheral function interrupt requests.	MTU0.TIER.BIT.TGIEA = 1; MTU0.TIER.BIT.TGIEB = 1;	TPU3.TIER.BIT.TGIEA = 1; TPU3.TIER.BIT.TGIEB = 1;

Procedure		RX (RX231)	H8S (H8S/2378)
17	Enable interrupt requests.*[6]	IEN(MTU0,TGIA0) = 1; IEN(MTU0,TGIB0) = 1;	— (No processing)
18	Make processor interrupt priority level setting.	— (No processing)	set_imask_exr(0);
19	Enable maskable interrupts.	setpsw_i();	— (No processing)
20	Start count operation.	MTU.TSTR.BIT.CST0 = 1;	TPU.TSTR.BIT.CST3 = 1;

Note 1. For information on the module stop function, refer to section 5, Module Stop Function.

Note 2. On the RX231 Group peripheral function pin settings are made in the MPC. For details, refer to 7.1, I/O Ports.

Note 3. The RX231 Group has no interrupt control mode. For details, refer to section 4, Points of Difference between Interrupts.

Note 4. For details of the interrupt priority level setting method, refer to section 4, Points of Difference between Interrupts.

Note 5. The MTU of the RX231 Group does not have interrupt request flags in peripheral functions. For details, refer to section 4, Points of Difference between Interrupts.

Note 6. The methods of enabling interrupt requests differ. For details, refer to section 4, Points of Difference between Interrupts.

3.4 Input Capture Operation

Points of difference in input capture operation on the RX231 Group and H8S/2378 Group are described below.

Table 3.5 lists preconditions for input capture operation on the RX231 Group and H8S/2378 Group.

Table 3.5 Conditions for Input Capture Operation

	Operation Conditions	
Item	**RX (RX231)**	**H8S (H8S/2378)**
Peripheral function operating clock	PCLKA: 24 MHz	ϕ: 20 MHz
Channels used	MTU0	Channel 3 of TPU
Pins used	MTIOC0A: P34 MTIOC0B: P15	TIOCA3: P20 TIOCB3: P21
Clearing of TCNT register	Clearing of counter at TGRB register input capture	
Input capture input edge	MTIOC0A pin: Both rising and falling edges MTIOC0B pin: Falling edge	TIOCA3 pin: Both rising and falling edges TIOCB3 pin: Falling edge
Noise filter function	Not used	Function not available

3.4.1 Operation

Figure 3.2 shows an example of input capture operation on the H8S/2378 Group and RX231 Group.

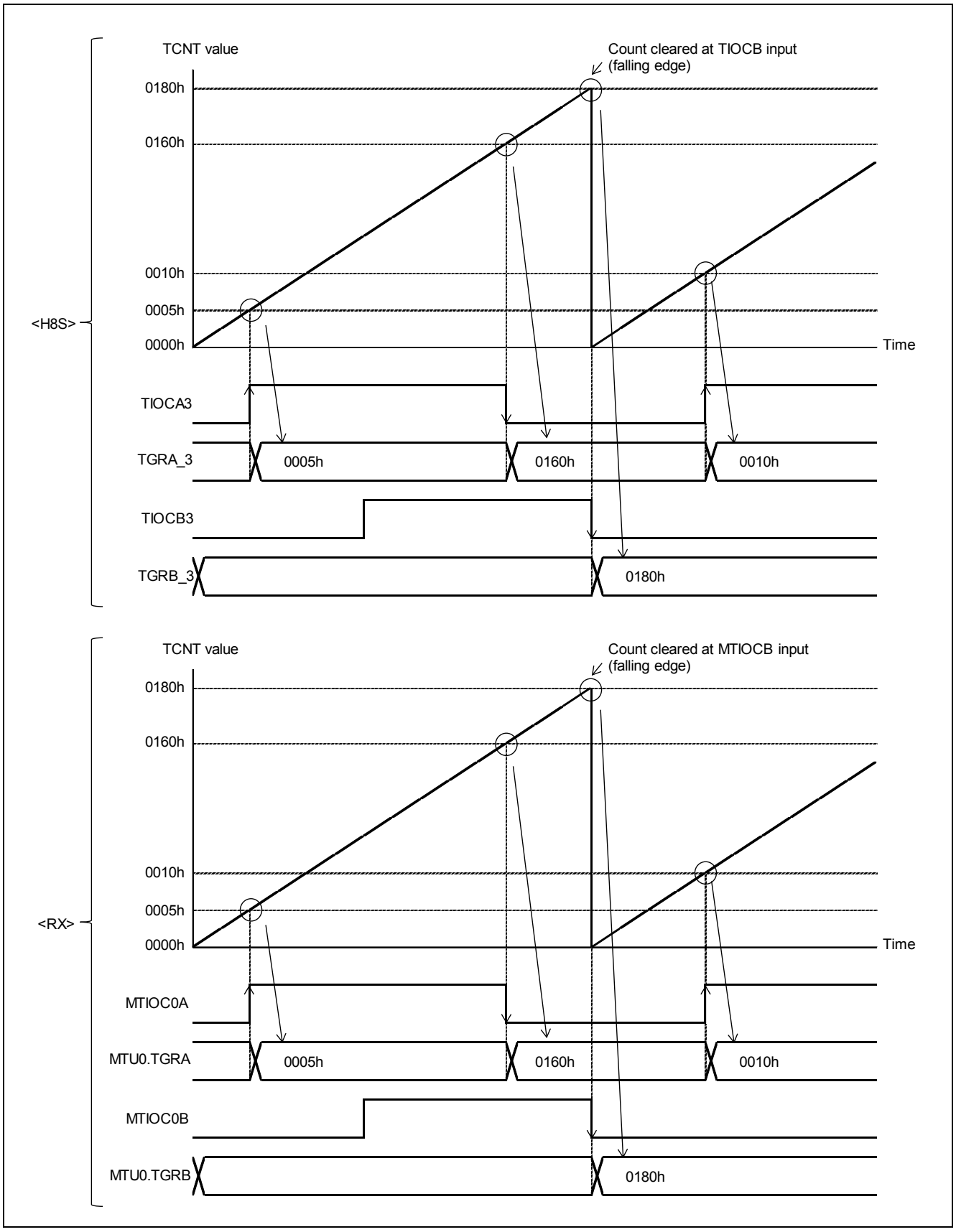

Figure 3.2 Example of Input Capture Operation on H8S/2378 Group and RX231 Group

3.4.2 Points of Difference in Setting Procedure

Table 3.6 lists points of difference in the initial setting procedure for input capture operation. The initial setting procedure for the H8S/2378 Group is that used for interrupt control mode 2.

If interrupts are used, interrupt settings are required.

Table 3.6 lists the setting procedure when interrupts are used.

Table 3.6 Points of Difference in Initial Setting Procedure for Input Capture Operation

Procedure		RX (RX231)	H8S (H8S/2378)
1	Cancel the module stop state.*1	SYSTEM.PRCR.WORD = 0xA502; MSTP(MTU) = 0; SYSTEM.PRCR.WORD = 0xA500;	MSTPCR.BIT._TPU = 0;
2	Disable interrupts.	IEN(MTU0,TGIA0) = 0; IEN(MTU0,TGIB0) = 0; MTU0.TIER.BIT.TGIEA = 0; MTU0.TIER.BIT.TGIEB = 0;	TPU3.TIER.BIT.TGIEA = 0; TPU3.TIER.BIT.TGIEB = 0;
3	Stop count operation.	MTU.TSTR.BIT.CST0 = 0;	TPU.TSTR.BIT.CST3 = 0;
4	Clear counter.	MTU0.TCNT = 0x0000;	TPU3.TCNT= 0x0000;
5	Make I/O port function settings.*2	PORT3.PMR.BIT.B4 = 0; PORT1.PMR.BIT.B5 = 0; PORT3.PDR.BIT.B4 = 0; PORT1.PDR.BIT.B5 = 0; MPC.PWPR.BIT.B0WI = 0; MPC.PWPR.BIT.PFSWE = 1; MPC.P34PFS.BYTE = 0x01; MPC.P15PFS.BYTE = 0x01; MPC.PWPR.BIT.PFSWE = 0; MPC.PWPR.BIT.B0WI = 1; PORT3.PMR.BIT.B4 = 1; PORT1.PMR.BIT.B5 = 1;	— (No processing)
6	Make noise filter function settings.*3	MTU0.NFCR.BIT.NFAEN = 0; MTU0.NFCR.BIT.NFBEN = 0;	— (No processing)
7	Make count clock setting.	MTU0.TCR.BIT.TPSC = 000b;	TPU3.TCR.BIT.TPSC = 000b;
8	Make counter clear setting.	MTU0.TCR.BIT.CCLR = 010b;	TPU3.TCR.BIT.CCLR = 010b;
9	Make operation mode setting.	MTU0.TMDR.BIT.MD = 0000b;	TPU3.TMDR.BIT.MD = 0000b;
10	Set counter to independent operation.	MTU.TSYR.BIT.SYNC0 = 0;	TPU.TSYR.BIT.SYNC3 = 0;
11	Make input capture input settings.	MTU0.TIORH.BIT.IOA = 1010b; MTU0.TIORH.BIT.IOB = 1001b;	TPU3.TIOR.BIT.IOA = 1010b; TPU3.TIOR.BIT.IOB = 1001b;
12	Make interrupt control mode setting.*4	— (No processing)	INTC.INTCR.BIT.INTM = 10b;
13	Make interrupt priority level settings.*4	IPR(MTU0,TGIA0) = 0x01; IPR(MTU0,TGIB0) = 0x01;	INTC.IPRG.BIT._TPU3 = 001b;
14	Clear peripheral function interrupt requests.	— (No processing)*6	TPU3.TSR.BIT.TGFA = 0; TPU3.TSR.BIT.TGFB = 0;
15	Clear interrupt requests.	IR(MTU0,TGIA0) = 0; IR(MTU0,TGIB0) = 0;	— (No processing)
16	Enable peripheral function interrupt requests.	MTU0.TIER.BIT.TGIEA = 1; MTU0.TIER.BIT.TGIEB = 1;	TPU3.TIER.BIT.TGIEA = 1; TPU3.TIER.BIT.TGIEB = 1;

Procedure		RX (RX231)	H8S (H8S/2378)
17	Enable interrupt requests.*[7]	IEN(MTU0,TGIA0) = 1; IEN(MTU0,TGIB0) = 1;	— (No processing)
18	Make processor interrupt priority level setting.	— (No processing)	set_imask_exr(0);
19	Enable maskable interrupts.	setpsw_i();	— (No processing)
20	Start count operation.	MTU.TSTR.BIT.CST0 = 1;	TPU.TSTR.BIT.CST3 = 1;

Note 1. For information on the module stop function, refer to section 5, Module Stop Function.
Note 2. On the RX231 Group peripheral function pin settings are made in the MPC. For details, refer to 7.1, I/O Ports.
Note 3. For details of the noise filter function, refer to User's Manual: Hardware.
Note 4. The RX231 Group has no interrupt control mode. For details, refer to section 4, Points of Difference between Interrupts.
Note 5. For details of the interrupt priority level setting method, refer to section 4, Points of Difference between Interrupts.
Note 6. The MTU of the RX231 Group does not have interrupt request flags in peripheral functions. For details, refer to section 4, Points of Difference between Interrupts.
Note 7. The methods of enabling interrupt requests differ. For details, refer to section 4, Points of Difference between Interrupts.

3.5 PWM Mode 1

PWM mode 1 operation works basically the same way on the RX231 Group and H8S/2378 Group. Two pairs of registers — the TGRA and TGRB register, and the TGRC and TGRD register — are used to generate PWM output on the TIOCA (MTIOCA) pin and TIOCC (MTIOCC) pin.

Points of difference in PWM mode 1 operation on the RX231 Group and H8S/2378 Group are described below.

Table 3.7 lists the preconditions for PWM mode 1 operation on the RX231 Group and H8S/2378 Group.

Table 3.7 Conditions for PWM Mode 1 Operation

	Operation Conditions	
Item	**RX (RX231)**	**H8S (H8S/2378)**
Peripheral function operating clock	PCLKA: 24 MHz	ϕ: 20 MHz
Channels used	MTU0	Channel 3 of TPU
Pins used	MTIOC0A: P34	TIOCA3: P20
Clearing of TCNT register	Clearing of counter at TGRA compare match	
PWM output waveform	Frequency: 1kHz MTIOC0A: 70% duty, high output at TGRB compare match	Frequency: 1kHz TIOCA0: 70% duty, high output at TGRB compare match

3.5.1 Operation

Figure 3.3 shows an example of PWM mode 1 operation on the H8S/2378 Group and RX231 Group.

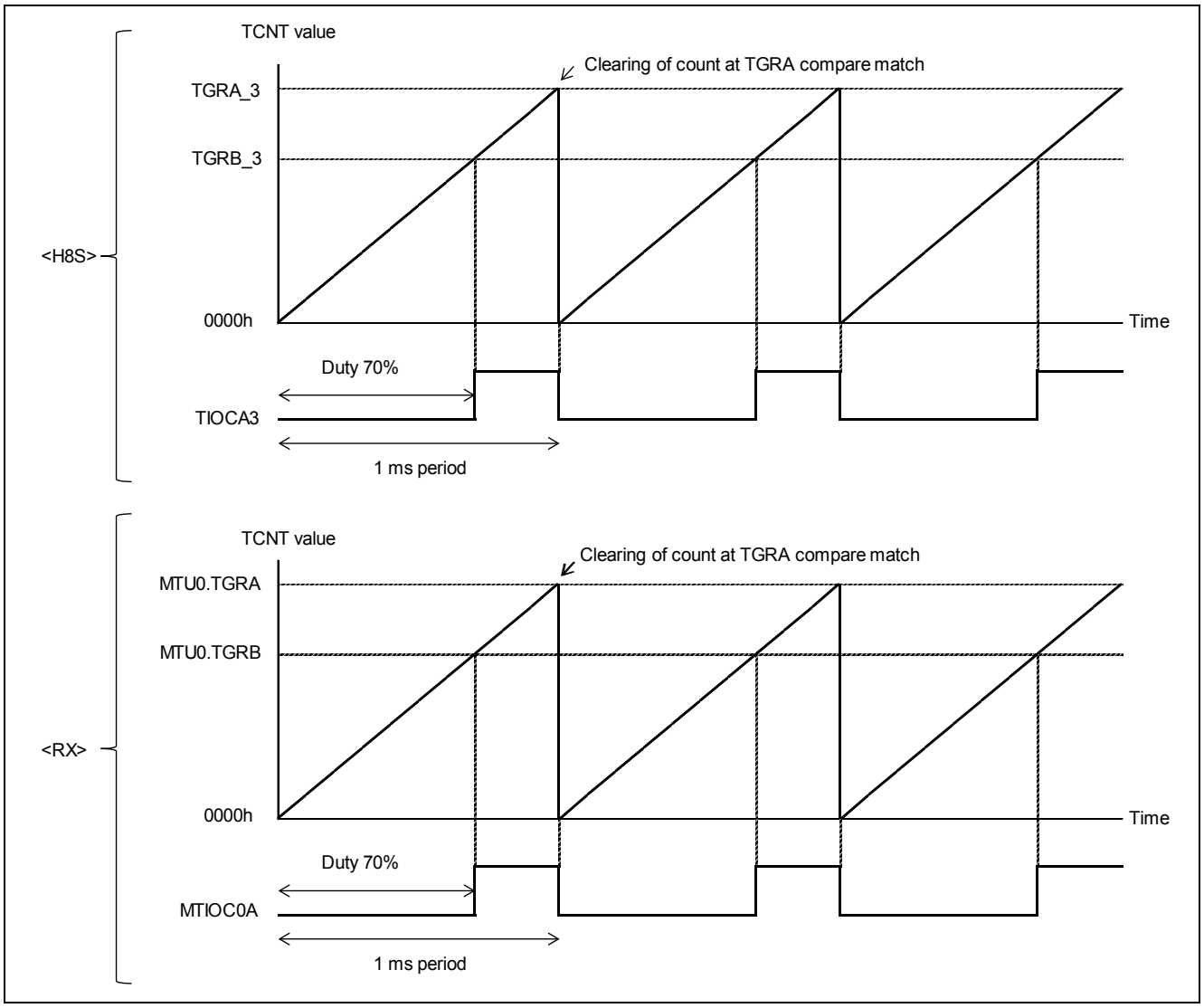

Figure 3.3 Example of PWM Mode 1 Operation on H8S/2378 Group and RX231 Group

3.5.2 Points of Difference in Setting Procedure

Table 3.8 lists points of difference in the initial setting procedure for PWM mode 1 operation. The initial setting procedure for the H8S/2378 Group is that used for interrupt control mode 2.

If interrupts are used, interrupt settings are required.

Table 3.8 lists the setting procedure when interrupts are used.

Table 3.8 Points of Difference in Initial Setting Procedure for PWM Mode 1 Operation

Procedure		RX (RX231)	H8S (H8S/2378)
1	Cancel the module stop state.*1	SYSTEM.PRCR.WORD = 0xA502; MSTP(MTU) = 0; SYSTEM.PRCR.WORD = 0xA500;	MSTPCR.BIT._TPU = 0;
2	Disable interrupts.	IEN(MTU0,TGIA0) = 0; IEN(MTU0,TGIB0) = 0; MTU0.TIER.BIT.TGIEA = 0; MTU0.TIER.BIT.TGIEB = 0;	TPU3.TIER.BIT.TGIEA = 0; TPU3.TIER.BIT.TGIEB = 0;
3	Stop count operation.	MTU.TSTR.BIT.CST0 = 0;	TPU.TSTR.BIT.CST3 = 0;
4	Clear counter.	MTU0.TCNT = 0x0000;	TPU3.TCNT= 0x0000;
5	Make I/O port function settings.*2	PORT3.PMR.BIT.B4 = 0; PORT3.PDR.BIT.B4 = 0; MPC.PWPR.BIT.B0WI = 0; MPC.PWPR.BIT.PFSWE = 1; MPC.P34PFS.BYTE = 0x01; MPC.PWPR.BIT.PFSWE = 0; MPC.PWPR.BIT.B0WI = 1; PORT3.PMR.BIT.B4 = 1;	— (No processing)
6	Make count clock setting.	MTU0.TCR.BIT.TPSC = 000b;	TPU3.TCR.BIT.TPSC = 000b;
7	Make counter clear setting.	MTU0.TCR.BIT.CCLR = 001b;	TPU3.TCR.BIT.CCLR = 001b;
8	Make operation mode setting.	MTU0.TMDR.BIT.MD = 0010b;	TPU3.TMDR.BIT.MD = 0010b;
9	Set counter to independent operation.	MTU.TSYR.BIT.SYNC0 = 0;	TPU.TSYR.BIT.SYNC3 = 0;
10	Make waveform output mode settings.	MTU0.TIORH.BIT.IOA = 0001b; MTU0.TIORH.BIT.IOB = 0010b;*3	TPU3.TIOR.BIT.IOA = 0001b; TPU3.TIOR.BIT.IOB = 0010b;*3
11	Make TGR register settings.	MTU0.TGRA = 0x5DBF; MTU0.TGRB = 0x419F;	TPU3.TGRA = 0x4E20; TPU3.TGRB = 0x36B0;
12	Make interrupt control mode setting.*4	— (No processing)	INTC.INTCR.BIT.INTM = 10b;
13	Make interrupt priority level settings.*5	IPR(MTU0,TGIA0) = 0x01; IPR(MTU0,TGIB0) = 0x01;	INTC.IPRG.BIT._TPU3 = 001b;
14	Clear peripheral function interrupt requests.	— (No processing)*6	TPU3.TSR.BIT.TGFA = 0; TPU3.TSR.BIT.TGFB = 0;
15	Clear interrupt requests.	IR(MTU0,TGIA0) = 0; IR(MTU0,TGIB0) = 0;	— (No processing)
16	Enable peripheral function interrupt requests.	MTU0.TIER.BIT.TGIEA = 1; MTU0.TIER.BIT.TGIEB = 1;	TPU3.TIER.BIT.TGIEA = 1; TPU3.TIER.BIT.TGIEB = 1;
17	Enable interrupt requests.*7	IEN(MTU0,TGIA0) = 1; IEN(MTU0,TGIB0) = 1;	— (No processing)
18	Make processor interrupt priority level setting.	— (No processing)	set_imask_exr(0);

Procedure		RX (RX231)	H8S (H8S/2378)
19	Enable maskable interrupts.	setpsw_i();	— (No processing)
20	Start count operation.	MTU.TSTR.BIT.CST0 = 1;	TPU.TSTR.BIT.CST3 = 1;

Note 1. For information on the module stop function, refer to section 5, Module Stop Function.

Note 2. On the RX231 Group peripheral function pin settings are made in the MPC. For details, refer to 7.1, I/O Ports.

Note 3. In PWM mode 1 the initial output value is the value set in the TGRA and TGRC registers. The initial output value set in the TIOR.IOB bit or TIORH.IOB and TIORL.IOD bits does not affect the output.

Note 4. The RX231 Group has no interrupt control mode. For details, refer to section 4, Points of Difference between Interrupts.

Note 5. For details of the interrupt priority level setting method, refer to section 4, Points of Difference between Interrupts.

Note 6. The MTU of the RX231 Group does not have interrupt request flags in peripheral functions. For details, refer to section 4, Points of Difference between Interrupts.

Note 7. The methods of enabling interrupt requests differ. For details, refer to section 4, Points of Difference between Interrupts.

3.6 PWM Mode 2

PWM mode 2 operation works basically the same way on the RX231 Group and H8S/2378 Group. One TGR register is used as a cycle register and the other TGR registers as duty registers to generate PWM output.

Points of difference in PWM mode 2 operation on the RX231 Group and H8S/2378 Group are described below.

Table 3.9 lists the preconditions for PWM mode 2 operation on the RX231 Group and H8S/2378 Group.

Table 3.9 Conditions for PWM Mode 2 Operation

	Operation Conditions	
Item	**RX (RX231)**	**H8S (H8S/2378)**
Peripheral function operating clock	PCLKA: 24 MHz	φ: 20 MHz
Channels used	MTU0	Channel 3 of TPU
Pins used	MTIOC0A: P34 MTIOC0B: P15 MTIOC0D: PA3	TIOCB3: P21 TIOCC3: P22 TIOCD3: P23
Clearing of TCNT register	Clearing of counter at TGRC compare match	Clearing of counter at TGRA compare match
PWM output waveform	Frequency: 1 kHz MTIOC0A: Duty 30% MTIOC0B: Duty 50% MTIOC0D: Duty 70%	Frequency: 1 kHz TIOCB3: Duty 30% TIOCC3: Duty 50% TIOCD3: Duty 70%

3.6.1 Operation

Figure 3.4 shows an example of PWM mode 2 operation on the H8S/2378 Group and RX231 Group.

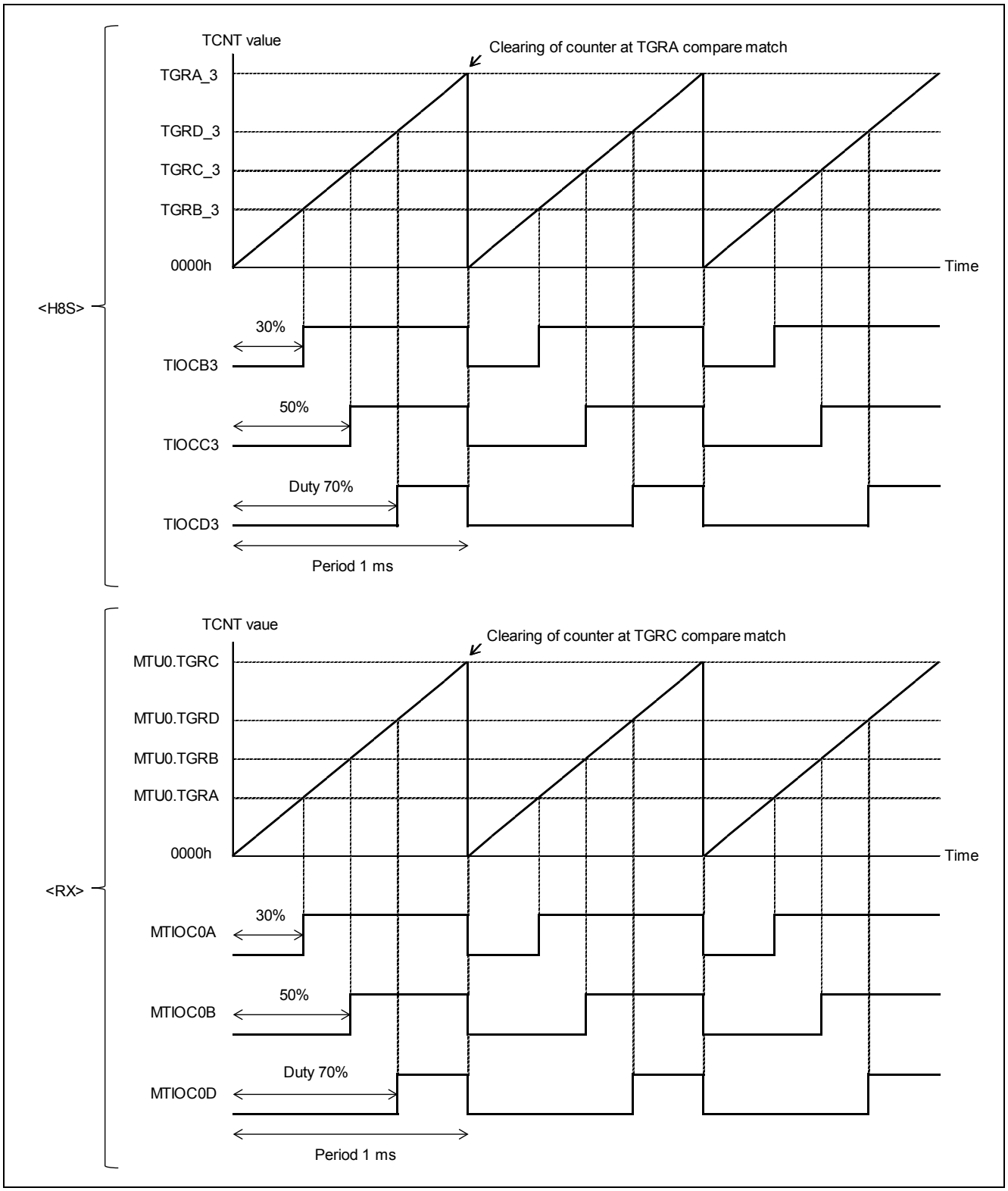

Figure 3.4 Example of PWM Mode 2 Operation on H8S/2378 Group and RX231 Group

3.6.2 Points of Difference in Setting Procedure

Table 3.10 lists points of difference in the initial setting procedure for PWM mode 2 operation. The initial setting procedure for the H8S/2378 Group is that used for interrupt control mode 2.

If interrupts are used, interrupt settings are required.

Table 3.10 lists the setting procedure when interrupts are used.

Table 3.10 Points of Difference in Initial Setting Procedure for PWM Mode 2 Operation

Procedure		RX (RX231)	H8S (H8S/2378)
1	Cancel the module stop state.*1	SYSTEM.PRCR.WORD = 0xA502; MSTP(MTU) = 0; SYSTEM.PRCR.WORD = 0xA500;	MSTPCR.BIT._TPU = 0;
2	Disable interrupts.	IEN(MTU0,TGIA0) = 0; IEN(MTU0,TGIB0) = 0; IEN(MTU0,TGIC0) = 0; IEN(MTU0.TGID0) = 0; MTU0.TIER.BIT.TGIEA = 0; MTU0.TIER.BIT.TGIEB = 0; MTU0.TIER.BIT.TGIEC = 0; MTU0.TIER.BIT.TGIED = 0;	TPU3.TIER.BIT.TGIEA = 0; TPU3.TIER.BIT.TGIEB = 0; TPU3.TIER.BIT.TGIEC = 0; TPU3.TIER.BIT.TGIED = 0;
3	Stop count operation.	MTU.TSTR.BIT.CST0 = 0;	TPU.TSTR.BIT.CST3 = 0;
4	Clear counter.	MTU0.TCNT = 0x0000;	TPU3.TCNT= 0x0000;
5	Make I/O port function settings.*2	PORT3.PMR.BIT.B4 = 0; PORT1.PMR.BIT.B5 = 0; PORTA.PDR.BIT.B3 = 0; MPC.PWPR.BIT.B0WI = 0; MPC.PWPR.BIT.PFSWE = 1; MPC.P34PFS.BYTE = 0x01; MPC.P15PFS.BYTE = 0x01; MPC.PA3PFS.BYTE = 0x01; MPC.PWPR.BIT.PFSWE = 0; MPC.PWPR.BIT.B0WI = 1; PORT3.PMR.BIT.B4 = 1; PORT1.PMR.BIT.B5 = 1; PORTA.PMR.BIT.B3 = 1;	— (No processing)
6	Make count clock setting.	MTU0.TCR.TPSC = 000b;	TPU3.TCR.BIT.TPSC = 000b;
7	Make counter clear setting.	MTU0.TCR.BIT.CCLR = 101b;	TPU3.TCR.BIT.CCLR = 001b;
8	Make operation mode setting.	MTU0.TMDR.BIT.MD = 0011b;	TPU3.TMDR.BIT.MD = 0011b;
9	Set counter to independent operation.	MTU.TSYR.BIT.SYNC0 = 0;	TPU.TSYR.BIT.SYNC3 = 0;
10	Make waveform output mode settings.	MTU0.TIORH.BIT.IOA = 0010b; MTU0.TIORH.BIT.IOB = 0010b; MTU0.TIORL.BIT.IOD = 0010b;	TPU3.TIOR.BIT.IOB = 0010b; TPU3.TIOR.BIT.IOC = 0010b; TPU3.TIOR.BIT.IOD = 0010b;
11	Make TGR register settings.	MTU0.TGRA = 0x1C1F; MTU0.TGRB = 0x2EDF; MTU0.TGRC = 0x5DBF; MTU0.TGRD = 0x419E;	TPU3.TGRA = 0x4E20; TPU3.TGRB = 0x1770; TPU3.TGRC = 0x2710; TPU3.TGRD = 0x36B0;
12	Make interrupt control mode setting.*3	— (No processing)	INTC.INTCR.BIT.INTM = 10b;

Procedure		RX (RX231)	H8S (H8S/2378)
13	Make interrupt priority level settings.*4	IPR(MTU0,TGIA0) = 0x01; IPR(MTU0,TGIB0) = 0x01; IPR(MTU0,TGIC0) = 0x01; IPR(MTU0,TGID0) = 0x01;	INTC.IPRG.BIT._TPU3 = 001b;
14	Clear peripheral function interrupt requests.	— (No processing)*5	TPU3.TSR.BIT.TGFA = 0; TPU3.TSR.BIT.TGFB = 0; TPU3.TSR.BIT.TGFC = 0; TPU3.TSR.BIT.TGFD = 0;
15	Clear interrupt requests.	IR(MTU0,TGIA0) = 0; IR(MTU0,TGIB0) = 0; IR(MTU0,TGIC0) = 0; IR(MTU0,TGID0) = 0;	— (No processing)
16	Enable peripheral function interrupt requests.	MTU0.TIER.BIT.TGIEA = 1; MTU0.TIER.BIT.TGIEB = 1; MTU0.TIER.BIT.TGIEC = 1; MTU0.TIER.BIT.TGIED = 1;	TPU3.TIER.BIT.TGIEA = 1; TPU3.TIER.BIT.TGIEB = 1; TPU3.TIER.BIT.TGIEC = 1; TPU3.TIER.BIT.TGIED = 1;
17	Enable interrupt requests.*6	IEN(MTU0,TGIA0) = 1; IEN(MTU0,TGIB0) = 1; IEN(MTU0,TGIC0) = 1; IEN(MTU0.TGID0) = 1;	— (No processing)
18	Make processor interrupt priority level setting.	— (No processing)	set_imask_exr(0);
19	Enable maskable interrupts.	setpsw_i();	— (No processing)
20	Start count operation.	MTU.TSTR.BIT.CST0 = 1;	TPU.TSTR.BIT.CST3 = 1;

Note 1. For information on the module stop function, refer to section 5, Module Stop Function.

Note 2. On the RX231 Group peripheral function pin settings are made in the MPC. For details, refer to 7.1, I/O Ports.

Note 3. The RX231 Group has no interrupt control mode. For details, refer to section 4, Points of Difference between Interrupts.

Note 4. For details of the interrupt priority level setting method, refer to section 4, Points of Difference between Interrupts.

Note 5. The MTU of the RX231 Group does not have interrupt request flags in peripheral functions. For details, refer to section 4, Points of Difference between Interrupts.

Note 6. The methods of enabling interrupt requests differ. For details, refer to section 4, Points of Difference between Interrupts.

4. Points of Difference between Interrupts

Table 4.1 lists points of difference between interrupt sources on the H8S/2378 Group and RX231 Group.

Table 4.1 Points of Difference between Interrupt Sources on H8S/2378 Group and RX231 Group

Channel	Name			Interrupt Source
	TPU of RX231 Group	MTU of RX231 Group	TPU of H8S/2378 Group	
0	TGI0A	TGIA0	TGI0A	TGRA input capture/compare match
	TGI0B	TGIB0	TGI0B	TGRB input capture/compare match
	TGI0C	TGIC0	TGI0C	TGRC input capture/compare match
	TGI0D	TGID0	TGI0D	TGRD input capture/compare match
	TCI0V	TCIV0	TCI0V	TCNT overflow
	Not available	TGIE0	Not available	TGRE compare match
	Not available	TGIF0	Not available	TGRF compare match
1	TGI1A	TGIA1	TGI1A	TGRA input capture/compare match
	TGI1B	TGIB1	TGI1B	TGRB input capture/compare match
	TCI1V	TCIV1	TCI1V	TCNT overflow
	TCI1U	TCIU1	TCI1U	TCNT underflow
2	TGI2A	TGIA2	TGI2A	TGRA input capture/compare match
	TGI2B	TGIB2	TGI2B	TGRB input capture/compare match
	TCI2V	TCIV2	TCI2V	TCNT overflow
	TCI2U	TCIU2	TCI2U	TCNT underflow
3	TGI3A	TGIA3	TGI3A	TGRA input capture/compare match
	TGI3B	TGIB3	TGI3B	TGRB input capture/compare match
	TGI3C	TGIC3	TGI3C	TGRC input capture/compare match
	TGI3D	TGID3	TGI3D	TGRD input capture/compare match
	TCI3V	TCIV3	TCI3V	TCNT overflow
4	TGI4A	TGIA4	TGI4A	TGRA input capture/compare match
	TGI4B	TGIB4	TGI4B	TGRB input capture/compare match
	Not available	TGIC4	Not available	TGRC input capture/compare match
	Not available	TGID4	Not available	TGRD input capture/compare matcha
	TCI4V	—	TCI4V	TCNT overflow
	—	TCIV4	—	TCNT overflow/underflow
	TCI4U	Not available	TCI4U	TCNT underflow
5	TGI5A	Not available	TGI5A	TGRA input capture/compare match
	TGI5B	Not available	TGI5B	TGRB input capture/compare match
	TCI5V	Not available	TCI5V	TCNT overflow
	TCI5U	Not available	TCI5U	TCNT underflow
	Not available	TGIU5	Not available	TGRU input capture/compare match
	Not available	TGIV5	Not available	TGRV input capture/compare match
	Not available	TGIW5	Not available	TGRW input capture/compare match

Table 4.2 lists the points of difference between the interrupt-related resources of TPU channel 1 on the H8S/2378 Group and TPU1 on the RX231 Group.

Table 4.3 lists the points of difference between the interrupt-related resources of TPU channel 1 on the H8S/2378 Group and MTU1 on the RX231 Group.

On the H8S/2378 Group the TPU has interrupt enable bits and interrupt request flags in peripheral functions only.

On the RX231 Group the TPU has interrupt enable bits and interrupt request flags in peripheral functions and in the interrupt controller.

On the RX231 Group the MTU has interrupt enable bits in peripheral functions and in the interrupt controller, as well as interrupt request flags in the interrupt controller.

Table 4.2 Points of Difference between Interrupt-Related Resources of TPU Channel 1 on H8S/2378 Group and TPU1 on RX231 Group

		TPU1 of RX (RX231)				Channel 1 of TPU of H8S (H8S/2378)			
Item		**TGI1A**	**TGI1B**	**TCI1V**	**TCI1U**	**TGI1A**	**TGI1B**	**TCI1V**	**TCI1U**
Interrupt enable bits	Peripheral function	TIER. TGIEA	TIER. TGIEB	TIER. TCIEV	TIER. TCIEU	TIER. TGIEA	TIER. TGIEB	TIER. TCIEV	TIER. TCIEU
	Interrupt controller	IER12. IEN3	IER12. IEN4	IER12. IEN5	IER12. IEN6	Not available			
Interrupt request flag	Peripheral function	TSR. TGFA	TSR. TGFB	TSR. TCFV	TSR. TCFU	TSR. TGFA	TSR. TGFB	TSR. TCFV	TSR. TCFU
	Interrupt controller	IR147. IR	IR148. IR	IR149. IR	IR150. IR	Not available			

Table 4.3 Points of Difference between Interrupt-Related Resources of TPU Channel 1 on H8S/2378 Group and MTU1 on RX231 Group

		MTU1 of RX (RX231)				Channel 1 of TPU of H8S (H8S/2378)			
Item		**TGIA1**	**TGIB1**	**TGIV1**	**TGIU1**	**TGI1A**	**TGI1B**	**TGI1V**	**TGI1U**
Interrupt enable bits	Peripheral function	TIER. TGIEA	TIER. TGIEB	TIER. TCIEV	TIER. TCIEU	TIER. TGIEA	TIER. TGIEB	TIER. TCIEV	TIER. TCIEU
	Interrupt controller	IER0F. IEN1	IER0F. IEN2	IER0F. IEN3	IER0F. IEN4	Not available			
Interrupt request flag	Peripheral function	Not available				TSR. TGFA	TSR. TGFB	TSR. TCFV	TSR. TCFU
	Interrupt controller	IR121. IR	IR122. IR	IR123. IR	IR124. IR	Not available			

The IERm registers (m = 02h to 1Fh) and IRn registers (n = interrupt vector number) listed in Table 4.2 and Table 4.3 are interrupt controller registers.

For the interrupt sources corresponding to the bits in the IERm registers and the interrupt vector numbers, refer to the section describing the interrupt controller in User's Manual: Hardware.

Interrupts can be accepted on the RX231 Group when the following conditions are met:

- The I flag (PSW.I bit) is set to 1.
- The interrupt is enabled in the IER and IPR registers of the ICU.
- Interrupt requests are enabled by the corresponding peripheral function interrupt request enable bit.

Table 4.4 is a comparative listing of the interrupt generation conditions on the RX231 Group and H8S/2378 Group.

Table 4.4 Comparative Listing of Interrupt Generation Conditions on RX231 Group and H8S/2378 Group

Item	RX (RX231)	H8S (H8S/2378)
Interrupt enable bit (I bit)	Setting the I bit in the PSW register to 1 (enabled) enables acceptance of maskable interrupts.	In interrupt control mode 0, setting the I bit to 0 (enabled) in the CCR register enables acceptance of maskable interrupts. In interrupt control mode 2 the I bit in the CCR register is not used.
Processor interrupt priority level	Only interrupt requests with a higher priority level than that indicated by the IPL[3:0] bits in the PSW register are accepted.	In interrupt control mode 2 only interrupt requests with a higher priority level than that indicated by bits I2 to I0 in the EXR register are accepted. In interrupt control mode 0 the bits I2 to I0 in the EXR register is not used.
Interrupt priority level	Set in the IPR register.	In interrupt control mode 0 the default settings are used. In interrupt control mode 2 the IPR register settings are used.
Interrupt request flag	The interrupt controller manages all interrupt status flags for peripheral functions, external pins, NMI interrupts, etc.	The interrupt controller manages interrupt status flags for external interrupts, and interrupt status flags for internal interrupt sources are managed within each on-chip peripheral function.
Interrupt request enable	Set in the IER register for maskable interrupts and in the NMIER register for non-maskable interrupts.	IRQ interrupts are enabled by settings in the IER register.
Peripheral function interrupt enable	Interrupts can be enabled or disabled by each peripheral function.	

Table 4.5 lists points of difference in the enabling and priority levels of processor interrupts.

On the RX231 Group the processor interrupt priority level is 0 (lowest level) by default when the PSW.I bit is set to 1 (interrupt enabled), so maskable interrupts are enabled.

On H8S/2378 Group, in interrupt control mode 0, processor interrupt priority levels are not used when the CCR.I bit is cleared to 0 (interrupt enabled), so maskable interrupts are enabled.

On H8S/2378 Group, in interrupt control mode 2, the processor interrupt priority level is 7 (highest level) by default, so maskable interrupts are enabled by setting bits I2 to I0 in EXR.

Table 4.5 Points of Difference in Enabling and Priority Levels of Processor Interrupts

		H8S (H8S/2378)	
Item	**RX (RX231)**	**Interrupt Control Mode 0**	**Interrupt Control Mode 2**
Interrupt enable default value	PSW.I bit: 0 (interrupt mask)	CCR.I bit: 1 (interrupt mask)	Not used*[1]
Processor interrupt priority level default value	PSW.IPL[3:0] bits: 0000b (lowest level)	Not used*[1]	EXR bits I2 to I0: 111b (highest level)
Operation after a reset	Maskable interrupts are not accepted.		

Note 1. Don't care.

Table 4.6 lists some of the embedded functions used for enabling interrupts.

Table 4.6 Embedded Functions Used for Enabling Interrupts (Partial Listing)

	Description		
		H8S (H8S/2378)	
Item	**RX (RX231)**	**Interrupt Control Mode 0**	**Interrupt Control Mode 2**
Processor interrupt enable setting	setpsw_i(); *[1]	set_imask_ccr(0); *[1]	Not used
Processor interrupt priority level setting (setting = 0)	set_ipl(0); *[1]	Not used	set_imask_exr(0); *[1]

Note 1. The file machine.h must be included.

For details, refer to the sections describing the interrupt controller (ICU), CPU, and peripheral functions used in User's Manual: Hardware.

5. Module Stop Function

On the H8S/2378 Group and RX231 Group it is possible to halt the functioning of individual peripheral modules.

Power consumption can be reduced by transitioning unused peripheral modules to the module stop state. Modules not listed in Table 5.1 are in the module stop state after a reset.

Table 5.1 Modules that Operate under Initial Settings on RX231 Group and H8S/2378 Group

RX (RX231)	H8S (H8S/2378)
DMAC, DTC, RAM	EXDMAC, DMAC, DTC

When a module is in the module stop state, its registers cannot be read or written to.

Before using any module not listed in Table 5.1, it is necessary to cancel the module stop state and then make initial settings.

For details, refer to the section describing the low power consumption functions in User's Manual: Hardware.

6. Register Write Protection Function

On the RX231 Group it is possible to protect important registers from being overwritten if program runaway occurs. The protect register (PRCR) is used to specify the registers that are protected by this function.

Register protection can be enabled for the clock generation circuit–related registers, flash memory–related registers, operating mode–related registers, low power consumption function–related registers, low-power timer–related registers, LVD–related registers, and software reset register.

For details, refer to the section on the register write protection function in User's Manual: Hardware.

7. Key Points when Migrating from H8S to RX

Some points to keep in mind when migrating from the H8S/2378 Group to the RX231 Group are described below.

7.1 I/O Ports

On the RX231 Group it is necessary to make settings to the MPC to assign pins to peripheral function I/O signals.

To apply I/O control to a pin on the RX231 Group, make the following two settings:

- PFS register of MPC: Select the peripheral function to be assigned to the pin.
- PMR register of I/O port: Select whether to assign the pin to a general I/O port or a peripheral function.

Table 7.1 provides a comparative listing of I/O settings for peripheral function pins on the RX231 Group and H8S/2378 Group.

Table 7.1 Comparison of I/O settings for Peripheral Function Pins on RX231 Group and H8S/2378 Group

Function	RX (RX231)	H8S (H8S/2378)
Pin function selection	I/O pins for peripheral functions can be assigned from a selection of multiple pins by making settings in the PFS register.	Pins can be switched between general I/O port and peripheral function settings and pin functions selected through combinations of the MCU operating mode, the setting of the SYSCR.EXPE bit, the PFCR registers, the DDR registers, and the settings of the various peripheral functions.
General I/O port/peripheral function switching	Settings in the PMR register can be used to select whether specific pins are used as I/O ports or as peripheral functions.	

For details, refer to the sections describing the multi-function pin controller (MPC) and I/O ports in User's Manual: Hardware.

7.2 I/O Register Macros

The macro definitions listed below are contained in the I/O register definition file (iodefine.h) of the RX231 Group.

Using macro definitions can make program code easier to read.

Table 7.2 lists macro usage examples.

Table 7.2 Macro Usage Examples

Macro	Usage Example
IR(“module name”,”bit name”)	IR(MTU0,TGIA0) = 0; Clears the IR bit corresponding to TGIA0 of MTU0 to 0 (clear interrupt request).
DTCE(“module name”,”bit name”)	DTCE(MTU0,TGIA0) = 1; Sets the DTCE bit corresponding to TGIA0 of MTU0 to 1 (enable DTC start).
IEN(“module name”,”bit name”)	IEN(MTU0,TGIA0) = 1; Sets the IEN bit corresponding to TGIA0 of MTU0 to 1 (enable interrupt).
IPR(“module name”,”bit name”)	IPR(MTU0,TGIA0) = 0x02; Sets the IPR bits corresponding to TGIA0 of MTU0 to 2 (interrupt priority level 2).
MSTP(“module name”)	MSTP(MTU) = 0; Clears the module stop setting bit of MTU0 to 0 (cancel module stop state).
VECT(“module name”,”bit name”)	#pragma interrupt(Excep_MTU0_TGIA0(vect=VECT(MTU0,TGIA0))) Declares the interrupt function corresponding to TGIA0 of MTU0.

7.3 Embedded Functions

On the RX231 Group interrupt functions are provided to implement control register settings or special instructions. To use these embedded functions, include the file machine.h.

Table 7.3 lists (examples of) points of difference between control register settings and special instructions on the RX231 Group and H8S/2378 Group.

Table 7.3 Points of Difference between Control Register Settings and Special Instructions on RX231 Group and H8S/2378 Group (Example)

	Format	
Item	**RX (RX231)**	**H8S (H8S/2378)**
Set I flag to 1.	setpsw_i(); *1	set_imask_ccr(1); *1*2
Clear I flag to 0.	clrpsw_i(); *1	set_imask_ccr(0); *1*2
Expand to WAIT instruction.	wait(); *1	None
Expand to NOP instruction.	nop(); *1	nop(); *1

Note 1. It is necessary to include the file machine.h.

Note 2. I = 1 means enable interrupts on the RX231 Group, and I = 1 means mask interrupts on the H8S/2378 Group.

8. Reference Documents

User's Manual: Hardware

H8S/2378 Group, H8S/2378R Group Hardware Manual Rev.7.00 (REJ09B0109-0700)
RX230 Group and RX231 Group User's Manual: Hardware Rev.1.10 (R01UH0496EJ0110)
(The latest versions can be downloaded from the Renesas Electronics website.)

Application Note

M16C Family, RX Family Migrating From the M16C Family to the RX Family: Timers Rev.1.10 (R01AN1729EJ0110)
(The latest versions can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest versions can be downloaded from the Renesas Electronics website.)

User's Manual: Development Environment

CC-RX Compiler User's Manual Rev.1.04 (R20UT3248EJ0104)
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package Ver.6.01 User's Manual (REJ10B0161-0100)
(The latest versions can be downloaded from the Renesas Electronics website.)

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Nov. 17, 2017	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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