RX Family, H8S Family

H8S to RX Migration Guide: ADC

R01AN4391EJ0100
Rev.1.00
Jul 13, 2018

Summary

This application note explains how to migrate from the A/D converter of the H8S Family to the 12-bit A/D converter (S12ADE) of the RX Family.

Target Devices

- RX Family
- H8S Family

An example of migrating from the H8S Family to the RX Family is presented, with the RX Family represented by the RX231 Group and the H8S Family represented by the H8S/2378 Group. When using this application note with other microcontrollers, appropriate changes should be made to match the specifications of the microcontroller used and thorough evaluation should be performed.

Devices on Which Operation Has Been Confirmed

- RX Family: RX231
- H8S Family: H8S/2378

There are some differences in terminology between the RX Family and H8S Family.

Differences in terminology related to the A/D converter are listed in the table below.

Table Differences in Terminology between RX Family and H8S Family

Item	RX Family	H8S Family
Name of A/D converter module	12-bit A/D converter (S12ADE)	A/D converter
Name of interrupt	Scan end interrupt (S12ADI0)	A/D conversion end interrupt (ADI)
Name of trigger by external pin input	Asynchronous trigger	External trigger

In the discussion below, the term A/D converter is used to refer to the A/D converter, 12-bit A/D converter (S12ADE), etc.

Contents

1. Points of Difference between A/D Converters

1.1 Points of Difference between Functions

Table 1.1 lists points of difference between the A/D converter functions.

Table 1.1 Points of Difference between A/D Converter Functions

Item	RX (RX231)	H8S (H8S/2378)
Number of units	1 unit	
Number of channel sets	None	2 channel sets
Input channels	24 channels	16 channels
Extended analog functions	Temperature sensor output Internal reference voltage	None
A/D conversion method	Successive approximation method	
Resolution	12 bits	10 bits
Conversion time	0.83 μs per channel (when A/D conversion clock (ADCLK) = 54 MHz)	7.4 μs per channel (when operating at 35 MHz)
A/D conversion clock setting	The peripheral module clock (PCLK) and A/D conversion clock (ADCLK) can be set to the following frequency ratios:*1 PCLK:ADCLK frequency ratio = 1:1, 1:2, 1:4, 2:1, 4:1, or 8:1 (ADCLK is set using the clock generation circuit.)	None
Data registers	24 registers for analog input, 1 for A/D-converted data duplication in double trigger mode 1 register for temperature sensor output 1 register for internal reference voltage 1 register for self-diagnostics	8 registers for analog input
Operating modes	Single scan mode Continuous scan mode Group scan mode (with ability to give priority to group A)	Single mode Scan mode
Conditions for A/D conversion start*2	Software trigger Synchronous trigger (trigger from MTU, ELC, or TPU) Asynchronous trigger	Software trigger Conversion start trigger from TPU or TMR External trigger signal

Item	RX (RX231)	H8S (H8S/2378)
Functions	Variable sampling state count function 12-bit A/D converter self-diagnostic function Selectable between A/D-converted value addition mode or average mode Analog input disconnection detection function (discharge function/precharge function) Double trigger mode (A/D-converted data duplication function) A/D data register auto-clear function Compare function (window A and window B) 16 ring buffers when the compare function is used	None
Interrupt sources	Scan end interrupt request (S12ADI) Group B dedicated scan end interrupt request (GBADI)	A/D conversion end interrupt request (ADI)
Event link function	Group scan mode • Generation of ELC event at group A scan end • Generation of ELC event at group B scan end Generation of ELC event at completion of all scans Ability to start scan by ELC trigger output Single scan mode • Generation of ELC event when window compare event conditions are met	None
Conversion modes	High-speed conversion mode Normal conversion mode	None
DMAC and DTC activation	Supported	
Low power consumption function	Ability to specify transition to module stop state*3	Ability to specify transition to module stop state

Note 1. Peripheral module clock (PCLK) refers to PCLKB and A/D conversion clock (ADCLK) to PCLKD. PCLKB and PCLKD can each be specified by setting a division ratio in the clock generation circuit. For details, refer to RX230 Group, RX231 Group User's Manual: Hardware.

Note 2. For details of A/D conversion start conditions, refer to Table 1.2, Comparison of A/D Conversion Start Triggers on RX231 Group and H8S/2378 Group.

Note 3. Allow at least 1 μs to elapse after canceling the module stop state before starting A/D conversion.

Table 1.2 shows a comparison of A/D conversion start triggers on the RX231 Group and H8S/2378 Group.

Table 1.2 Comparison of A/D Conversion Start Triggers on RX231 Group and H8S/2378 Group

Item		**Name**[*1]
RX (RX231)	**H8S (H8S/2378)**	**RX (RX231)**
Software trigger		None
Trigger input on ADTRG0# pin	Trigger input on $\overline{\text{ADTRG}}$ pin	None
TPU0 to TPU4 TGRA compare match or input capture, or TPU0.TGRA compare match or input capture	Conversion start trigger from TPU (16-bit timer pulse unit)	TRGAN1 TRG4ABN1
None	Conversion start trigger from TMR (8-bit timer)	
MTU0.TGRA compare match or input capture	None	TRG0AN
MTU0.TGRB compare match or input capture		TRG0BN
MTU0 to MTU4 TGRA compare match or input capture, or MTU4.TCNT underflow (trough) in complementary PWM mode		TRGAN
MTU0.TGRE compare match		TRG0EN
MTU0.TGRF compare match		TRG0FN
MTU4.TADCORA and MTU4.TCNT compare match (interrupt skipping function)		TRG4AN
MTU4.TADCORB and MTU4.TCNT compare match (interrupt skipping function)		TRG4BN
MTU4.TADCORA and MTU4.TCNT or MTU4.TADCORB and MTU4.TCNT compare match (interrupt skipping function)		TRG4ABN
Trigger from ELC		None

Note 1. A/D conversion start triggers are not named on the H8S/2378 Group.

Note: For information on the multi-function timer pulse unit (MTU), 16-bit timer pulse unit (TPU), and event link controller (ELC) of the RX231 Group, refer to RX230 Group, RX231 Group User's Manual: Hardware.

1.2 Points of Difference between A/D Converters

Figure 1.1 is a block diagram of the 12-bit A/D converter of the RX231 Group.

Figure 1.2 is a block diagram of the A/D converter of the H8S/2378 Group.

The main points of difference between the H8S/2378 Group and RX231 Group are indicated by the red circles in Figure 1.1 and Figure 1.2.

The H8S/2378 Group and RX231 Group have different pin configurations. Refer to Table 1.3 for a listing of the points of difference for the input and output pins.

The 12-bit A/D converter of the RX231 Group is provided with a power generator for self-diagnostics and a function for outputting event signals to the event link controller (ELC). The A/D converter of the H8S/2378 Group is not provided with such a power generator or event signal output function.

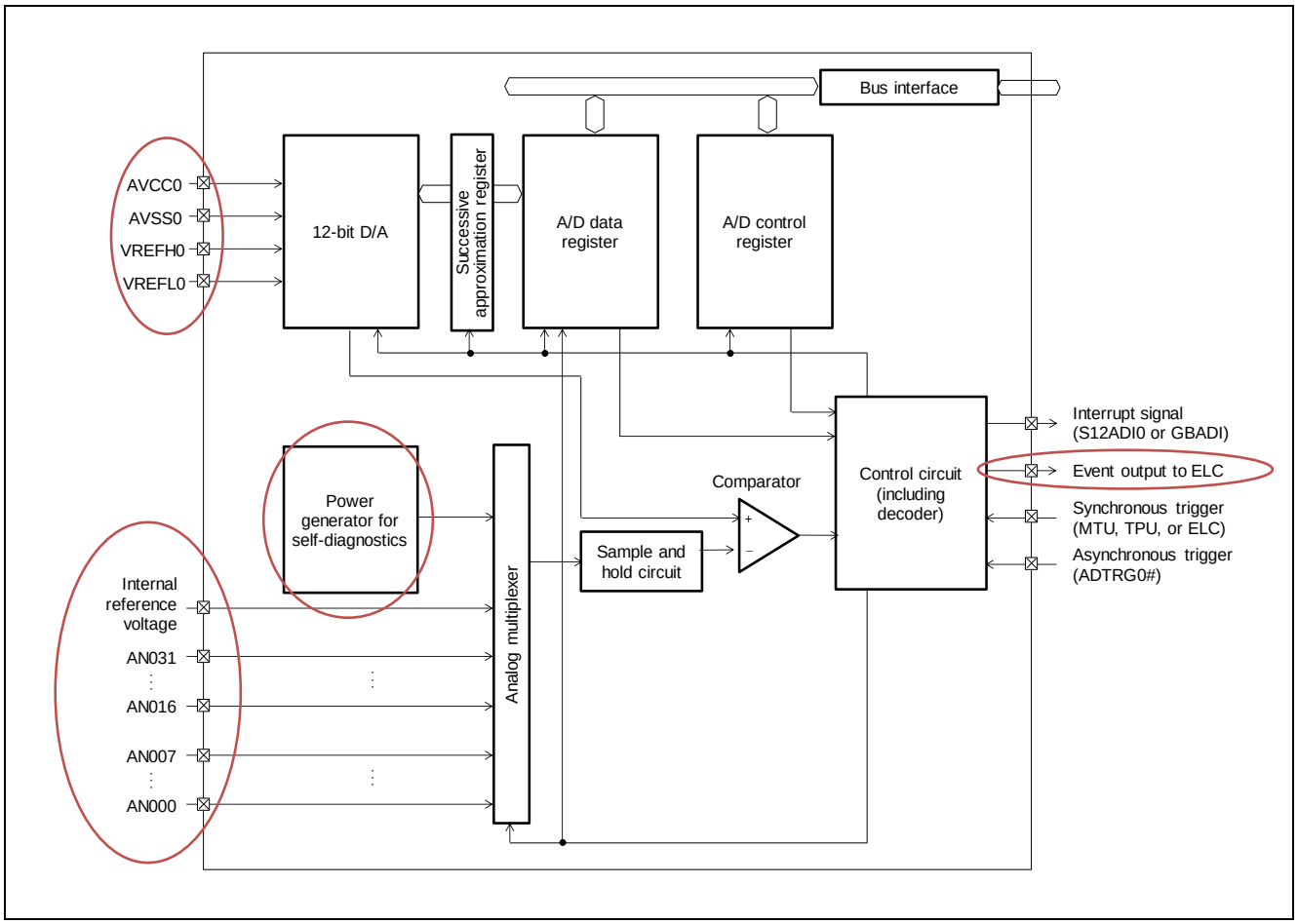


Figure 1.1 Block Diagram of 12-Bit A/D Converter of RX231 Group

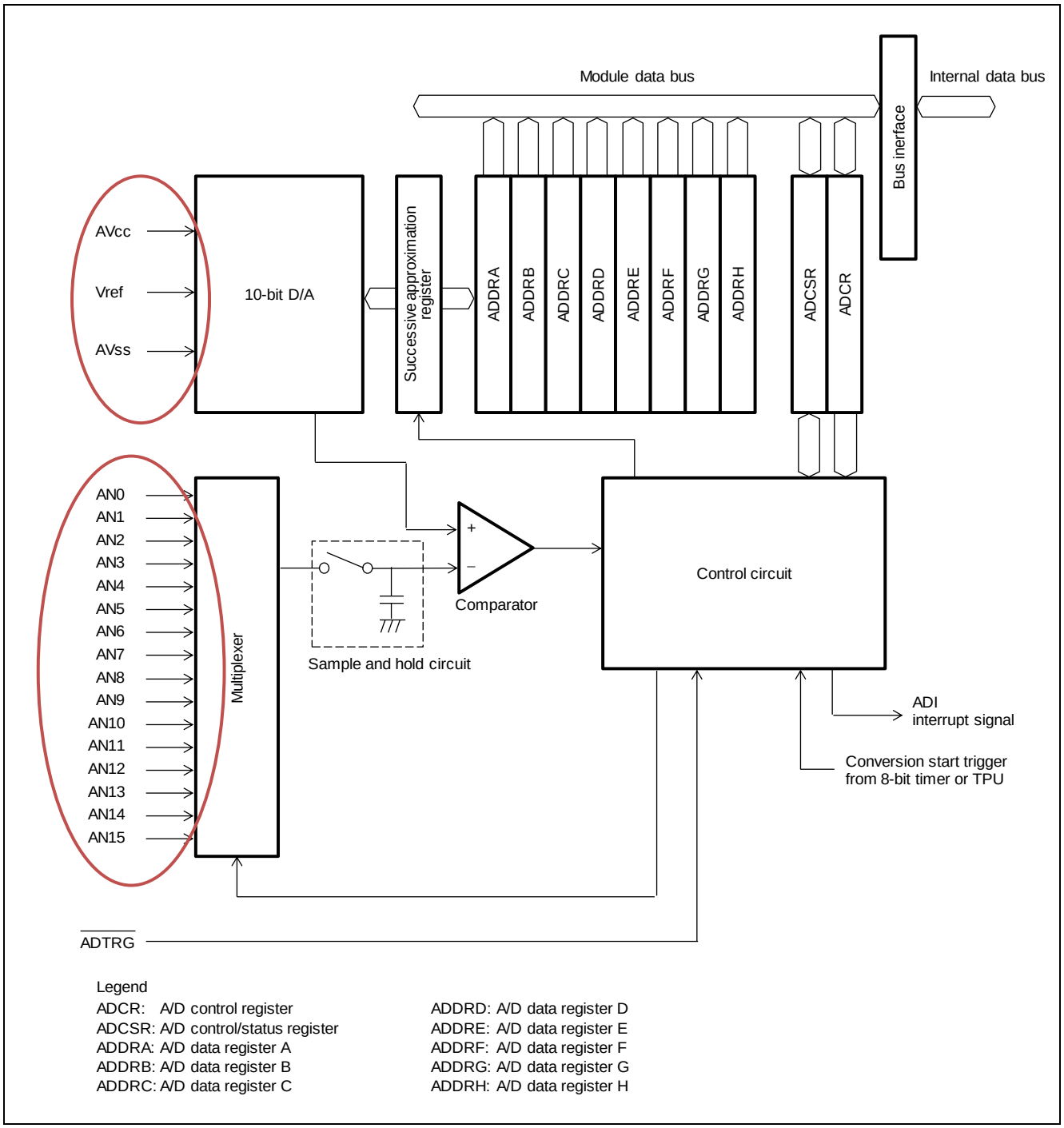


Figure 1.2 Block Diagram of A/D Converter of H8S/2378 Group

Table 1.3 Points of Difference for Input/Output Pins

RX (RX231)	H8S (H8S/2378)	Function	I/O
AVCC0	AVcc	Analog block power supply pin	Input
AVSS0	AVss	Analog block ground pin	Input
VREFH0	Vref	Reference power supply pin	Input
VREFL0	None	Reference power supply ground pin	Input
AN000 to AN007, AN016 to AN031	AN0 to AN15*1	Analog input pins	Input
ADTRG0#	$\overline{\text{ADTRG}}$	A/D external trigger input pin	Input

Note 1. On the H8S/2378 Group, channels are grouped together as “channel sets.”
AN0 to AN7 are the analog input channels of channel set 0 and AN8 to AN15 the analog input channels of channel set 1.

1.3 Points of Difference between Registers

Table 1.4 lists the A/D converter registers of the RX231 Group and H8S/2378 Group.

Table 1.4 A/D Converter Registers of RX231 Group and H8S/2378 Group

RX (RX231)	H8S (H8S/2378)
A/D data register y (ADDRy) (y = 0 to 7, 16 to 31)	A/D data registers A to H (ADDRA to ADDRH)
A/D data duplication register (ADDBLDR)	None
A/D temperature sensor data register (ADTSDR)	
A/D internal reference voltage data register (ADOCDR)	
A/D self-diagnosis data register (ADRD)	
A/D control register (ADCSR)	A/D control register (ADCR)
None	A/D control/status register (ADCSR)
A/D control extended register (ADCER)	None
A/D channel select register A0 (ADANSA0)	
A/D channel select register A1 (ADANSA1)	
A/D channel select register B0 (ADANSB0)	
A/D channel select register B1 (ADANSB1)	
A/D conversion start trigger select register (ADSTRGR)	
A/D sampling state register n (ADSSTRn) (n = 0 to 7, L, T, O)	
A/D-converted value addition/average function select register 0 (ADADS0)	
A/D-converted value addition/average function select register 1 (ADADS1)	
A/D-converted value addition/average count select register (ADADC)	
A/D group scan priority control register (ADGSPCR)	
A/D conversion extended input control register (ADEXICR)	
A/D disconnection detection control register (ADDISCR)	
A/D high-potential/low-potential reference voltage control register (ADHVREFCNT)	
A/D event link control register (ADELCCR)	
A/D compare function control register (ADCMPCR)	
A/D compare function window A channel select register 0 (ADCMPANSR0)	
A/D compare function window A channel select register 1 (ADCMPANSR1)	
A/D compare function window A extended input select register (ADCMPANSER)	
A/D compare function window A comparison condition setting register 0 (ADCMPLR0)	
A/D compare function window A comparison condition setting register 1 (ADCMPLR1)	
A/D compare function window A extended input comparison condition setting register (ADCMPLER)	
A/D compare function window A lower-side level setting register (ADCMPDR0)	
A/D compare function window A upper-side level setting register (ADCMPDR1)	

RX (RX231)	H8S (H8S/2378)
A/D compare function window A channel status register 0 (ADCMPSR0)	None
A/D compare function window A channel status register 1 (ADCMPSR1)	
A/D compare function window A extended input channel status register (ADCMPSER)	
A/D compare function window A/B status monitor register (ADWINMON)	
A/D compare function window B channel select register (ADCMPBNSR)	
A/D compare function window B lower-side level setting register (ADWINLLB)	
A/D compare function window B upper-side level setting register (ADWINULB)	
A/D compare function window B channel status register (ADCMPBSR)	
A/D data storage buffer register n (ADBUFn) (n = 0 to 15)	
A/D data storage buffer enable register (ADBUFEN)	
A/D data storage buffer pointer register (ADBUFPTR)	

Table 1.5 lists correspondences between the register bit functions of the RX231 Group and H8S/2378 Group. It shows which register bits on the RX231 Group correspond to the register bit functions of the H8S/2378 Group.

Table 1.5 Correspondences between Register Bit Functions of RX231 Group and H8S/2378 Group

RX (RX231)		H8S (H8S/2378)		
Register	**Bit**	**Register**	**Bit**	**Function**
ADDRy (y = 0 to 7, 16 to 31)		ADDRA to ADDRH		16-bit read-only registers that store the A/D conversion results.
IR102*1	IR	ADCSR	ADF	A/D conversion end flag
ADCSR	ADIE		ADIE	A/D conversion end interrupt enable/disable
	ADST		ADST	A/D conversion start/stop
ADANSA0	ANSA0[7:0]		CH3 to CH0	Selection of analog input channels on which A/D conversion is performed
ADANSA1	ANSA1[15:0]			
ADSTRGR	TRSA[5:0]	ADCR	TRGS1, TRGS0	A/D conversion start trigger selection, enable/disable A/D conversion start by trigger
ADCSR	EXTRG			
	TRGE			
	ADCS[1:0]		SCANE, SCANS	Scan mode selection
ADSSTRn (n = 0 to 7, L, T, O)			CKS1, CKS0	Setting of A/D conversion time

Note 1. IR registers are interrupt controller registers. The A/D converter of the RX231 Group does not use interrupt request flags for peripheral function. For details, refer to section 5, Points of Difference between Interrupts.

The methods for selecting analog input channels for A/D conversion are different on the RX231 Group and H8S/2378 Group.

On the RX231 Group the bits in the A/D channel select registers correspond to analog input channels. This means that up to 24 analog input channels can be selected in any combination on the RX231 Group. For details, refer to RX230 Group, RX231 Group User's Manual: Hardware.

In addition, the A/D data register formats are different on the RX231 Group and H8S/2378 Group.

On the H8S/2378 Group, the top 10 bits of each A/D data register are used to store A/D conversion results.

On the RX231 Group, in contrast, the ADRFMT bit in the ADCER register is used to select the register format between flush-right (LSB side) and flush-left (MSB side). When flush-right (LSB side) is selected, the bottom 12 bits each A/D data register are used to store A/D conversion results, and when flush-left (MSB side) is selected, the top 12 bits are used. The default A/D data register format is flush-right (LSB side).

2. Peripheral Functions Used

Table 2.1 lists the peripheral functions and modes used in the A/D converter operation examples.

Table 2.1 Peripheral Functions and Modes Used in A/D Converter Operation Examples

	RX (RX231)		H8S (H8S/2378)		Operation Example	
No.	Peripheral Function	Mode	Peripheral Function	Mode	Mode	Reference
1	12-bit A/D converter (S12ADE)	Single scan mode	A/D converter	Single mode	Single mode	3.1
2		Continuous scan mode		Scan mode	Scan mode	3.2
3		Group scan mode		None	Group scan mode	3.3

3. Points of Difference in Operation

3.1 Single Mode Operation

The setting procedure for reproducing on the RX231 Group the single mode operation of the H8S/2378 Group is presented below. The operations and setting procedures listed in Table 3.1, Single Mode Operation Conditions, are described.

Table 3.1 Single Mode Operation Conditions

	Operation Conditions	
Item	**RX (RX231)**	**H8S (H8S/2378)**
Operating mode	Single scan mode	Single mode
Analog input channel	AN000	AN0
A/D conversion start trigger	TPU0.TGRA0 compare match or input capture	
Interrupt	Scan end interrupt (S12ADI0)	A/D conversion end interrupt (ADI)

In single mode on the H8S/2378 Group, A/D conversion is performed once on the analog input of a single specified channel. In single scan mode on the RX231 Group, A/D conversion is performed once on the analog input of up to 24 selected channels, starting from the lowest channel number and proceeding in order.

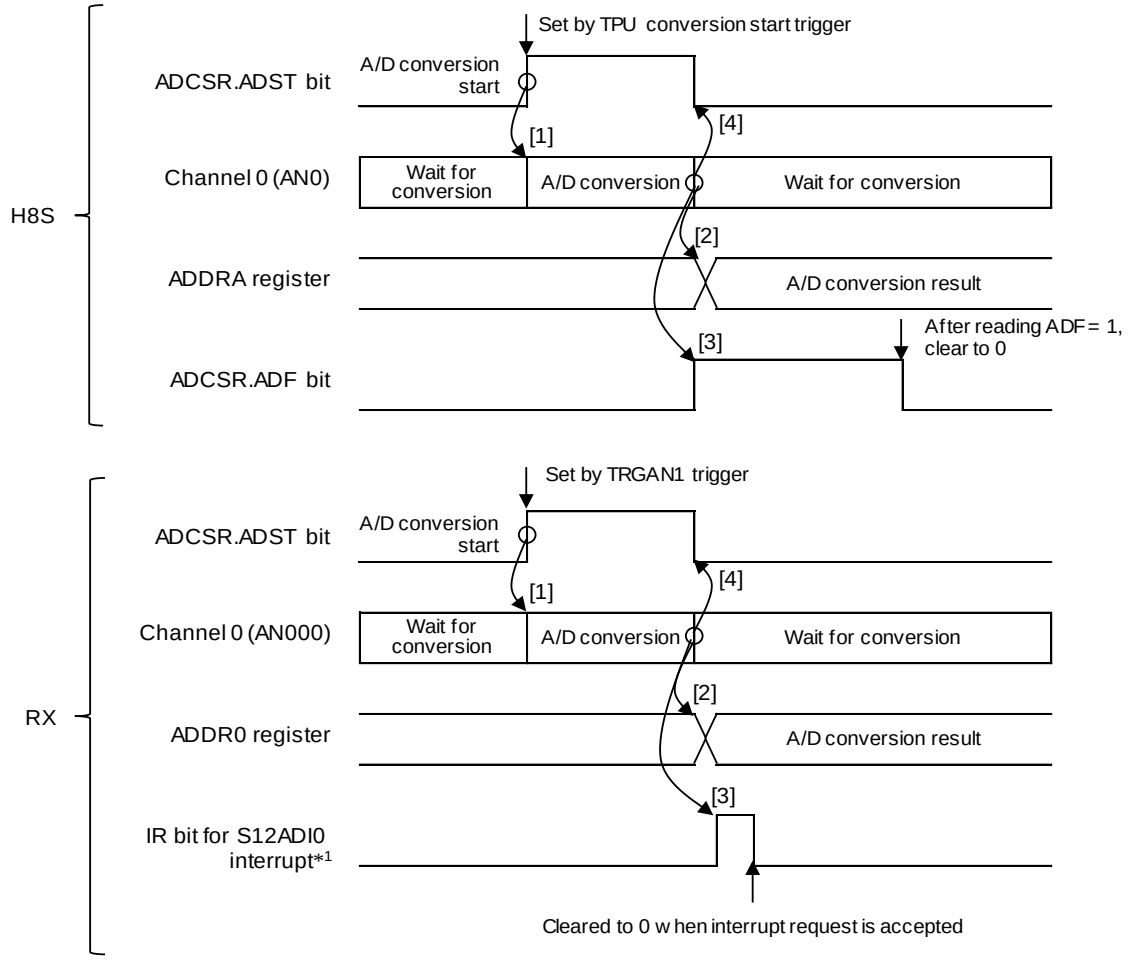
To reproduce the single mode operation of the H8S/2378 Group on the RX231 Group, select a single channel as the analog input channel in single scan mode.

3.1.1 Operation

Figure 3.1 is a timing chart of single mode operation.

Table 3.2 presents a description of single mode operation.

The numbers in Figure 3.1 correspond to the numbers in Table 3.2.



Note 1. The H8S/2378 Group and RX231 Group have different interrupt architectures. For details, see section 5, Points of Difference between Interrupts.

Figure 3.1 Single Mode Operation Timing Chart

Table 3.2 Description of Single Mode Operation

Item	RX (RX231) (Single Scan Mode)	H8S (H8S/2378) (Single Mode)
[1] A/D conversion start	When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the TRGAN1 trigger from the TPU, A/D conversion of the channels selected in the ADANSA0 and ADANSA1 registers starts, beginning with the ANn with the lowest n number and proceeding in order.	When the ADST bit in ADCSR is set to 1 (A/D conversion start) by the conversion start trigger from the TPU, A/D conversion of the single channel selected by bits CH3 to CH0 in ADCSR starts.
[2] Storage of A/D conversion results	When A/D conversion of one channel finishes, the A/D conversion result is stored in the A/D data register (ADDRy) corresponding to that channel.	When A/D conversion finishes, the A/D conversion result is stored in the A/D data register (ADDRA to ADDRH) corresponding to that channel.
[3] Generation of A/D conversion end interrupt	After A/D conversion of all the selected channels finishes, the IR bit for the S12ADI0 interrupt is set to 1 (generate interrupt request) and a S12ADI0 interrupt request is generated when the ADCSR.ADIE bit is set to 1 (generation of S12ADI0 interrupt after scan end enabled).	After A/D conversion finishes, the ADF bit in ADCSR is set to 1 (A/D conversion end). At this point, if the ADIE bit in ADCSR is set to 1 (generation of ADI interrupt by ADF enabled), an ADI interrupt request is generated.
[4] A/D conversion end	The value of the ADCSR.ADST bit remains 1 (A/D conversion start) while A/D conversion is in progress, and when A/D conversion of all the selected channels finishes it is cleared to 0 automatically, and the 12-bit A/D converter enters the standby state.	The value of the ADST bit in ADCSR remains 1 (A/D conversion start) while A/D conversion is in progress, and when conversion finishes it is cleared to 0 automatically, and the A/D converter enters the standby state.

3.1.2 Points of Difference between Setting Procedures

Table 3.3 lists the points of difference between the initial setting procedures for single mode operation.

The H8S/2378 Group and RX231 Group have different interrupt architectures and setting procedures for I/O port functions. For details, refer to section 5, Points of Difference between Interrupts, and 8.1, I/O Ports.

Table 3.3 Points of Difference between Initial Setting Procedures for Single Mode Operation

Procedure		RX (RX231)	H8S (H8S/2378)
1	Cancel module stop state*1	MSTP(S12AD) = 0;	MSTPCR.BIT._AD = 0;
2	Disable interrupt requests	S12AD.ADCSR.BIT.ADIE = 0; IEN(S12AD, S12ADI0) = 0;	AD.ADCSR.BIT.ADIE = 0;
3	Disable A/D conversion	S12AD.ADCSR.BIT.ADST = 0;	AD.ADCSR.BIT.ADST = 0;
4	Select scan mode	S12AD.ADCSR.BIT.ADCS = 0;	AD.ADCR.BIT.SCAN = 0;
5	Select channel	S12AD.ADANSA0.WORD = 0x0001;	AD.ADCSR.BIT.CH = 0;
6	Select A/D conversion start trigger	S12AD.ADCSR.BIT.EXTRG = 0; S12AD.ADSTRGR.BIT.TRSA = 13;	— (No processing)*2
7	Set A/D conversion time	S12AD.ADSSTR0 = 0x58;	AD.ADCR.BIT.CKS = 3;
8	Set I/O port functions*3	PORT4.PMR.BIT.B0 = 0; PORT4.PDR.BIT.B0 = 0; MPC.P40PFS.BYTE = 0x80;	— (No processing)
9	Set interrupt control mode	— (No processing)	INTC.INTCR.BIT.INTM = 2;
10	Set interrupt priority level	IPR(S12AD, S12ADI0) = 0x01;	INTC.IPRF.BIT._AD = 1;
11	Clear peripheral function interrupt request	— (No processing)	AD.ADCSR.BIT.ADF = 0;
12	Clear interrupt request	IR(S12AD, S12ADI0) = 0;	— (No processing)
13	Enable interrupt requests	S12AD.ADCSR.BIT.ADIE = 1; IEN(S12AD, S12ADI0) = 1;	AD.ADCSR.BIT.ADIE = 1;
14	Set processor interrupt priority level	— (No processing)	set_imask_exr(0);
15	Enable maskable interrupts	setpsw_i();	— (No processing)
16	Enable A/D conversion start by trigger signal	S12AD.ADCSR.BIT.TRGE = 1;	AD.ADCR.BIT.TRGS = 1;

Note 1. For information on the module stop function, refer to section 6, Module Stop Function.

Note 2. On the H8S/2378 Group, selection of the A/D conversion start trigger occurs simultaneously with step 16 “Enable A/D conversion start by trigger signal.”

Note 3. When using the AN000 pin, set the relevant pin as general input.
(Clear bits PORT.PDR.Bm and PORT.PMR.Bm to 0 (m: 0 to 7).)

3.2 Scan Mode Operation

The setting procedure for reproducing on the RX231 Group the scan mode operation of the H8S/2378 Group is presented below. The operations and setting procedures listed in Table 3.4, Scan Mode Operation Conditions, are described.

Table 3.4 Scan Mode Operation Conditions

	Operation Conditions	
Item	**RX (RX231)**	**H8S (H8S/2378)**
Operating mode	Continuous scan mode	Scan mode
Analog input channel	AN000 to AN002	AN0 to AN2
A/D conversion start trigger	Software	
Interrupt	Scan end interrupt (S12ADI0)	A/D conversion end interrupt (ADI)

In scan mode on the H8S/2378 Group, A/D conversion is performed consecutively on the analog inputs of a maximum of four or eight specified channels.

In continuous scan mode on the RX231 Group, A/D conversion is performed on the analog input of up to 24 selected channels, starting from the lowest channel number and proceeding in order.

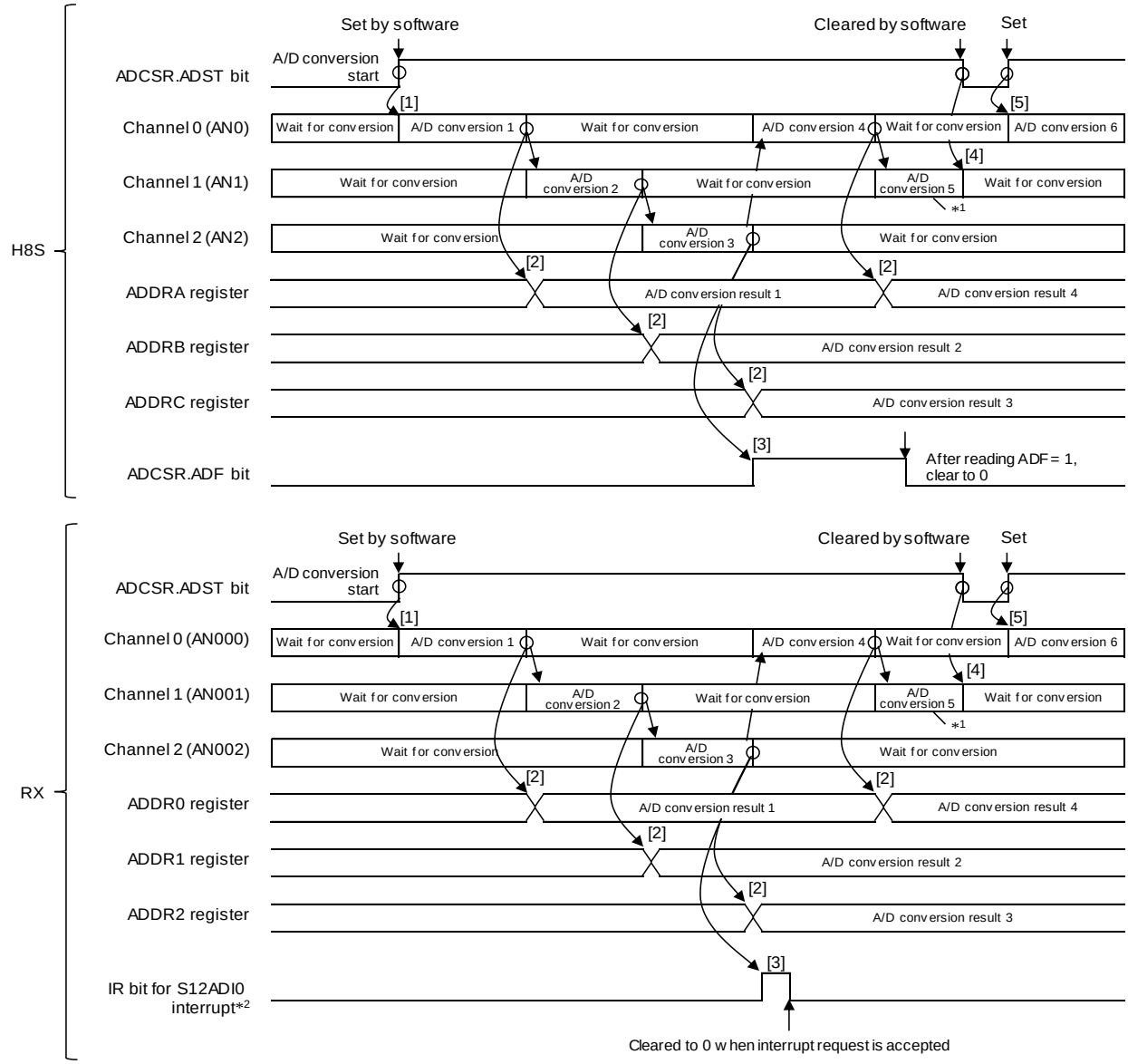
Operation is identical in scan mode on the H8S/2378 Group and in continuous scan mode on the RX231 Group.

3.2.1 Operation

Figure 3.2 is a timing chart of scan mode operation.

Table 3.5 presents a description of scan mode operation.

The numbers in Figure 3.2 correspond to the numbers in Table 3.5.



Note 1. The converted data from A/D conversion 5 is ignored.

Note 2. The H8S/2378 Group and RX231 Group have different interrupt architectures. For details, see section 5, Points of Difference between Interrupts.

Figure 3.2 Scan Mode Operation Timing Chart

Table 3.5 Description of Scan Mode Operation

Item	RX (RX231) (Continuous Scan Mode)	H8S (H8S/2378) (Scan Mode)
[1] A/D conversion start	When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger input, A/D conversion of the channels selected in the ADANSA0 and ADANSA1 registers starts, beginning with the ANn with the lowest n number and proceeding in order.	When the ADST bit in ADCSR is set to 1 (A/D conversion start) by a software trigger input, A/D conversion starts from the first channel selected by bits CH3 to CH0 in ADCSR.
[2] Storage of A/D conversion results	When A/D conversion of one channel finishes, the A/D conversion result is stored consecutively in the A/D data register (ADDRy) corresponding to that channel.	When A/D conversion of one channel finishes, the A/D conversion result is stored consecutively in the A/D data register (ADDRA to ADDRH) corresponding to that channel.
[3] Generation of A/D conversion end interrupt	After A/D conversion of all the selected channels finishes, the IR bit for the S12ADI0 interrupt is set to 1 (generate interrupt request) and a S12ADI0 interrupt request is generated when the ADCSR.ADIE bit is set to 1 (generation of S12ADI0 interrupt after scan end enabled). The 12-bit A/D converter restarts conversion of the channels selected in the ADANSA0 and ADANSA1 registers, beginning with the ANn with the lowest n number and proceeding in order.	After A/D conversion of all the selected channels finishes, the ADF bit in ADCSR is set to 1 (A/D conversion end). At this point, if the ADIE bit in ADCSR is set to 1 (generation of ADI interrupt by ADF enabled), an ADI interrupt request is generated. The A/D converter restarts conversion from the first channel selected by bits CH3 to CH0 in ADCSR.
[4] A/D conversion end	Operation items 2 and 3 are repeated as long as the ADCSR.ADST bit is not cleared to 0 and remains set to 1 (A/D conversion start). When the ADCSR.ADST bit is cleared to 0 (A/D conversion stop), A/D conversion halts, and the 12-bit A/D converter enters the standby state.	Operation items 2 and 3 are repeated as long as the ADST bit in ADCSR is not cleared to 0 and remains set to 1 (A/D conversion start). When the ADST bit in ADCSR is cleared to 0 (A/D conversion stop), A/D conversion halts, and the A/D converter enters the standby state.
[5] A/D conversion restart	Henceforth, A/D conversion of the channels selected in the ADANSA0 and ADANSA1 registers restarts when the ADCSR.ADST bit is set to 1 (A/D conversion start), beginning with the ANn with the lowest n number and proceeding in order.	Henceforth, A/D conversion from the first channel selected by bits CH3 to CH0 in ADCSR restarts when the ADST bit in ADCSR is set to 1 (A/D conversion start).

3.2.2 Points of Difference between Setting Procedures

Table 3.6 lists the points of difference between the initial setting procedures for scan mode operation.

The H8S/2378 Group and RX231 Group have different interrupt architectures and setting procedures for I/O port functions. For details, refer to section 5, Points of Difference between Interrupts, and 8.1, I/O Ports.

Table 3.6 Points of Difference between Initial Setting Procedures for Scan Mode Operation

Procedure		RX (RX231)	H8S (H8S/2378)
1	Cancel module stop state*1	MSTP(S12AD) = 0;	MSTPCR.BIT._AD = 0;
2	Disable interrupt requests	S12AD.ADCSR.BIT.ADIE = 0; IEN(S12AD, S12ADI0) = 0;	AD.ADCSR.BIT.ADIE = 0;
3	Disable A/D conversion	S12AD.ADCSR.BIT.ADST = 0;	AD.ADCSR.BIT.ADST = 0;
4	Select scan mode	S12AD.ADCSR.BIT.ADCS = 2;	AD.ADCR.BIT.SCAN = 2;
5	Select channel	S12AD.ADANSA0.WORD = 0x0007;	AD.ADCSR.BIT.CH = 2;
6	Set A/D conversion time	S12AD.ADSSTR0 = 0x58;	AD.ADCR.BIT.CKS = 3;
7	Set I/O port functions*3	PORT4.PMR.BIT.B0 = 0; PORT4.PDR.BIT.B0 = 0; MPC.P40PFS.BYTE = 0x80; PORT4.PMR.BIT.B1 = 0; PORT4.PDR.BIT.B1 = 0; MPC.P41PFS.BYTE = 0x80; PORT4.PMR.BIT.B2 = 0; PORT4.PDR.BIT.B2 = 0; MPC.P42PFS.BYTE = 0x80;	— (No processing)
8	Set interrupt control mode	— (No processing)	INTC.INTCR.BIT.INTM = 2;
9	Set interrupt priority level	IPR(S12AD, S12ADI0) = 0x01;	INTC.IPRF.BIT._AD = 1;
10	Clear peripheral function interrupt request	— (No processing)	AD.ADCSR.BIT.ADF = 0;
11	Clear interrupt request	IR(S12AD, S12ADI0) = 0;	— (No processing)
12	Enable interrupt requests	S12AD.ADCSR.BIT.ADIE = 1; IEN(S12AD, S12ADI0) = 1;	AD.ADCSR.BIT.ADIE = 1;
13	Set processor interrupt priority level	— (No processing)	set_imask_exr(0);
14	Enable maskable interrupts	setpsw_i();	— (No processing)
15	Enable A/D conversion start	S12AD.ADCSR.BIT.ADST = 1;	AD.ADCSR.BIT.ADST = 1;

Note 1. For information on the module stop function, refer to section 6, Module Stop Function.

Note 2. On the H8S/2378 Group, selection of the A/D conversion start trigger occurs simultaneously with step 15 “Enable A/D conversion start by trigger signal.”

Note 3. When using pins AN000 to AN002, set the relevant pins as general input.
(Clear bits PORT.PDR.Bm and PORT.PMR.Bm to 0 (m: 0 to 7).)

3.3 Group Scan Mode Operation

The setting procedure for group scan mode operation on the RX231 Group is presented below. The operations and setting procedures listed in Table 3.7, Group Scan Mode Operation Conditions, are described.

Table 3.7 Group Scan Mode Operation Conditions

	Operation Conditions
Item	**RX (RX231)**
Operating mode	Group scan mode
Analog input channel	Group A: AN000, AN001 Group B: AN002, AN003
A/D conversion start trigger	Group A: MTU0.TGRA compare match or input capture Group B: MTU0.TGRB compare match or input capture
Interrupt	Scan end interrupt (S12ADI0) Group B scan end interrupt (GBADI)

In group scan mode on the RX231 Group, the analog inputs of up to 24 selected channels are divided into two groups (group A and group B), and A/D conversion is performed on each group as a unit.

As in single scan mode, in scan operation A/D conversion starts from the lowest channel number and proceeds in order.

It is possible to start A/D conversion of group A and group B at different times by selecting separate scan start conditions (synchronous triggers) for group A and group B.

When scan end interrupt and group B scan end interrupt are enabled, a scan end interrupt (S12ADI0) is generated when scan operation ends on group A and a group B scan end interrupt (GBADI) is generated when scan operation ends on group B.

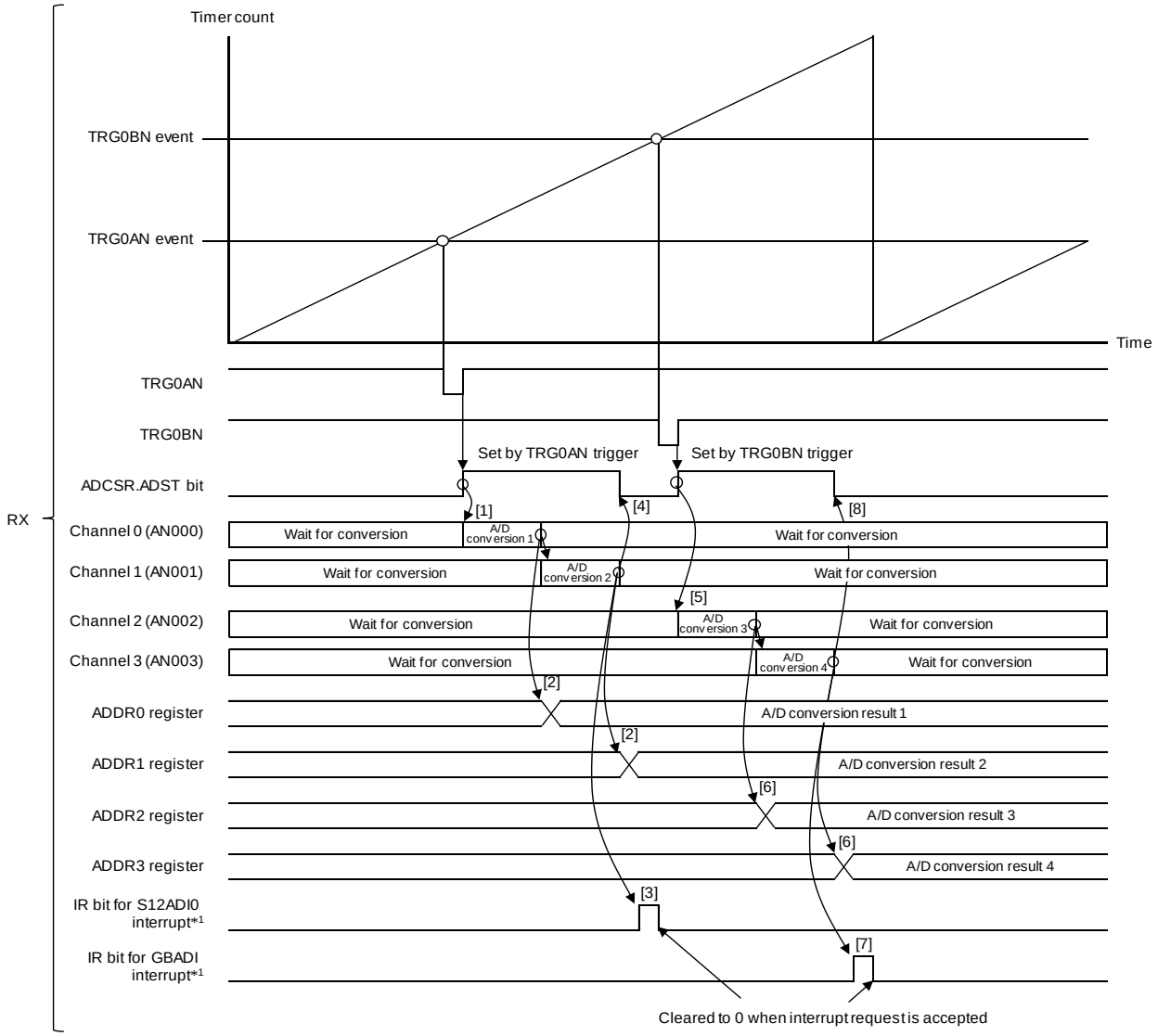
For details of group scan mode, refer to RX230 Group, RX231 Group User's Manual: Hardware.

3.3.1 Operation

Figure 3.3 is a timing chart of group scan mode operation on the RX231 Group.

Table 3.8 presents a description of group scan mode operation.

The numbers in Figure 3.3 correspond to the numbers in Table 3.8.



Note 1. The H8S/2378 Group and RX231 Group have different interrupt architectures. For details, see section 5, Points of Difference between Interrupts.

Figure 3.3 Group Scan Mode Operation Timing Chart

Table 3.8 Descriotion of Group Scan Mode Operation on RX231 Group

Item	RX (RX231) (Group Scan Mode)
[1] Group A scan start	When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the TRG0AN trigger from the MPU, scanning of group A starts. A/D conversion of the channels selected in the ADANSA0 and ADANSA1 registers proceeds, beginning with the ANn with the lowest n number and proceeding in order.
[2] Storage of group A A/D conversion results	When A/D conversion of one channel finishes, the A/D conversion result is stored in the A/D data register (ADDRy) corresponding to that channel.
[3] Generation scan end interrupt	After A/D conversion of all the channels in group A finishes, the IR bit for the S12ADI0 interrupt is set to 1 (generate interrupt request) and a S12ADI0 interrupt request is generated when the ADCSR.ADIE bit is set to 1 (generation of S12ADI0 interrupt after scan end enabled).
[4] Group A scan end	The value of the ADCSR.ADST bit remains 1 (A/D conversion start) while A/D conversion is in progress, and when A/D conversion of all the selected channels finishes it is cleared to 0 automatically, and the 12-bit A/D converter enters the standby state.
[5] Group B scan start	When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the TRG0BN trigger from the MPU, scanning of group B starts. A/D conversion of the channels selected in the ADANSB0 and ADANSB1 registers proceeds, beginning with the ANn with the lowest n number and proceeding in order.
[6] Storage of group B A/D conversion results	When A/D conversion of one channel finishes, the A/D conversion result is stored in the A/D data register (ADDRy) corresponding to that channel.
[7] Generation of group B scan end interrupt	After A/D conversion of all the channels in group B finishes, the IR bit for the GBADI interrupt is set to 1 (generate interrupt request) and a GBADI interrupt request is generated when the ADCSR.GBADI bit is set to 1 (generation of GBADI interrupt after group B scan end enabled).
[8] Group B scan end	The value of the ADCSR.ADST bit remains 1 (A/D conversion start) while A/D conversion is in progress, and when A/D conversion of all the selected channels finishes it is cleared to 0 automatically, and the 12-bit A/D converter enters the standby state.

3.3.2 Setting Procedure

Table 3.9 lists the initial setting procedure for group scan mode operation.

Table 3.9 Initial Setting Procedure for Group Scan Mode Operation

Procedure		RX (RX231)
1	Cancel module stop state*1	MSTP(S12AD) = 0;
2	Disable interrupt requests	S12AD.ADCSR.BIT.ADIE = 0; S12AD.ADCSR.BIT.GBADIE = 0; IEN(S12AD, S12ADI0) = 0; IEN(S12AD, GBADI) = 0;
3	Disable A/D conversion	S12AD.ADCSR.BIT.ADST = 0;
4	Select scan mode	S12AD.ADCSR.BIT.ADCS = 1;
5	Select channel	S12AD.ADANSA0.WORD = 0x0003; S12AD.ADANSB0.WORD = 0x000C;
6	Select A/D conversion start trigger	S12AD.ADCSR.BIT.EXTRG = 0; S12AD.ADSTRGR.BIT.TRSA = 1; S12AD.ADSTRGR.BIT.TRSB = 2;
7	Set A/D conversion time	S12AD.ADSSTR0 = 0x58; S12AD.ADSSTR1 = 0x58; S12AD.ADSSTR2 = 0x58; S12AD.ADSSTR3 = 0x58;
8	Set I/O port functions*2	PORT4.PMR.BIT.B0 = 0; PORT4.PDR.BIT.B0 = 0; MPC.P40PFS.BYTE = 0x80; PORT4.PMR.BIT.B1 = 0; PORT4.PDR.BIT.B1 = 0; MPC.P41PFS.BYTE = 0x80; PORT4.PMR.BIT.B2 = 0; PORT4.PDR.BIT.B2 = 0; MPC.P42PFS.BYTE = 0x80; PORT4.PMR.BIT.B3 = 0; PORT4.PDR.BIT.B3 = 0; MPC.P43PFS.BYTE = 0x80;
9	Set interrupt priority level	IPR(S12AD, S12ADI0) = 0x01; IPR(S12AD, GBADI) = 0x01;
10	Clear interrupt requests	IR(S12AD, S12ADI0) = 0; IR(S12AD, GBADI) = 0;
11	Enable interrupt requests	S12AD.ADCSR.BIT.ADIE = 1; S12AD.ADCSR.BIT.GBADIE = 1; IEN(S12AD, S12ADI0) = 1; IEN(S12AD, GBADI) = 1;
12	Enable maskable interrupts	setpsw_i();
13	Enable A/D conversion start by trigger signal	S12AD.ADCSR.BIT.TRGE = 1;

Note 1. For information on the module stop function, refer to section 6, Module Stop Function.

Note 2. When using pins AN000 to AN003, set the relevant pins as general input.
(Clear bits PORT.PDR.Bm and PORT.PMR.Bm to 0 (m: 0 to 7).)

3.4 Input Sampling and Scan Conversion Time on RX231 Group

Figure 3.4 shows scan conversion timing (software activation and synchronous trigger activation) on the RX231 Group.

Figure 3.5 shows scan conversion timing (asynchronous trigger activation) on the RX231 Group.

The various time durations required for scan operations activated by an A/D conversion start trigger or other condition differ on the RX231 Group. For details, refer to Table 3.12, Time Durations Required for Scan Operations on RX231 Group.

On the RX231 Group, after the scan conversion start delay time (t_D) has elapsed, disconnection detection assist processing and self-diagnostic conversion processing take place, after which A/D conversion starts.

Regarding the disconnection detection assist function and self-diagnostic function, refer to Table 3.11, Overview of Disconnection Detection Assist Function and Self-Diagnostic Function on RX231 Group.

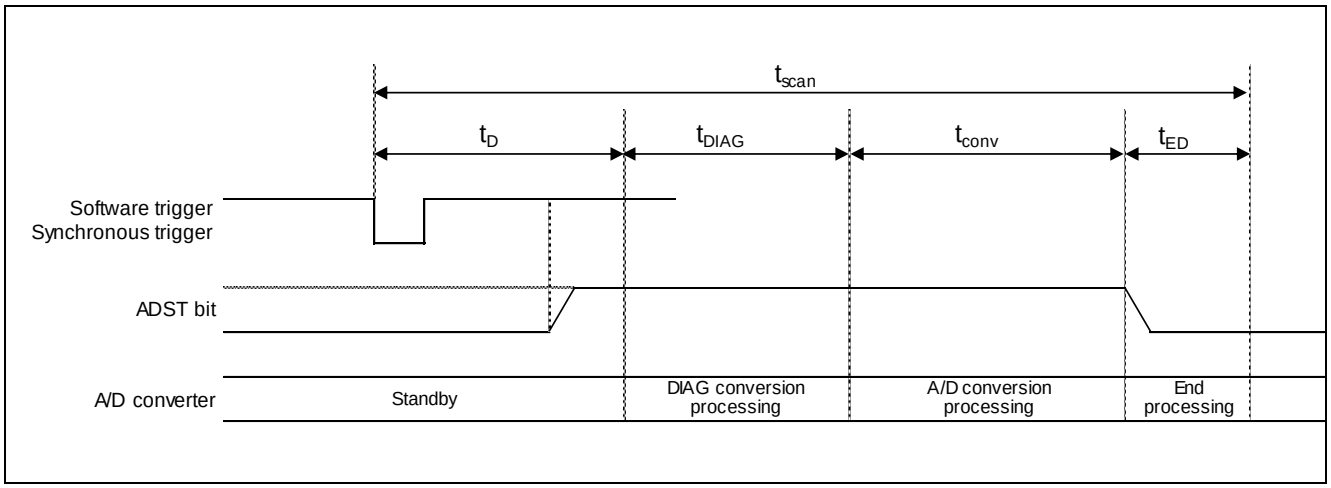


Figure 3.4 RX231 Group Scan Conversion Timing (Software Activation and Synchronous Trigger Activation)

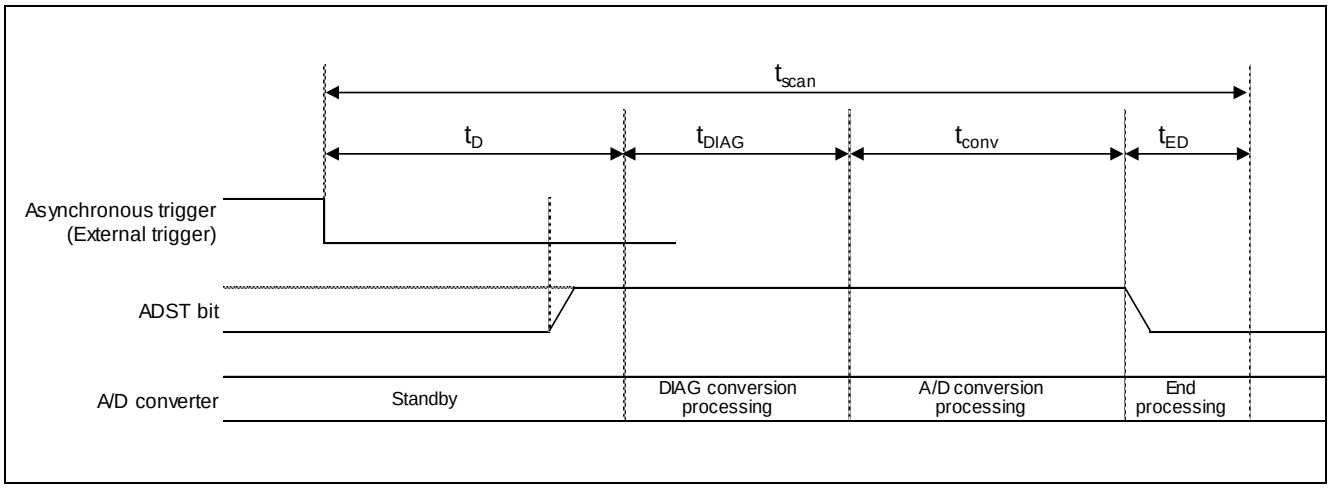


Figure 3.5 RX231 Group Scan Conversion Timing (Asynchronous Trigger Activation)

Table 3.10 lists details of the scan conversion time on the RX231 Group.

Table 3.10 RX231 Group Scan Conversion Time Details

Item			Remarks
Scan conversion time (t_{SCAN})	Scan conversion start delay time (t_D)		None
	Disconnection detection assist processing time (t_{DIS})		When disconnection detection assist function is disabled, t_{DIS} = 0.*1
	Self-diagnostic conversion time (t_{DIAG})		When self-diagnostic function is disabled, t_{DIAG} = 0.
	A/D conversion processing time (t_{CONV})	Sampling time (t_{SPL})	The sampling time can be adjusted by using the ADSSTRn registers.
		Successive conversion time (t_{SAM})	During high-speed conversion operation: 32 states (ADCLK) During small-current conversion operation: 41 states (ADCLK) High-speed conversion operation and small-current conversion operation are selectable by using the ADCSR.ADHSC bit.
	Scan conversion end delay time (t_{ED})		None

Note: The time required for A/D conversion of temperature sensor output or the internal reference voltage is fixed at 15 states (ADCLK).

Table 3.11 provides an overview of the disconnection detection assist function and self-diagnostic function on the RX231 Group.

Table 3.11 Overview of Disconnection Detection Assist Function and Self-Diagnostic Function on RX231 Group

Function	Overview	Setting	Default
Disconnection detection assist function	This function fixes the sampling capacitance charge at a fixed state before A/D conversion starts. This function makes it possible to detect when a line connected to an analog input is disconnected.	ADDISCR. ADNDIS[4:0] bits	Disabled
Self-diagnostic function	This function detects 12-bit A/D converter failures.	ADCER. DIAGM bit	Disabled

For details of the disconnection detection assist function and self-diagnostic function, refer to RX230 Group, RX231 Group User's Manual: Hardware.

The scan conversion time (t_{SCAN}) for single scan operation where n is the number of selected channels is expressed as follows:

$t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

However, in cases where the sampling time (t_{SPL}) differs among the selected channels, ($t_{CONV} \times n$) must be replaced by the sum total of the sampling time (t_{SPL}) and successive conversion time (t_{SAM}) for all of the selected channels.

The duration of the first cycle during continuous scan operation is the single scan t_{SCAN} value with t_{ED} omitted. The duration of the second and subsequent cycles during continuous scan operation is ($t_{DIS} \times n$) + t_{DIAG} + t_{DSD} + ($t_{CONV} \times n$).

Table 3.12 lists the various time durations required for scan operations on the RX231 Group.

The required time durations are indicated in numbers of cycles of the peripheral module clock (PCLK) and A/D conversion clock (ADCLK). PCLK refers to PCLKB and ADCLK refers to PCLKD. PCLKB and PCLKD can each be specified by setting a division ratio in the clock generation circuit.

By means of these division ratio settings, the frequency ratio of PCLK and ADCLK can be set as follows:

PCLK:ADCLK frequency ratio = 1:1, 1:2, 1:4, 2:1, 4:1, or 8:1

For information on clocks, refer to section 9, Clock Generation Circuit, in RX230 Group, RX231 Group User's Manual: Hardware.

Table 3.12 Time Durations Required for Scan Operations on RX231 Group

Item			Symbol		Type/Condition: Synchronous Trigger*6	Type/Condition: Asynchronous Trigger	Type/Condition: Software Trigger	Unit
Scan start processing time*1*2	A/D conversion of group A in group A priority control operation*3	Group B halted (group A activated after group B stopped by group A A/D conversion source)	t_D		3 PCLK + 6 ADCLK	—	—	Cycles
		Group B not halted (activated by group A A/D conversion source)			2 PCLK + 4 ADCLK	—	—	
	A/D conversion with self-diagnostic function enabled	Self-diagnostic conversion start			2 PCLK + 6 ADCLK	4 PCLK + 6 ADCLK	6 ADCLK	
	Other than above				2 PCLK + 4 ADCLK	4 PCLK + 4 ADCLK	4 ADCLK	
Disconnection detection assist processing time			t_{DIS}		ADDISCR.ADNDIS[3:0] setting value (initial value: 00h) × ADCLK*4			
Self-diagnostic conversion time*1	Sampling time		t_{DIAG}	t_{SPL}	ADSSTR0 setting value (initial value: 0Dh) × ADCLK*5			
	Successive conversion time	12-bit conversion precision		t_{SAM}	32 ADCLK (high-speed conversion operation)			
					41 ADCLK (small-current conversion operation)			
	Normal A/D conversion start after self-diagnostic conversion end			t_{DED}	2 ADCLK			
	Self-diagnostic conversion start after conversion of last channel in continuous scan mode			t_{DSD}	2 ADCLK			
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	ADSSTRn (n = 0 to 7, L, T, O) setting value (initial value: 0Dh) × ADCLK*5			
	Successive conversion time	12-bit conversion precision		t_{SAM}	32 ADCLK (high-speed conversion operation)			
					41 ADCLK (small-current conversion operation)			
Scan end*1			t_{ED}		1 PCLK + 3 ADCLK*7			

Note 1. Refer to Figure 3.4 and Figure 3.5 for the timing of t_D, t_{DIAG}, t_{CONV}, and t_{ED}.
Note 2. Maximum duration from software write or trigger input to A/D conversion start.
Note 3. Group A priority control operation can be enabled in group scan mode. During group A priority control operation, if a group A trigger input occurs during group B A/D conversion, group B A/D conversion operation is halted and group A A/D conversion operation takes place.
For details, refer to RX230 Group, RX231 Group User's Manual: Hardware.
Note 4. Fixed at 0Fh (15 ADCLK) during A/D conversion of temperature sensor output or the internal reference voltage.
Note 5. The necessary sampling time (ns) is determined according to the voltage condition. For details, refer to 50.5, A/D Conversion Characteristics, in RX230 Group, RX231 Group User's Manual: Hardware.
Note 6. Not including the time consumed in the route from timer output to trigger input.
Note 7. 2 PCLK + 3 ADCLK when ADCLK is operating at a higher frequency than PCLK (when the PCLK:ADCLK frequency ratio is set to 1:2 or 1:4).

3.5 External Trigger Input Timing

Figure 3.6 shows a timing chart of the period from asynchronous trigger input to A/D conversion end on the RX231 Group.

Table 3.13 lists the operation conditions for the RX231 Group timings shown in Figure 3.6.

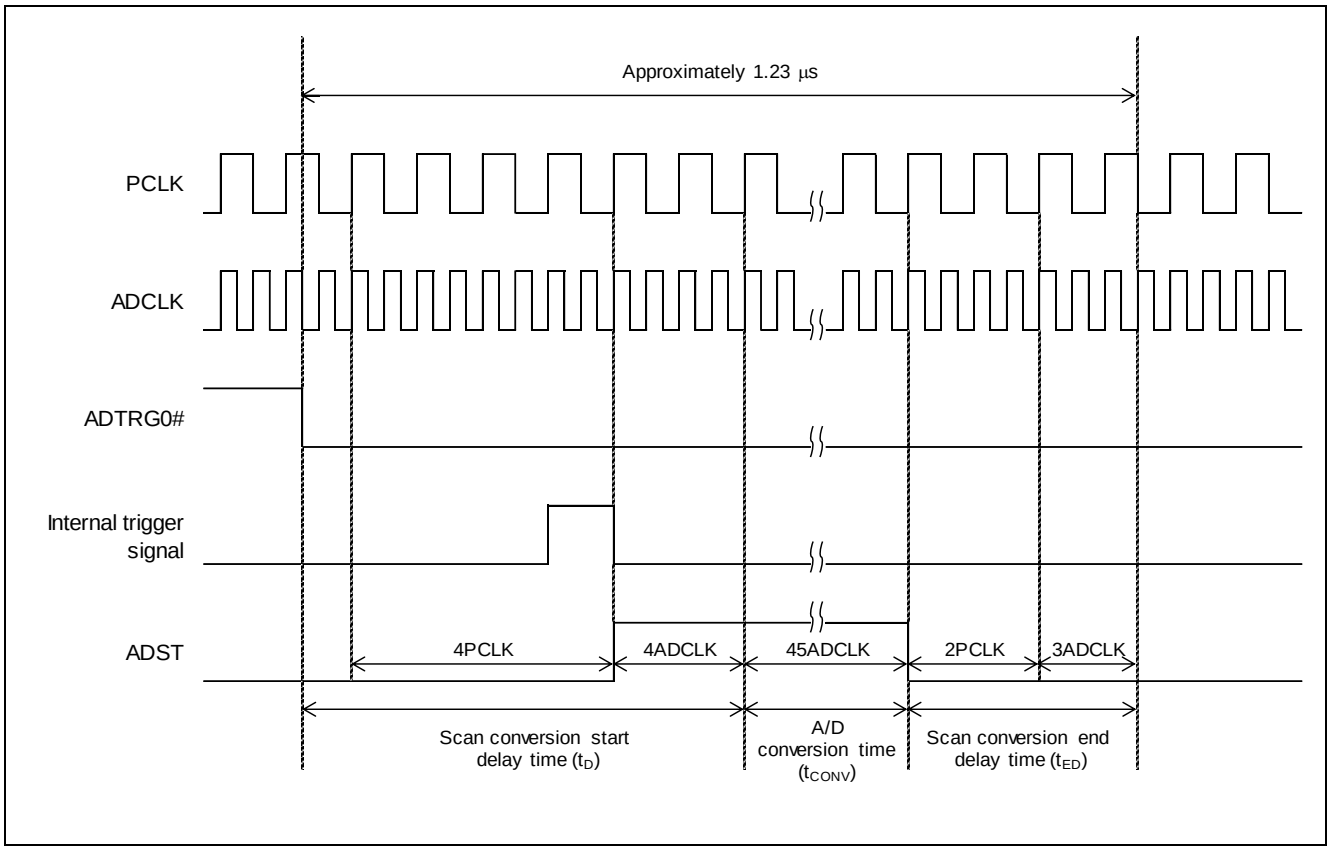


Figure 3.6 Timing Chart of Asynchronous Trigger Input to A/D Conversion End on RX231 Group

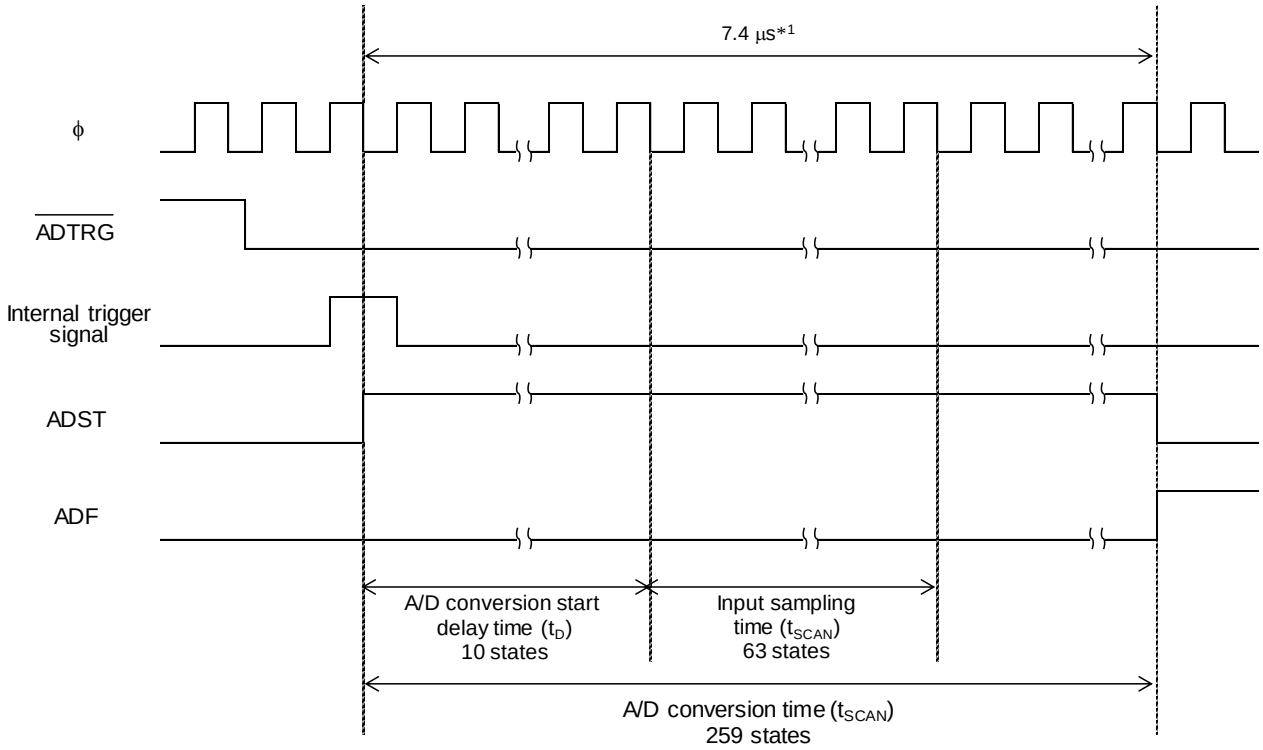
Table 3.13 RX231 Group Timing Operation Conditions

Item	Condition
A/D conversion clock (ADCLK)	52 MHz
Peripheral module clock (PCLK): A/D conversion clock (ADCLK) frequency ratio	PCLK:ADCLK = 1:2
Operating mode	Single scan mode
Analog input channels on which A/D conversion is performed	1 channel
Conversion mode	High-speed conversion operation
Disconnection detection assist function	Not used
Self-diagnostic function	Not used
Sampling state count (ADSSTRn setting value)	13 states

Note: For details of the scan conversion time, refer to 3.4, Input Sampling and Scan Conversion Time on RX231 Group.

Figure 3.7 shows a timing chart of the period from external trigger input to A/D conversion end on the H8S/2378 Group.

Table 3.13 lists the operation conditions for the H8S/2378 Group timings shown in Figure 3.7.



Note 1. The A/D conversion time (t_{SCAN}) duration should be set to 7.4 µs or more.

Note: The A/D conversion start delay time (t_D) varies due to changes in the timing of writes to ADCSR. This also results in changes to the A/D conversion time (t_{SCAN}). The state counts shown in the figure indicate minimum values.

Figure 3.7 Timing Chart of External Trigger Input to A/D Conversion End on H8S/2378 Group

Table 3.14 H8S/2378 Group Timing Operation Conditions

Item	Condition
Operating clock	35 MHz
Operating mode	Single mode
A/D conversion time (setting value of CKS1 and CKS0 in ADCR)	266 states (max.)

4. Usage Notes

4.1 Permissible Signal Source Impedance

Figure 4.1 shows an equivalent circuit of an analog input pin and external sensor.

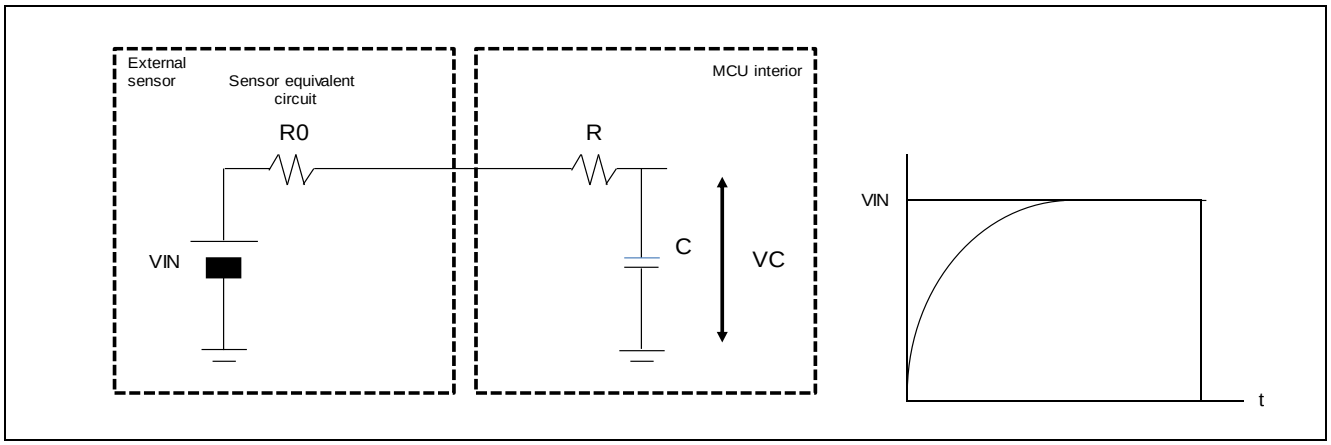


Figure 4.1 Analog Input Pin and External Sensor Equivalent Circuit

The design of the analog inputs of the RX231 Group and H8S/2378 Group is guaranteed to provide conversion precision of input signals when the signal source impedance does not exceed that shown in Table 4.1.

When performing conversion of the input on one pin only in single mode on the H8S/2378 Group or single scan mode on the RX231 Group, the actual input load is equal to the internal input resistance alone when a large external capacitance is provided and the signal source impedance not an issue. However, such a configuration acts as a low-pass filter, so conversion may not be able to track analog signals with a large differential coefficient.

When performing conversion of high-speed analog input signals or when performing conversion of input from multiple pins in scan mode, a low-impedance buffer should be inserted into the circuit.

Table 4.2 lists internal input resistance values for the RX231 Group and H8S/2378 Group.

Table 4.1 Signal Source Impedance at which Conversion Precision Is Guaranteed

Item	RX (RX231)	H8S (H8S/2378)
R0	0.5 kΩ or less	5 kΩ or less

Table 4.2 Internal Input Resistance of RX231 Group and H8S/2378 Group

Item	RX (RX231)	H8S (H8S/2378)
R	2.6 kΩ	10 kΩ

4.2 Setting Ranges of Analog Power Supply Pin, Etc.

Table 4.3 lists points of difference in voltage setting ranges.

Exceeding the voltage setting ranges of the RX231 Group and H8S/2378 Group indicated in Table 4.3 could have an adverse effect on the reliability of these devices.

Table 4.3 Points of Difference in Voltage Setting Ranges

Item	RX (RX231)	H8S (H8S/2378)
Analog input pin setting ranges	The voltage applied to analog input pins ANn should be within the range of VREFL0 ≤ VAN ≤ VREFH0. The voltage applied to analog input pins ANn (n = 000 to 007) should be AVSS0 ≤ VAN ≤ AVCC0. The voltage applied to analog input pins ANn (n = 016 to 031) should be VSS ≤ VAN ≤ VCC and AVSS0 ≤ VAN ≤ AVCC0.	The voltage applied to analog input pins ANn during A/D conversion should be within the range of AVss ≤ ANn ≤ Vref.
Reference voltage setting range	The reference voltage setting range using the VREFH0 pin should be VREFH0 ≤ AVCC0.	The reference voltage setting range using the Vref pin should be Vref ≤ AVcc.
Relationships between power supply pins	The relationship of AVSS0 and VSS should be AVSS0 = VSS. When performing A/D conversion on analog input pins AN016 to AN031, ensure that AVCC0 = VCC. Also, connect 0.1 μF capacitors as close as possible to the power supply pins in a closed loop configuration as shown in Table 4.2, such that VREFL0 = AVSS0 = VSS at the supply source. When not using the 12-bit A/D converter, ensure that VREFH0 = AVCC0 = VCC and VREFL0 = AVSS0 = VSS.	The relationship of AVcc and AVss to Vcc and Vss should be AVcc ≥ Vcc and AVss = Vss, and the AVcc and AVss pins should be left open when not using the A/D converter.

Table 4.2 shows a connection example of the power supply pins of the RX231 Group.

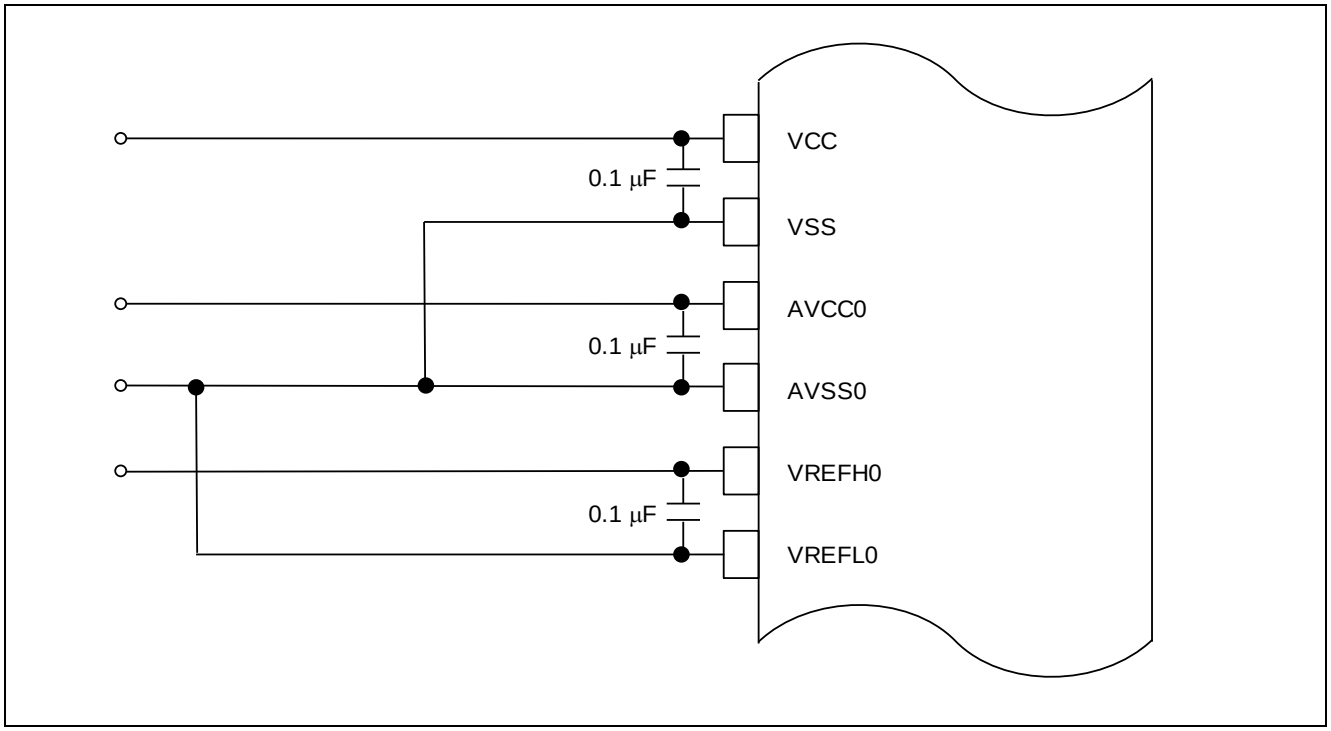


Figure 4.2 Connection Example of RX231 Group Power Supply Pins

4.3 Notes on Board Design

When designing boards populated with RX231 Group or H8S/2378 Group microcontrollers, separate the digital and analog circuits to the extent possible. In addition, do not allow the signal lines of digital and analog circuits to cross or run too close to each other. If these design principles are not followed, noise could affect the analog signals, diminishing the accuracy of A/D-converted values.

Isolate the analog input pins, reference power supply pin, reference ground pin (RX231 Group only), and analog power supply pin from the digital circuits by means of the analog ground pin.

Also ensure that the analog ground pin has a stable one-point connection to ground on the board.

Table 4.4 lists pins on the RX231 Group and H8S/2378 Group.

Table 4.4 RX231 Group and H8S/2378 Group Pins

Pin	RX (RX231)	H8S (H8S/2378)
Analog input pins	AN000 to AN007, AN016 to AN031	AN0 to AN15
Reference power supply pin	VREFH0	Vref
Reference ground pin	VREFL0	None
Analog power supply pin	AVCC0	AVcc
Analog ground pin	AVSS0	AVss

On the RX231 Group the reference voltage can be selected by setting the ADHVREFCNT.HVSEL[1:0] bits and LVSEL bit, as follows:

- High-potential side reference voltage: Selectable between AVCC0 and VREFH0
- Low-potential side reference voltage: Selectable between AVSS0 and VREFL0

These settings allow AVCC0 or AVSS0 to be used as the reference voltage.

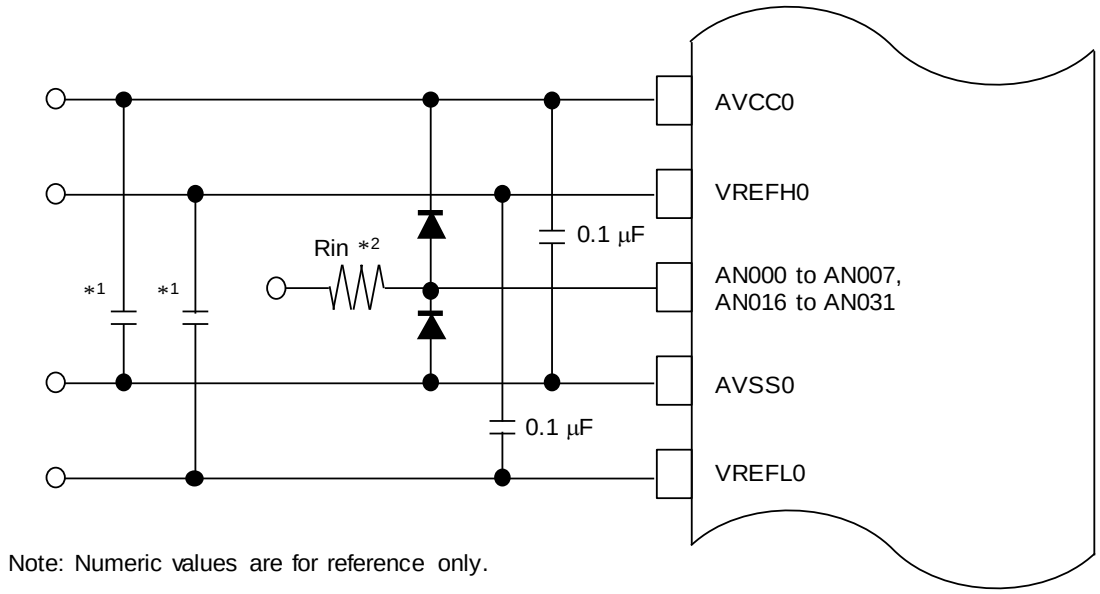
The default settings are AVCC0 selected as the high-potential side reference voltage and AVSS0 as the low-potential side reference voltage.

4.4 Notes on Anti-Noise Measures

On both the RX231 Group and H8S/2378 Group it is necessary to connect a protection circuit to prevent damage to the analog input pins caused by abnormal voltages such as large surges.

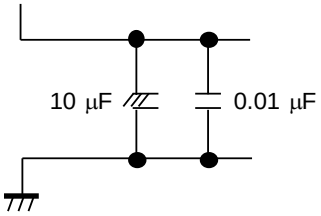
Figure 4.3 shows an example analog input protection circuit for the RX231 Group.

Figure 4.4 shows an example analog input protection circuit for the H8S/2378 Group.



Note: Numeric values are for reference only.

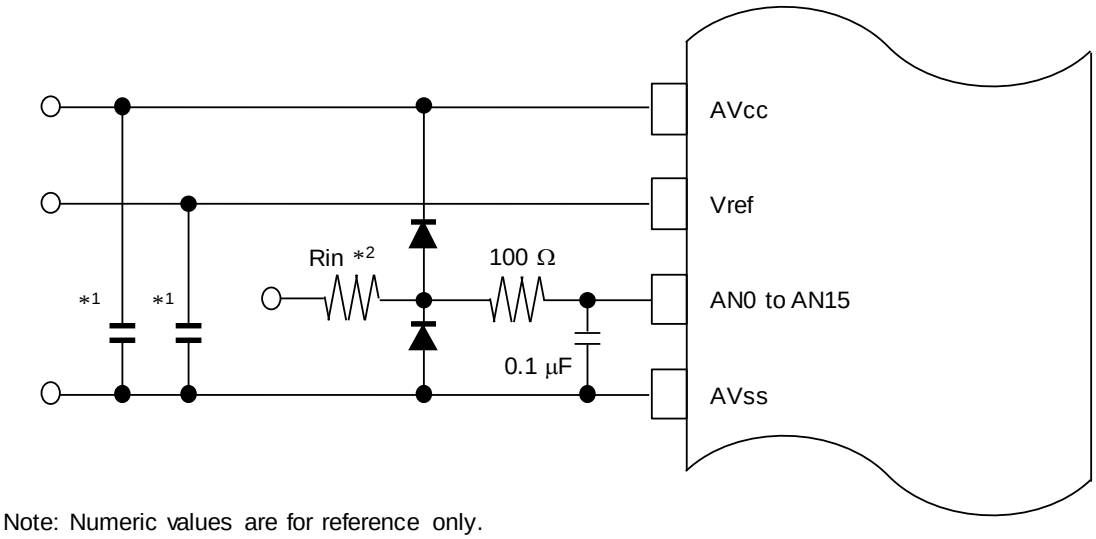
Note 1.



Note 2. Rin: signal source impedance

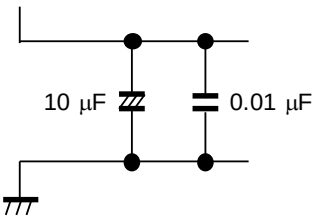
Figure 4.3 Example Analog Input Protection Circuit for RX231 Group

On the RX231 Group, insert capacitors between AVCC0 and AVSS0, and between VREFH0 and VREFL0, and connect a protection circuit to the analog input pins (AN000 to AN007 and AN016 to AN031), as shown in Figure 4.3.



Note: Numeric values are for reference only.

Note 1.



Note 2. Rin: input impedance

Figure 4.4 Example Analog Input Protection Circuit for H8S/2378 Group

On the H8S/2378 Group, connect a protection circuit between AVcc and AVss, as shown in Figure 4.4. The bypass capacitor connected to AVss and the filter capacitors connected to AN0 to AN15 must be connected to AVss without fail.

Note that connecting capacitors for use as filters can cause errors by levelling the input current on AN0 to AN15. Also, when A/D conversion is performed frequently, as in scan mode, the charging current flowing to the capacitance of the A/D converter's internal sample-and-hold circuit can exceed the current input via the input impedance (Rin), resulting in errors in the voltage of the analog input pins. Therefore, careful consideration should be given to the circuit constants before deciding the final values.

5. Points of Difference between Interrupts

In contrast to the H8S/2378 Group, on the RX231 Group, in addition to interrupt enable and interrupt request bits in the registers of each peripheral function, there are interrupt enable and interrupt request bits in the registers of the interrupt controller for the peripheral functions.

Table 5.1 lists the points of difference between the interrupt-related resources of the A/D converter.

The IERm registers (m = 02h to 1Fh) and IRn registers (n = interrupt vector number) listed in Table 5.1 are interrupt controller registers.

For the interrupt sources corresponding to the bits in the IERm registers and the interrupt vector numbers, refer to the section describing the interrupt controller in User's Manual: Hardware.

Table 5.1 Points of Difference between A/D Converter Interrupt-Related Resources

		RX (RX231)		H8S (H8S/2378)
Item		**S12ADI0**	**GBADI**	**ADI**
Interrupt enable register (enable bit)	Peripheral function	ADCSR.ADIE	ADCSR.GBADIE	ADCSR.ADIE
	Interrupt controller	IER0C.IEN6	IER0C.IEN7	Not available.
Interrupt request register (source flag)	Peripheral function	Not available.	Not available.	ADCSR.ADF
	Interrupt controller	IR102.IR	IR103.IR	Not available.

Interrupts can be accepted on the RX231 Group when the following conditions are met:

- The I flag (PSW.I bit) is set to 1.
- The interrupt is enabled in the IER and IPR registers of the ICU.
- Interrupt requests are enabled by the corresponding peripheral function interrupt request enable bit.

Table 5.2 is a comparative listing of the interrupt generation conditions on the RX231 Group and H8S/2378 Group.

Table 5.2 Comparative Listing of Interrupt Generation Conditions on RX231 Group and H8S/2378 Group

Item	RX (RX231)	H8S (H8S/2378)
Interrupt enable bit (I bit)	Setting the I bit in the PSW register to 1 (enabled) enables acceptance of maskable interrupts.	In interrupt control mode 0, setting the I bit to 0 (enabled) in the CCR register enables acceptance of maskable interrupts. In interrupt control mode 2 the I bit in the CCR register is not used.
Processor interrupt priority level	Only interrupt requests with a higher priority level than that indicated by the IPL[3:0] bits in the PSW register are accepted.	In interrupt control mode 2 only interrupt requests with a higher priority level than that indicated by bits I2 to I0 in the EXR register are accepted. In interrupt control mode 0 the bits I2 to I0 in the EXR register is not used.
Interrupt priority level	Set in the IPR register.	In interrupt control mode 0 the default settings are used. In interrupt control mode 2 the IPR register settings are used.
Interrupt request flag	The interrupt controller manages all interrupt status flags for peripheral functions, external pins, NMI interrupts, etc.	The interrupt controller manages interrupt status flags for external interrupts, and interrupt status flags for internal interrupt sources are managed within each on-chip peripheral function.
Interrupt request enable	Set in the IER register for maskable interrupts and in the NMIER register for non-maskable interrupts.	IRQ interrupts are enabled by settings in the IER register.
Peripheral function interrupt enable	Interrupts can be enabled or disabled by each peripheral function.	

Table 5.3 lists points of difference in the enabling and priority levels of processor interrupts.

On the RX231 Group the processor interrupt priority level is 0 (lowest level) by default when the PSW.I bit is set to 1 (interrupt enabled), so maskable interrupts are enabled.

On H8S/2378 Group, in interrupt control mode 0, processor interrupt priority levels are not used when the CCR.I bit is cleared to 0 (interrupt enabled), so maskable interrupts are enabled.

On H8S/2378 Group, in interrupt control mode 2, the processor interrupt priority level is 7 (highest level) by default, so maskable interrupts are enabled by setting bits I2 to I0 in EXR.

Table 5.3 Points of Difference in Enabling and Priority Levels of Processor Interrupts

		H8S (H8S/2378)	
Item	**RX (RX231)**	**Interrupt Control Mode 0**	**Interrupt Control Mode 2**
Interrupt enable default value	PSW.I bit: 0 (interrupt mask)	CCR.I bit: 1 (interrupt mask)	Not used
Processor interrupt priority level default value	PSW.IPL[3:0] bits: 0000b (lowest level)	Not used	EXR bits I2 to I0: 111b (highest level)
Operation after a reset	Maskable interrupts are not accepted.		

Table 5.4 lists some of the embedded functions used for enabling interrupts.

Table 5.4 Embedded Functions Used for Enabling Interrupts (Partial Listing)

	Description		
		H8S (H8S/2378)	
Item	**RX (RX231)**	**Interrupt Control Mode 0**	**Interrupt Control Mode 2**
Processor interrupt enable setting	setpsw_i(); *1	set_imask_ccr(0); *1	Not used
Processor interrupt priority level setting (setting = 0)	set_ipl(0); *1	Not used	set_imask_exr(0); *1

Note 1. The file machine.h must be included.

For details, refer to the sections describing the interrupt controller (ICU), CPU, and peripheral functions used in User's Manual: Hardware.

6. Module Stop Function

On the H8S/2378 Group and RX231 Group it is possible to halt the functioning of individual peripheral modules.

Power consumption can be reduced by transitioning unused peripheral modules to the module stop state. Modules not listed in Table 6.1 are in the module stop state after a reset.

Table 6.1 Modules that Operate under Initial Settings on RX231 Group and H8S/2378 Group

RX (RX231)	H8S (H8S/2378)
DMAC, DTC, RAM	EXDMAC, DMAC, DTC

When a module is in the module stop state, its registers cannot be read or written to.

Before using any module not listed in Table 6.1, it is necessary to cancel the module stop state and then make initial settings.

For details, refer to the section describing the low power consumption functions in User's Manual: Hardware.

7. Register Write Protection Function

On the RX231 Group it is possible to protect important registers from being overwritten if program runaway occurs. The protect register (PRCR) is used to specify the registers that are protected by this function.

Register protection can be enabled for the clock generation circuit–related registers, flash memory–related registers, operating mode–related registers, low power consumption function–related registers, low-power timer–related registers, LVD–related registers, and software reset register.

For details, refer to the section on the register write protection function in User's Manual: Hardware.

8. Key Points when Migrating from H8S to RX

Some points to keep in mind when migrating from the H8S/2378 Group to the RX231 Group are described below.

8.1 I/O Ports

On the RX231 Group it is necessary to make settings to the MPC to assign pins to peripheral function I/O signals.

To apply I/O control to a pin on the RX231 Group, make the following two settings:

- PFS register of MPC: Select the peripheral function to be assigned to the pin.
- PMR register of I/O port: Select whether to assign the pin to a general I/O port or a peripheral function.

Table 8.1 provides a comparative listing of I/O settings for peripheral function pins on the RX231 Group and H8S/2378 Group.

Table 8.1 Comparison of I/O settings for Peripheral Function Pins on RX231 Group and H8S/2378 Group

Function	RX (RX231)	H8S (H8S/2378)
Pin function selection	I/O pins for peripheral functions can be assigned from a selection of multiple pins by making settings in the PFS register.	Pins can be switched between general I/O port and peripheral function settings and pin functions selected through combinations of the MCU operating mode, the setting of the SYSCR.EXPE bit, the PFCR registers, the DDR registers, and the settings of the various peripheral functions.
General I/O port/peripheral function switching	Settings in the PMR register can be used to select whether specific pins are used as I/O ports or as peripheral functions.	

For details, refer to the sections describing the multi-function pin controller (MPC) and I/O ports in User's Manual: Hardware.

8.2 I/O Register Macros

The macro definitions listed below are contained in the I/O register definition file (iodefine.h) of the RX231 Group.

Using macro definitions can make program code easier to read.

Table 8.2 lists macro usage examples.

Table 8.2 Macro Usage Examples

Macro	Usage Example
IR(“module name”,”bit name”)	IR(MTU0,TGIA0) = 0; Clears the IR bit corresponding to TGIA0 of MTU0 to 0 (clear interrupt request).
DTCE(“module name”,”bit name”)	DTCE(MTU0,TGIA0) = 1; Sets the DTCE bit corresponding to TGIA0 of MTU0 to 1 (enable DTC start).
IEN(“module name”,”bit name”)	IEN(MTU0,TGIA0) = 1; Sets the IEN bit corresponding to TGIA0 of MTU0 to 1 (enable interrupt).
IPR(“module name”,”bit name”)	IPR(MTU0,TGIA0) = 0x02; Sets the IPR bits corresponding to TGIA0 of MTU0 to 2 (interrupt priority level 2).
MSTP(“module name”)	MSTP(MTU) = 0; Clears the module stop setting bit of MTU0 to 0 (cancel module stop state).
VECT(“module name”,”bit name”)	#pragma interrupt(Excep_MTU0_TGIA0(vect=VECT(MTU0,TGIA0))) Declares the interrupt function corresponding to TGIA0 of MTU0.

8.3 Embedded Functions

On the RX231 Group interrupt functions are provided to implement control register settings or special instructions. To use these embedded functions, include the file machine.h.

Table 8.3 lists (examples of) points of difference between control register settings and special instructions on the RX231 Group and H8S/2378 Group.

Table 8.3 Points of Difference between Control Register Settings and Special Instructions on RX231 Group and H8S/2378 Group (Example)

	Format	
Item	**RX (RX231)**	**H8S (H8S/2378)**
Set I flag to 1.	setpsw_i(); ∗1	set_imask_ccr(1); ∗1∗2
Clear I flag to 0.	clrpsw_i(); ∗1	set_imask_ccr(0); ∗1∗2
Expand to WAIT instruction.	wait(); ∗1	None
Expand to NOP instruction.	nop(); ∗1	nop(); ∗1

Note 1. It is necessary to include the file machine.h.

Note 2. I = 1 means enable interrupts on the RX231 Group, and I = 1 means mask interrupts on the H8S/2378 Group.

9. Reference Documents

User's Manual: Hardware

H8S/2378 Group, H8S/2378R Group Hardware Manual Rev.7.00 (REJ09B0109-0700)
RX230 Group and RX231 Group User's Manual: Hardware Rev.1.10 (R01UH0496EJ0110)
(The latest versions can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest versions can be downloaded from the Renesas Electronics website.)

User's Manual: Development Environment

CC-RX Compiler User's Manual Rev.1.05 (R20UT3248EJ0105)
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor
Compiler Package Ver.6.01 User's Manual (REJ10B0161-0100)
(The latest versions can be downloaded from the Renesas Electronics website.)

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Jul. 13, 2018	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0