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Harris Analog

HA-5002 SPICE BUFFER AMPLIFIER MACRO-MODEL

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Introduction

This application note describes the SPICE macro-model for the HA-5002, a wide bandwidth, high output current, buffer amp. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the Spice net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to help relate the SPICE listing to the schematic. The model is designed to emulate a typical rather than a worst case part. Most AC and DC parameters are simulated. Significant poles and zeros are included to give the most accurate AC and transient simulation with minimum complexity.

Model Description

CI and LI represent the input parasitics of the HA-5002, with voltage source VIO modelling the offset voltage. Diodes DI1, DI2, DO1, and DO2 with current sources IP and IN and capacitors CP and CN model input current and slew rate. Power supply current is modeled by current source IPS. The actual part has 2 positive and 2 negative power supplies, whereas this macromodel has only one of each.

The most significant singularities of the HA-5002 are modeled by EP1-3 and GP4, RP1-4, CP1-4, and LP4.

Source EO and elements RO, LO, and CO model the output stage and package parasitics.

Parameters Not Modeled

To maintain a simple macro-model not all op amp parameters are modeled. Most of the parameters not modeled are listed below:

- Power Supply Range
- Temperature Effects
- Input and Output Voltage Limits.
- Input Voltage and Current Noise.
- Tolerances for Monte Carlo Analysis
- Power Supply Current Tracking of Output Current.

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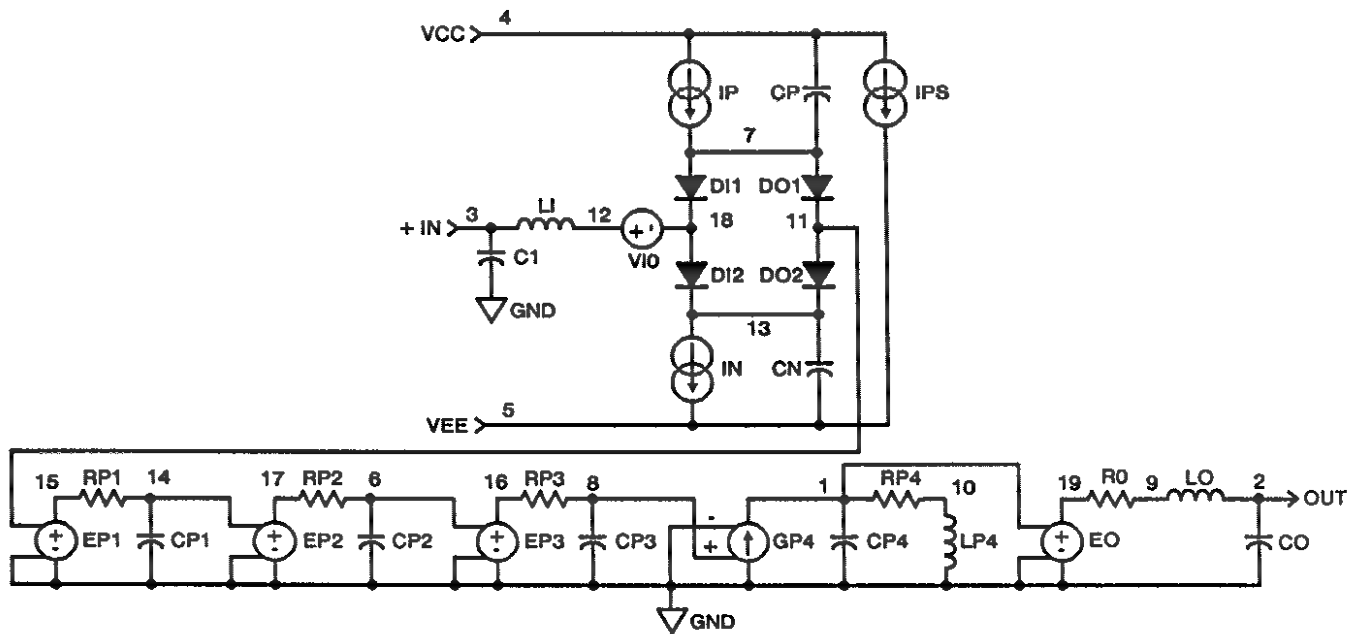
Spice Listing

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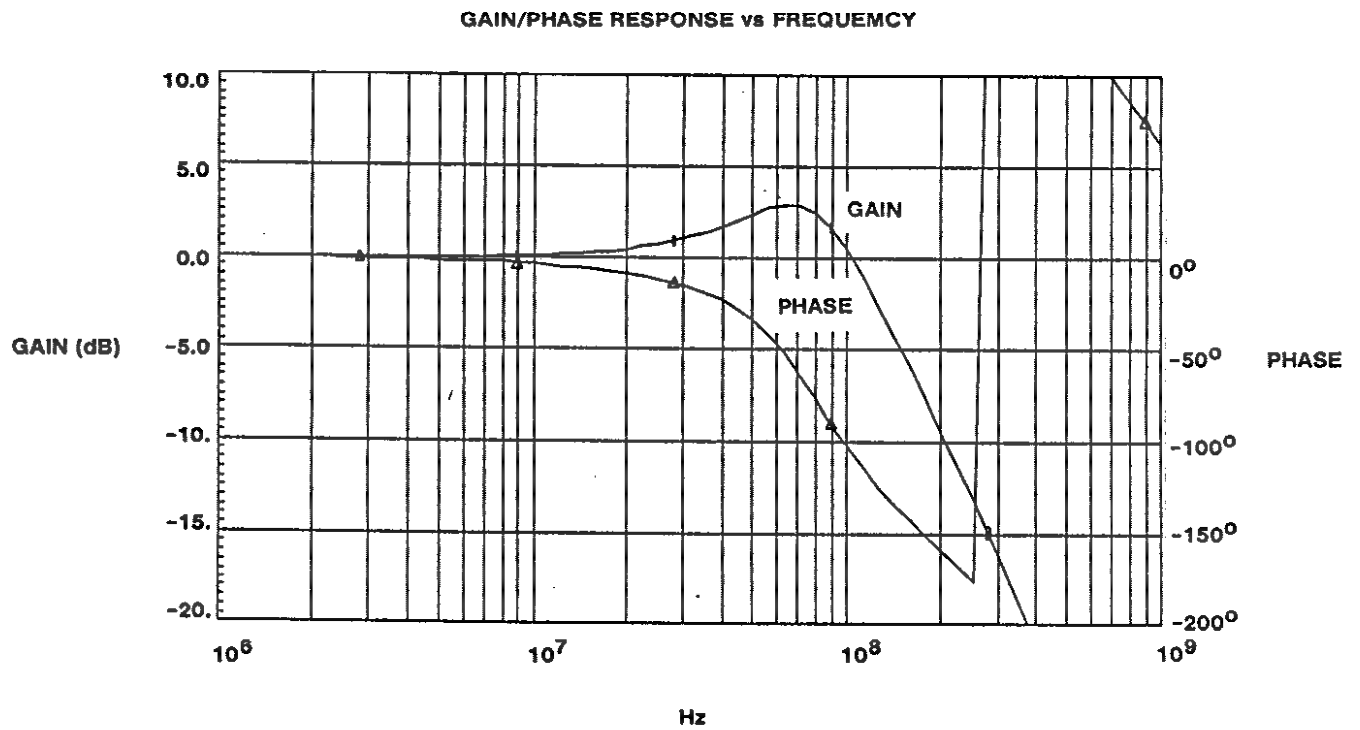
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*
*HA-5002 MACRO-MODEL
*REV:7-29-91
*D.W. RIEMER
*
*PINOUT:      IN  VCC  VEE  OUT
*
.SUBCKT HA5002 3 4 5 2
.MODEL D1  D   IS=5.57E-11  N=1 RS=10
.MODEL D2  D   IS=3E-11    N=1 RS=10
*
*INPUT STAGE
*OFFSET VOLTAGE MAY BE VARIED BY
*ADJUSTING THE VALUE OF SOURCE VIO.
*
CI 3 0 +1E-12
LI 3 12 +2E-09
VIO 12 18 +3E-03
IP 4 7 +1E-05
CP 4 7 +8E-05
IN 13 5 +7E-06
CN 13 5 6.66E-15
DO2 11 13 D2
DI2 18 13 D2
DO1 7 11 D2
DI1 7 18 D1
*
*SINGULARITES
*GAIN MAY BE ADJUSTED BY CHANGING
*THE VALUE OF EP1 (0.995->?)
*
EP1 15 0 11 0 0.995
EP2 17 0 14 0 1
EP3 16 0 6 0 1
GP4 0 1 8 0 1
RP1 15 14 600
RP2 17 6 350
RP3 16 8 100
RP4 1 10 1
CP1 14 0 +1E-12
CP2 6 0 +1E-12
CP3 8 0 +1E-12
CP4 1 0 +2E-09
LP4 10 0 +2E-09
*
*OUTPUT STAGE
*
IPS 4 5 +8.3E-03
EO 19 0 1 0 1
RO 19 9 3
LO 9 2 +1E-09
CO 2 0 +1E-12
.ENDS HA5002

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Macro-Model Schematic

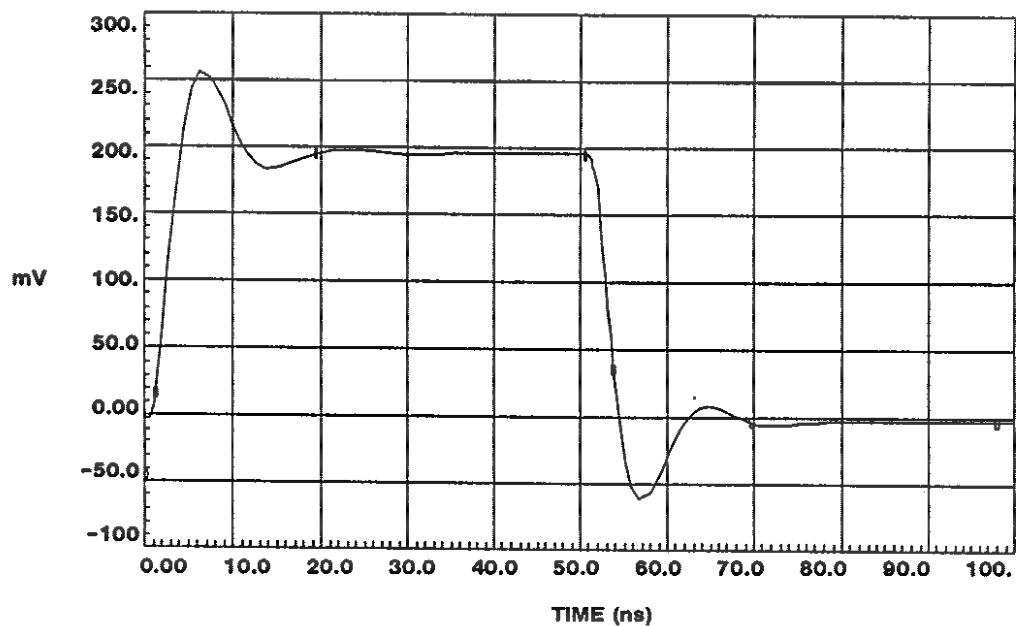


Model Performance



Model Performance (Continued)

SMALL SIGNAL RESPONSE



LARGE SIGNAL RESPONSE

