

ISL7109x and ISL71010: Stability Region and Trim Range for Precision Voltage References

Introduction

This application note discusses the three most commonly asked questions about the ISL7109x and ISL71010 families of series voltage references:

- What is the region of stable operation with regards to compensation and output capacitors?
- How to fine trim the output voltage?
- How to alter the output voltage over a wider voltage range?

Figure 1 shows the simplified block diagram of the series voltage reference, emphasizing the functional blocks that accomplish the above tasks.

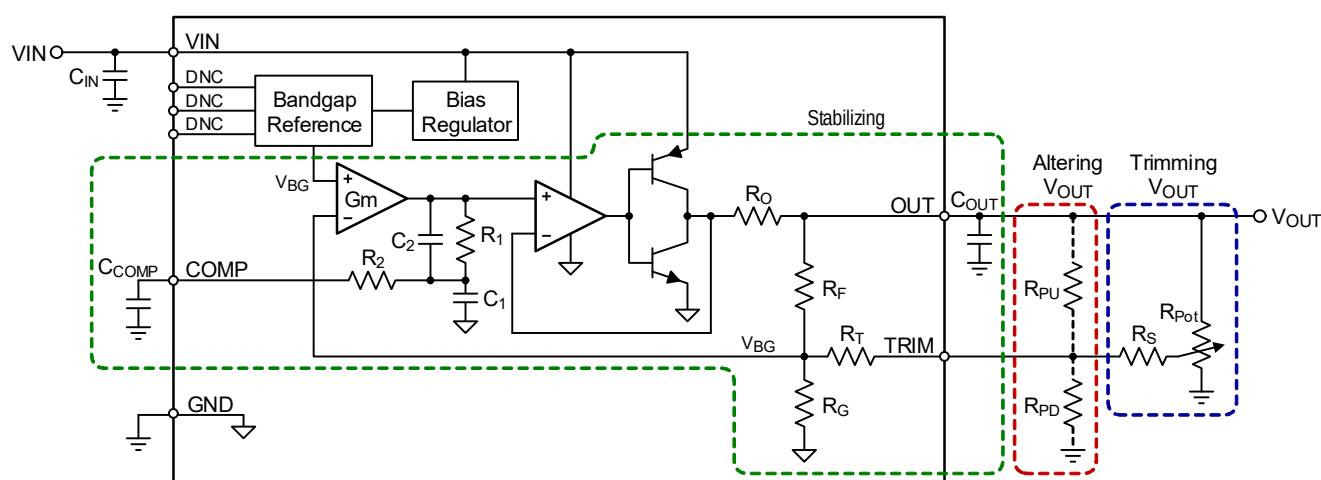


Figure 1. Simplified Block Diagram

The voltage references covered by this application note are ISL71090SEH12, ISL71091SEH20, ISL71090SEH25, ISL71091SEH33, ISL71091SEH40, ISL71090SEH50, ISL71090SEH75, ISL71091SEH10 in ceramic package, and ISL71010B25 and ISL71010B50 in plastic package.

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1. C_{OUT} versus C_{COMP} Stability Region

The ISL7109x and ISL71010 voltage references are designed to be stable, just using the internal compensation network that consists of R_1 , C_1 , and C_2 (Figure 2). The range of the applicable output capacitance, however, is limited to $C_{OUT} = 0$ to 200pF and $C_{OUT} = 10$ n to 200nF. For larger C_{OUT} values, the addition of an external compensation capacitor (C_{COMP}) is required.

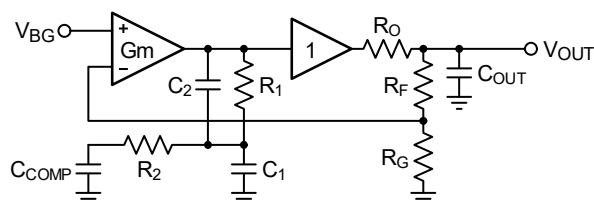


Figure 2. Internal Amplifier Loop

Figure 3 depicts the loop gain and phase responses of the internal amplifier loop. Here, $f_{z(int)}$ is the zero location created by R_1 and C_1 , while $f_{p(int)}$ is the highest pole location due to R_1 and C_2 . Note: The phase of the loop gain is $> -90^\circ$ across the entire amplifier bandwidth. Adding output capacitance C_{OUT} , however, reduces the pole frequency from $f_{p(int)}$ to $f_{p1(ext)}$, which is primarily created by C_{OUT} and R_O , the amplifier output impedance.

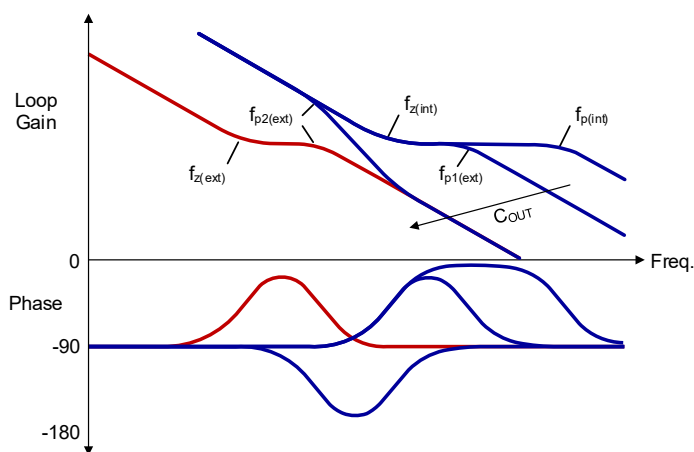


Figure 3. Loop Gain and Phase Responses

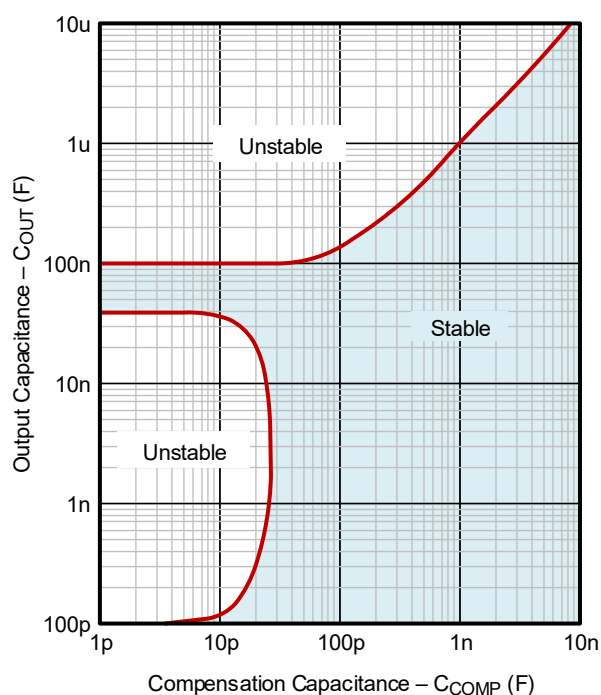


Figure 4. VREF Stability Region

With increasing C_{OUT} , the pole frequency decreases, and phase lag increases up to the point where $f_{p1(ext)} \leq f_{z(int)}$ and the loop phase approaches -180° , causing the loop to be unstable. In this case, the external compensation capacitance, C_{COMP} , must be added that reduces the zero frequency, therefore, restoring phase and loop stability.

As voltage references commonly apply larger output capacitance to drive reference voltage inputs of ADCs with minimum voltage drops, the use of C_{COMP} is almost always necessary. To ensure voltage reference stability across a wide range of C_{OUT} , Figure 4 shows the stability region for various C_{COMP} values.

2. Determining the Internal Component Values

One major contributor to the high accuracy of the output voltage is the factory calibrated resistor ratio of feedback to gain resistance. This ratio sets the gain of the internal non-inverting amplifier: $G = V_{OUT}/V_{BG} = 1 + R_F/R_G$.

While process and temperature variations can cause the absolute resistor values to change by as much as $\pm 20\%$, it is the resistor ratio (combined with a stable V_{BG}) that determines the accuracy of a reference. Evidently, the highest reference accuracy only exists for an unmodified, factory calibrated output.

Altering the reference output voltage from its nominal value is achieved by altering the amplifier gain. This can be accomplished by paralleling an external resistor to either R_F or R_G , which now relies on the device internal, absolute resistor values. Consequently, modifying the reference output voltage through external resistors makes this adjustment method device specific.

To determine the device's internal component values, complete the following the measurement procedure.

▪ Referring to [Figure 5](#):

1. Apply an input voltage to the VIN terminal that is at least 2V higher than the nominal output voltage.
2. Measure $V_{OUT(nom)}$ at the unloaded VOUT terminal.
3. Measure V_{BG} at the TRIM terminal.
4. Calculate the circuit gain with: $G = V_{OUT(nom)}/V_{BG}$

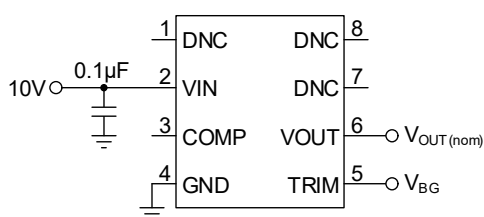


Figure 5. Measuring $V_{OUT(nom)}$ and V_{BG}

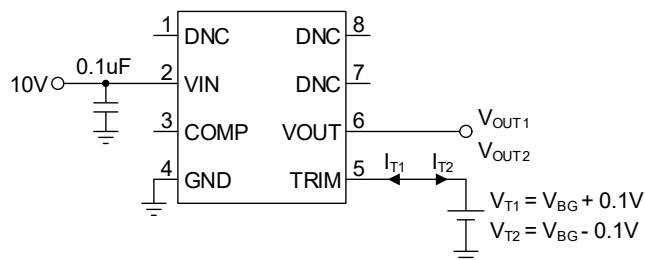


Figure 6. Applying ΔV_T and measuring ΔI_T and ΔV_{OUT}

▪ Referring to [Figure 6](#):

5. Apply the trim voltage $V_{T1} = V_{BG} + 0.1V$ and measure trim current, I_{T1} and output voltage V_{OUT1} .
6. Apply the trim voltage $V_{T2} = V_{BG} - 0.1V$ and measure trim current, I_{T2} and output voltage V_{OUT2} .
Note: This makes $\Delta V_T = 0.2V$.
7. Calculate $\Delta V_{OUT} = V_{OUT1} - V_{OUT2}$ and $\Delta I_T = I_{T1} - I_{T2}$.
8. Calculate the internal trim resistance with: $R_T = \Delta V_T / \Delta I_T$.
9. Next, calculate the feedback resistor with: $R_F = R_T \times \Delta V_{OUT} / \Delta V_T$.
10. Finally, calculate the gain resistor with: $R_G = R_F / (G - 1)$.

When the internal component values have been established, the resistor calculation for altering/adjusting V_{OUT} should commence.

3. Fine Trimming the Output Voltage

The output voltage can be adjusted above and below the factory-calibrated value using the trim terminal. The recommended method is to connect the end terminals of a 100kΩ potentiometer (R_{Pot}) between VOUT and GND and its wiper using a 1MΩ series resistor (R_S) to the TRIM terminal. [Figure 7](#) shows an adjustment example using the 2.5V reference ISL71090SEH25, whose internal component values have been determined using the procedure described in [Determining the Internal Component Values](#).

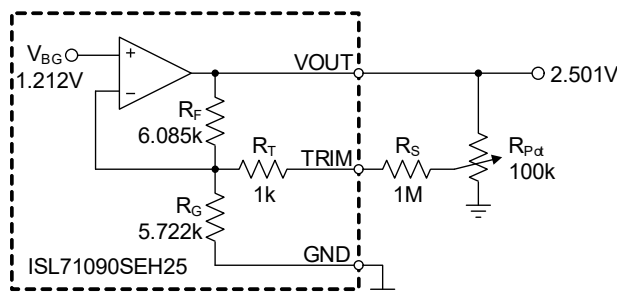


Figure 7. Fine Tuning the Output of a 2.5V Voltage Reference

The highest output voltage is reached when the wiper is turned towards ground, as the total gain resistance is reduced, therefore, increasing circuit gain. The positive adjustment range, $\Delta V_{OUT(+)} = V_{OUT(max)} - V_{OUT(nom)}$, is calculated using [Equation 1](#):

$$(EQ. 1) \quad \Delta V_{OUT(+)} = V_{OUT(nom)} \times \frac{R_F \parallel R_G}{R_S + R_T} = 2.501V \times \frac{2.949}{1001} = +7.37mV$$

Turning the wiper towards VOUT, reduces the circuit gain, which results in the lowest V_{OUT} level. The negative adjustment range, $\Delta V_{OUT(-)} = V_{OUT(min)} - V_{OUT(nom)}$, is calculated using [Equation 2](#):

$$(EQ. 2) \quad \Delta V_{OUT(-)} = V_{OUT(nom)} \times \frac{R_F \parallel R_G - R_F}{R_S + R_T + R_F} = 2.501V \times \frac{-3.136}{1007.1} = -7.79mV$$

When applying this type of fine adjustment, the capacitance at the TRIM terminal must be minimized to preserve amplifier stability. Minimizing this capacitance is accomplished by the following:

- Not connecting a capacitor to the TRIM terminal
- Avoiding GND plane material under the TRIM terminal during PCB layout
- Connecting the series resistor directly to the TRIM terminal, which also minimizes noise injection

Small trim adjustments do not disturb the factory-set temperature coefficient of the reference but trimming near the extreme values or altering V_{OUT} over a wider range does.

4. Altering the Output Voltage

Altering the reference output voltage over a wider range is possible but not recommended as it can increase the overall noise and temperature coefficient of the reference circuit.

Raising the output voltage necessitates an increase in gain, which is accomplished by connecting a pull-down resistor, R_{PD} , between TRIM and GND (Figure 8). This connection reduces the total gain resistance to

$R_G = R_G \parallel R_{PD}$ and raises the output voltage to:

$$(EQ. 3) \quad V_{OUT(High)} = V_{BG} \left(1 + \frac{R_F}{R_G \parallel R_{PD}} \right)$$

Lowering the output voltage requires a gain reduction, achieved by connecting a pull-up resistor, R_{PU} , between TRIM and VOUT (Figure 9). This lowers the output voltage to:

$$(EQ. 4) \quad V_{OUT(Low)} = V_{BG} \left(1 + \frac{R_F \parallel R_{PU}}{R_G} \right)$$

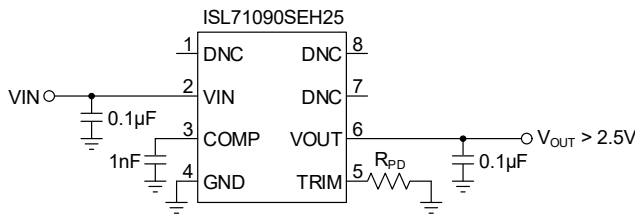


Figure 8. Making $V_{OUT} > V_{OUT(nom)}$

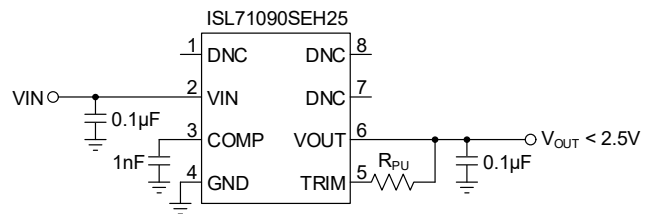


Figure 9. Making $V_{OUT} < V_{OUT(nom)}$

Solving Equation 3 and Equation 4 for R_{PD} and R_{PU} provides the resistor values required to yield the required output voltage.

$$(EQ. 5) \quad R_{PD} = \frac{1}{\frac{(V_{OUT(High)}/V_{BG}) - 1}{R_F} - \frac{1}{R_G}}$$

$$(EQ. 6) \quad R_{PU} = \frac{1}{\frac{1}{R_G[(V_{OUT(Low)}/V_{BG}) - 1]} - \frac{1}{R_F}}$$

Altering the output voltage always increases the circuit's temperature coefficient, which can be calculated using Equation 7.

$$(EQ. 7) \quad T_{CO(TOT)} = T_{CO(VREF)} + \left| (T_{CO(RES)} - T_{CO(VREF)}) \times \frac{V_{OUT(new)} - V_{OUT(nom)}}{V_{OUT(nom)}} \right|$$

Example:

If the output voltage of the ISL71090SEH25 with $T_{CO} = 10\text{ppm}/^\circ\text{C}$, needs adjusting to 2.3V, and the resistor used has a T_{CO} of $100\text{ppm}/^\circ\text{C}$, the total tempco is:

$$T_{CO(TOT)} = 10\text{ppm}/^\circ\text{C} + \left| (100\text{ppm}/^\circ\text{C} - 10\text{ppm}/^\circ\text{C}) \times \frac{2.3\text{V} - 2.5\text{V}}{2.5\text{V}} \right| = 17.2\text{ppm}/^\circ\text{C}$$

5. Conclusion

To preserve stability with large output capacitances, apply the $C_{COMP} - C_{OUT}$ combos listed in [Table 1](#).

Table 1.

Table 1. Recommended Capacitor Pairs

C_{COMP} (nF)	C_{OUT} (μF)
1	0.1
1	1
10	10

To achieve output voltages deviating from the nominal values, always choose a reference whose nominal output is closest to the required value to minimize the overall temperature coefficient.

6. Revision History

Revision	Date	Description
1.01	Jul 20, 2026	Updated Figures 1 and 2.
1.00	Aug 20, 2025	Initial release.

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