

ISL73041SEH, ISL71441M

iSim:PE Model vs Silicon Application Report

Abstract

The [ISL73041SEH](#) (radiation hardened) and [ISL71441M](#) (radiation tolerant) PWM input 12V Half Bridge GaN FET Drivers are designed to drive low $r_{DS(ON)}$ Gallium Nitride FETs (GaN FET) for DC/DC switching regulators. An integrated programmable GaN FET gate drive voltage, high-side bootstrap switch, and strong gate drive current provide a compact and robust GaN FET half-bridge driver.

The iSim:PE model for the ISL73041SEH and ISL71441M was developed to help system designers evaluate the operation of this IC in a simulation environment before or in conjunction with proto-typing a system design. This model simulates typical performance characteristics such as PWM propagation/dead time delay, gate drive rise/fall time, power-up sequencing, and various DC thresholds at room temperature ($T = 25^{\circ}\text{C}$).

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2. Model Revision

3. Schematic File

4. Simulation Schematic

R34AN0007EU0100 Rev.1.00
Oct 23, 2023

5. Silicon vs Simulation Performance Curves

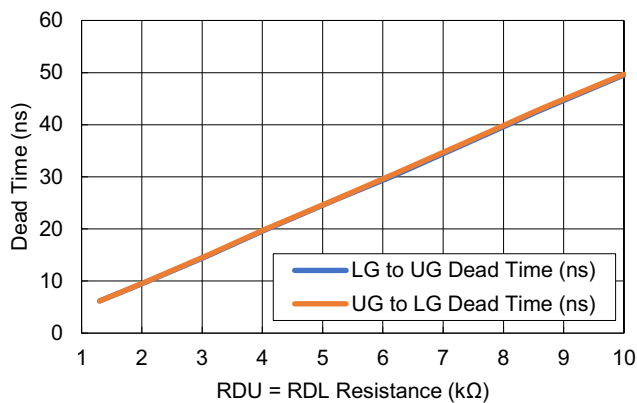


Figure 2. Dead Time vs RDU/RDL Resistor (Silicon)

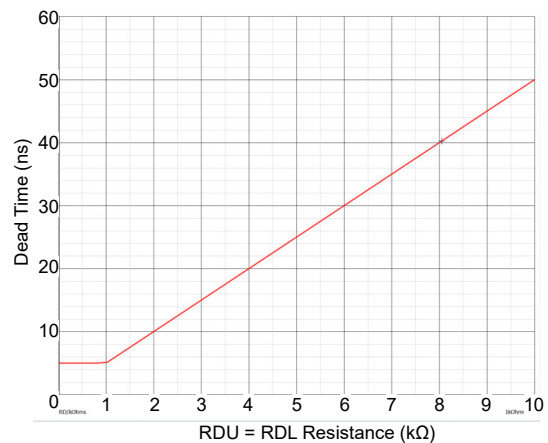


Figure 3. Dead Time vs RDU/RDL Resistor (Simulation)

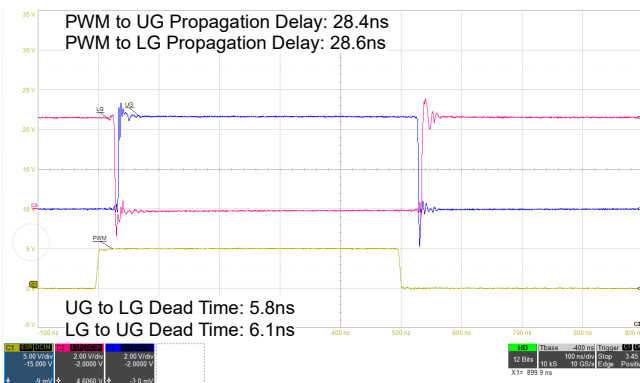


Figure 4. PWM Propagation and Dead Time Delay with RDU = RDL = 1.3kΩ; PHS = PGND; BOOT = PVCC (Silicon)

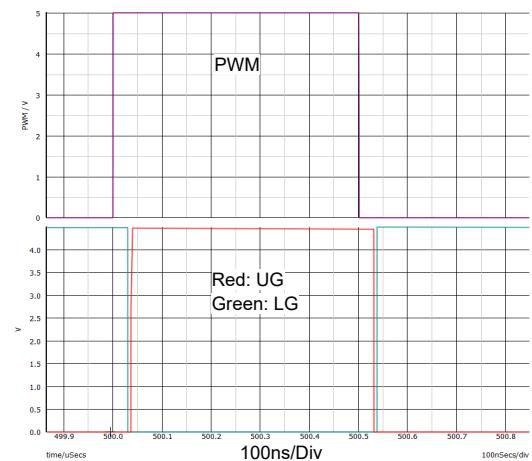


Figure 5. PWM Propagation and Dead Time Delay with RDU = RDL = 1.3kΩ; PHS = PGND; BOOT = PVCC (Simulation)

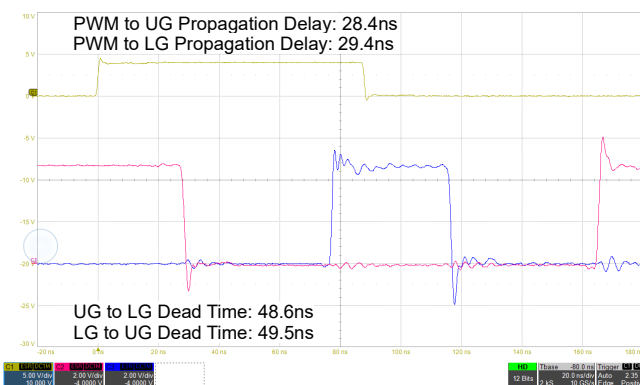


Figure 6. PWM Propagation and Dead Time Delay with RDU = RDL = 10kΩ; PHS = PGND; BOOT = PVCC (Silicon)

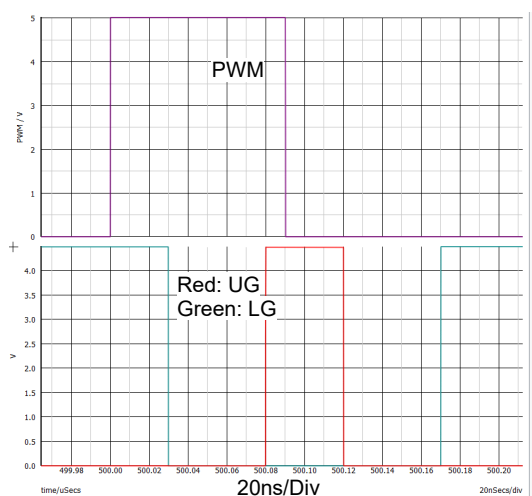


Figure 7. PWM Propagation and Dead Time Delay with RDU = RDL = 10kΩ; PHS = PGND; BOOT = PVCC (Simulation)

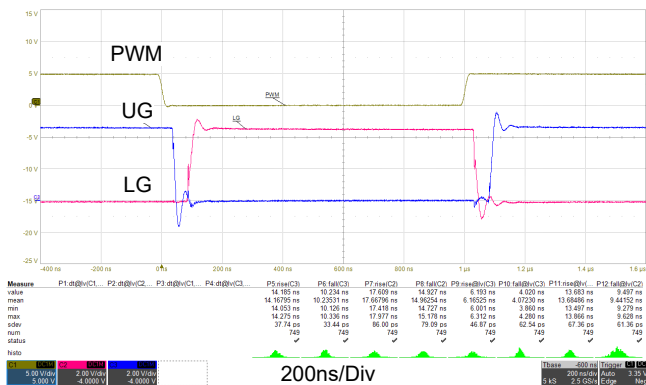


Figure 8. UG/LG Rise and Fall Time with 5.1nF on UG; 10nF on LG; PHS = PGND; BOOT = PVCC (Silicon)

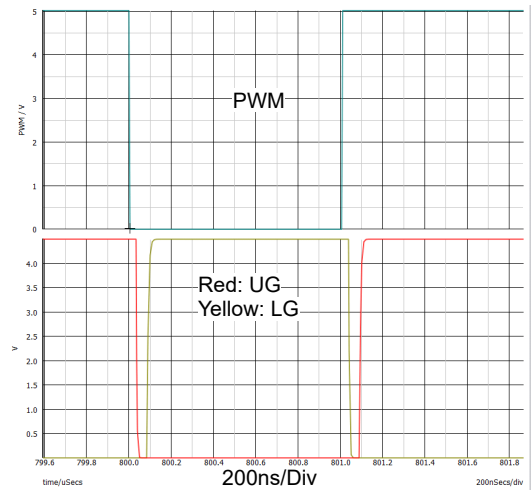


Figure 9. UG/LG Rise and Fall Time with 5.1nF on UG; 10nF on LG; PHS = PGND; BOOT = PVCC (Simulation)

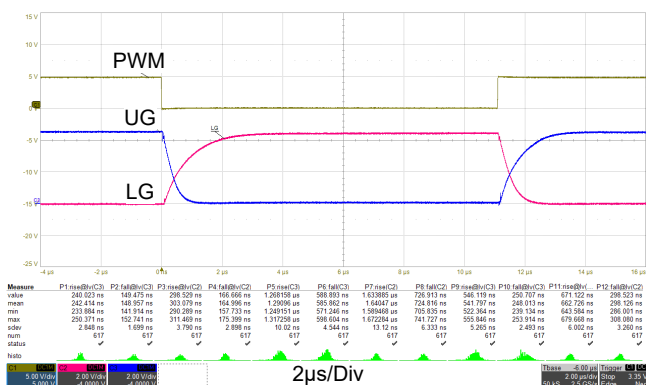


Figure 10. UG/LG Rise and Fall Time with 470nF on UG; 1000nF on LG; PHS = PGND; BOOT = PVCC (Silicon)

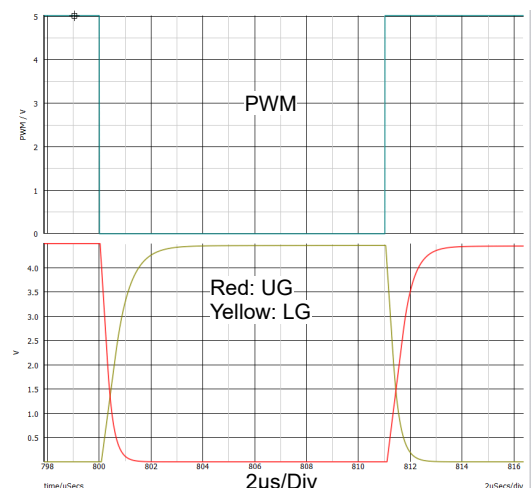


Figure 11. UG/LG Rise and Fall Time with 470nF on UG; 1000nF on LG; PHS = PGND; BOOT = PVCC (Simulation)

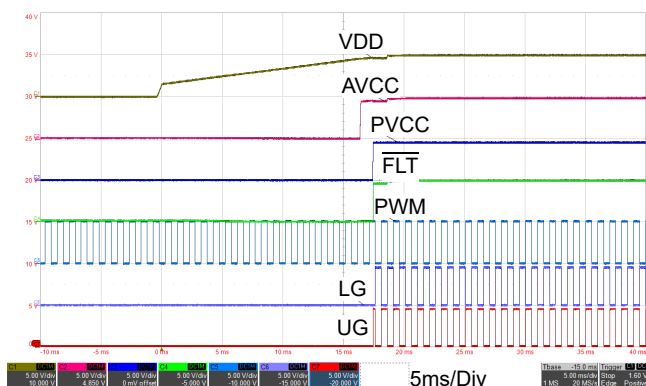


Figure 12. V_{DD} Supply Power-Up Sequence (Silicon)

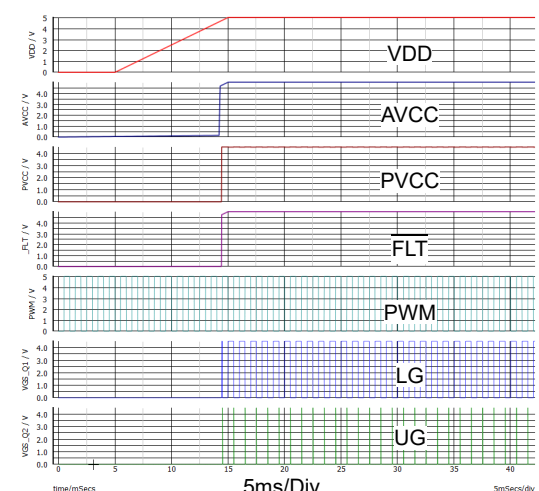


Figure 13. V_{DD} Supply Power-Up Sequence (Simulation)

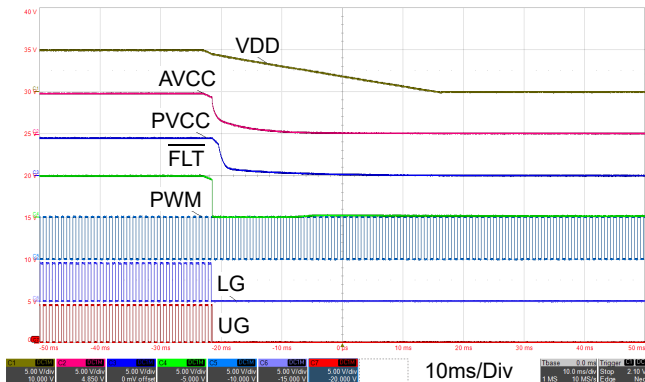


Figure 14. V_{DD} Supply Power-Down Sequence (Silicon)

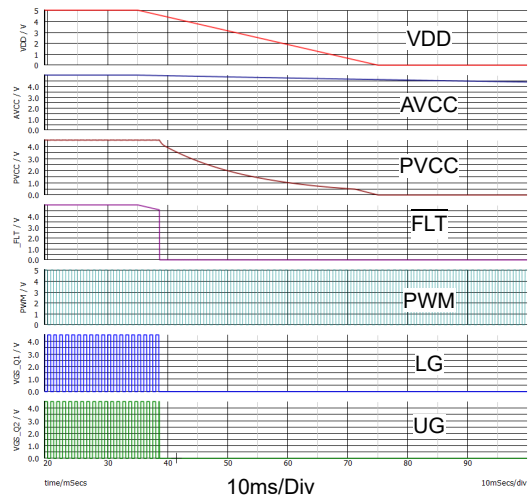


Figure 15. V_{DD} Supply Power-Down Sequence (Simulation)

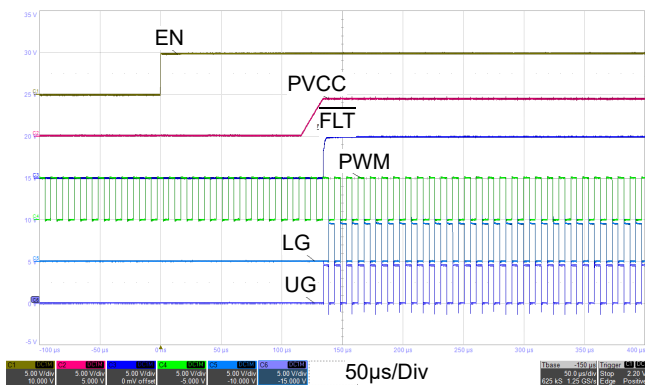


Figure 16. EN Rising Sequence (Silicon)

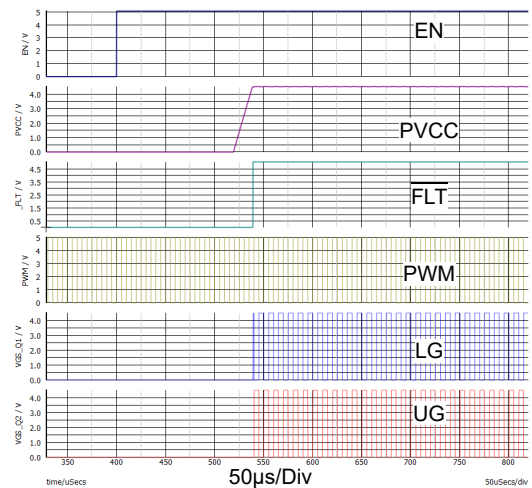


Figure 17. EN Rising Sequence (Simulation)

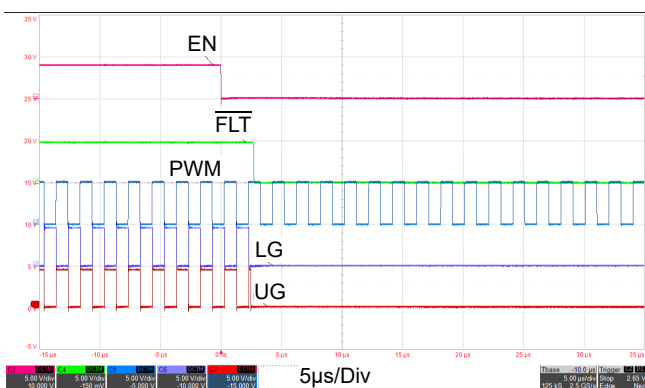


Figure 18. EN Falling Response (Silicon)

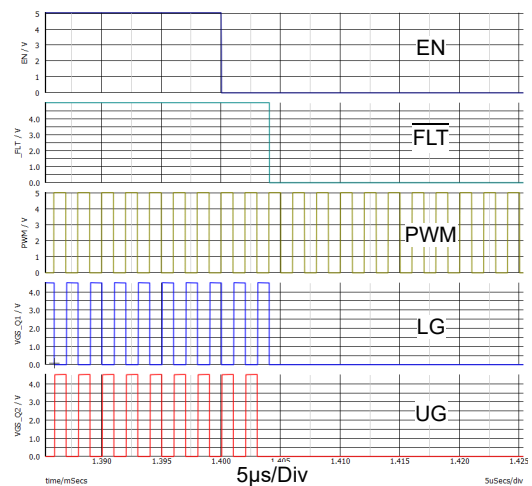


Figure 19. EN Falling Response (Simulation)

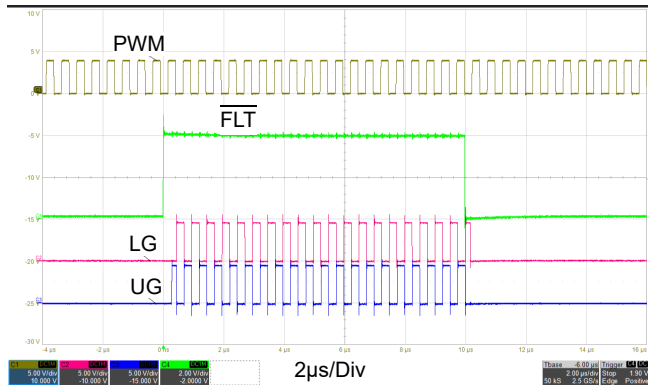


Figure 20. FLT Transient Response (Silicon)

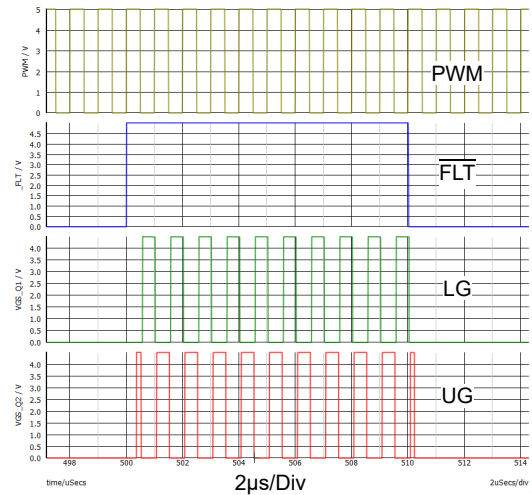


Figure 21. FLT Transient Response (Simulation)

Positive Window Detect Rising Threshold	-	PWM = 0V	-55 to +125°C	160	250	400	mV
Positive Window Detect Falling Threshold	-	PWM = 0V		140	220	380	mV
Negative Window Detect Rising Threshold	-	PWM = 0V		-380	-210	-140	mV
Negative Window Detect Falling Threshold	-	PWM = 0V		-400	-240	-160	mV

Figure 22. PHS Detect Window Voltage (Silicon)

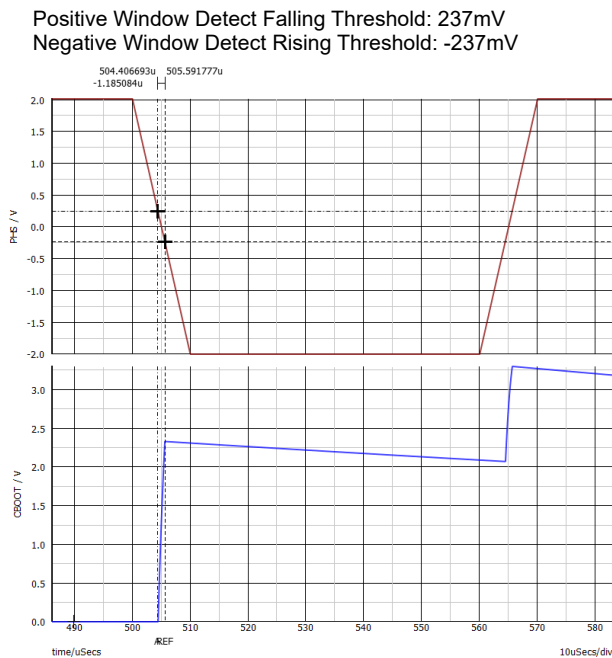


Figure 23. PHS Detect Window Voltage Showing Boot Switch Charging/Discharging BOOT (Simulation)

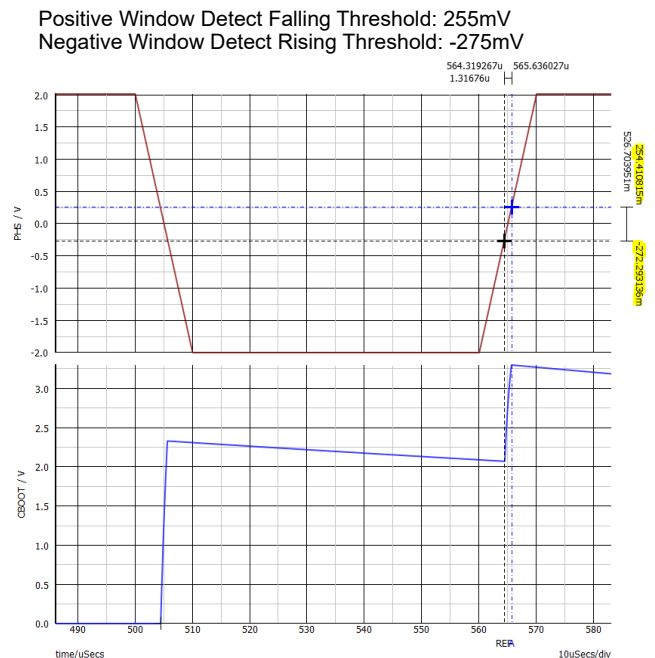


Figure 24. PHS Detect Window Voltage Showing Boot Switch Charging/Discharging BOOT (Simulation)

PWM High Threshold	V_{PWMH}	VDD = 4.75V to 13.2V	-55 to +125°C	-	2.7	2.8	V
PWM Middle Level Range	V_{PWMM}	VDD = 4.75V to 13.2V		1.45	-	2.4	V
PWM Low Threshold	V_{PWML}	VDD = 4.75V to 13.2V		0.95	1.1	-	V
Mid-High Level Hysteresis	-	VDD = 4.75V to 13.2V		-	100	200	mV
Mid-Low Level Hysteresis	-	VDD = 4.75V to 13.2V		-	200	350	mV

Figure 25. PWM Threshold Levels (Silicon)

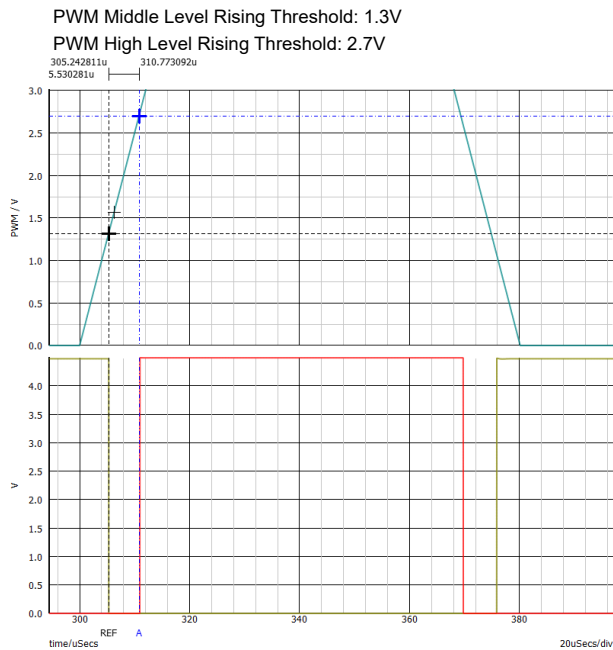


Figure 26. PWM Threshold Levels (Simulation)

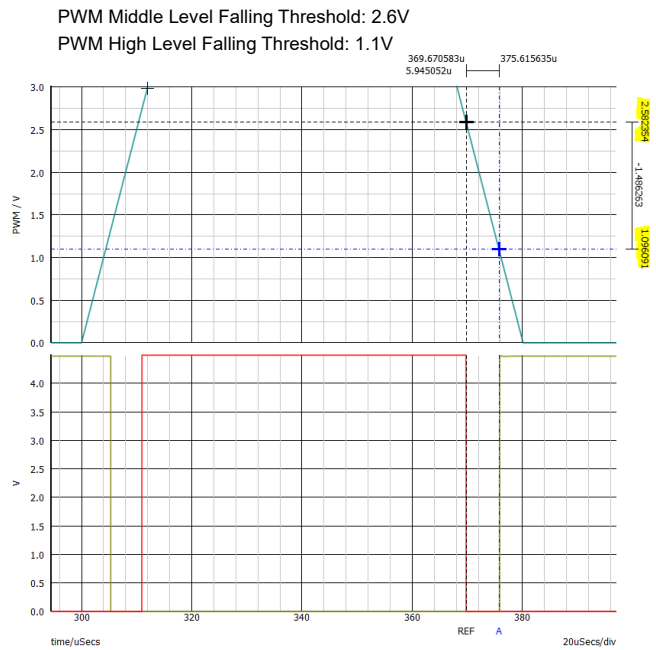
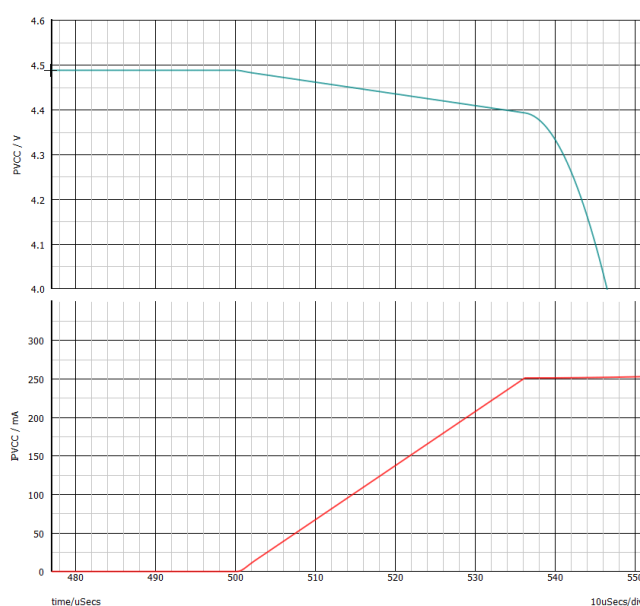
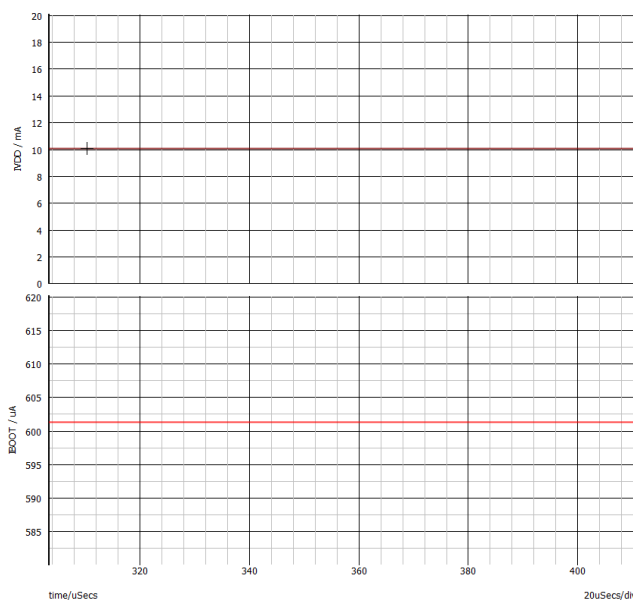


Figure 27. PWM Threshold Levels (Simulation)

PVCC Gate Drive Voltage	PVCC	PVCC = 4.5V = FB or with external resistors; I_{OUT} from 0mA to 150mA; VDD from 4.85V to 13.2V	-55°C	4.39	4.5	4.6	V
			+25°C	4.4	4.5	4.6	
			+125°C	4.39	4.5	4.6	
			+25°C (Post Rad)	4.39	4.5	4.6	
PVCC Output Current Limit	I_{LIMITP}	VDD = 4.75V; FB = PVCC; Force PVCC = 4.2V	-55 to +125°C	190	250	350	mA

Figure 28. PVCC Load Regulation and Constant Current Limit (Silicon)

Figure 29. PVCC Load Regulation and Constant Current Limit (Simulation)

Quiescent Supply Current	I_{DDQ}	PWM = Float; RDU = RDL = 1.3k Ω	-55 to +125°C	-	9	-	mA
BOOT Quiescent Current	I_{Q_Boot}	PWM = Float; BOOT-PHS = 4.5V	-55 to +125°C	-	580	650	μ A

Figure 30. V_{DD} and BOOT Quiescent Current with RDU = RDL = 1.3k Ω (Silicon)Figure 31. V_{DD} and BOOT Quiescent Current with RDU = RDL = 1.3k Ω (Simulation)

6. Revision History

Revision	Date	Description
1.00	Oct 23, 2023	Initial release.

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