RZ/T2H, RZ/N2H

Mitigation software for DDR Memory Controller issue

Introduction

This document provides guidance on implementing mitigation software that reduces the likelihood of a "DDR Memory Controller issue" reported in a Renesas Technical Update.

Technical Update URL:

https://www.renesas.com/ja/document/tcu/ddr-memory-controller-issue?language=en&r=25567515

Target Device

RZ/T series: RZ/T2H

RZ/N series: RZ/N2H

Product	Part Number	Package	Cortex-A55	Cortex-R52	Security
RZ/T2H	R9A09G077M48GBG#AC0 R9A09G077M48GBG#BC0	729-pin FCBGA	Quad cores	Two CPUs	Available
	R9A09G077M28GBG#AC0 R9A09G077M28GBG#BC0	729-pin FCBGA	Dual cores	Two CPUs	Available
	R9A09G077M08GBG#AC0 R9A09G077M08GBG#BC0	729-pin FCBGA	Single core	Two CPUs	Available
	R9A09G077M44GBG#AC0 R9A09G077M44GBG#BC0	729-pin FCBGA	Quad cores	Two CPUs	Not Available
	R9A09G077M24GBG#AC0 R9A09G077M24GBG#BC0	729-pin FCBGA	Dual cores	Two CPUs	Not Available
	R9A09G077M04GBG#AC0 R9A09G077M04GBG#BC0	729-pin FCBGA	Single core	Two CPUs	Not Available
RZ/N2H	R9A09G087M48GBG#AC0 R9A09G087M48GBG#BC0	576-pin FCBGA	Quad cores	Two CPUs	Available
	R9A09G087M28GBG#AC0 R9A09G087M28GBG#BC0	576-pin FCBGA	Dual cores	Two CPUs	Available
	R9A09G087M08GBG#AC0 R9A09G087M08GBG#BC0	576-pin FCBGA	Single core	Two CPUs	Available
	R9A09G087M44GBG#AC0 R9A09G087M44GBG#BC0	576-pin FCBGA	Quad cores	Two CPUs	Not Available
	R9A09G087M24GBG#AC0 R9A09G087M24GBG#BC0	576-pin FCBGA	Dual cores	Two CPUs	Not Available
	R9A09G087M04GBG#AC0 R9A09G087M04GBG#BC0	576-pin FCBGA	Single core	Two CPUs	Not Available

Contents

1. Introduction

1.1 Overview

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Supplementary information

- Please apply either of the following mitigation software for FSP and Linux.
  for FSP : r01an7850ej0100-rzt2h-rzn2h-Mitigation-for-DDR-MEMC-Controller.pdf (This file)
  (DDR_MemoryController_issue_FSP_Mitigation.zip)
  for Linux : 0002-Mitigation-for-DDR-MEMC-Controller.patch
  (DDR_MemoryController_issue_Linux_Mitigation.zip)
- No need to apply this software to the revised product.

1.2 Target Modules

The target modules that require function implementation are listed below.

Table 1.1 Target modules list

Modules	Details
LPDDR4 SDRAM Subsystem (DDRSS)	If DDRSS is used, refer to Section “2. Mitigation Function Implementation” to implement the mitigation function.

2. Mitigation Function Implementation

This section explains how to implement the mitigation function.

1. To implement the mitigation function, add the following Miti_for_DDR_Memory_Controller_issue( ) to hal_entry.c.
   (The following source code is identical to lines 55 through 140 of the attached “reference_code.c”.)

```
void Miti_for_DDR_Memory_Controller_issue()
{
    R_BSP_RegisterProtectDisable(BSP_REG_PROTECT_LPC_RESET);
    R_BSP_MODULE_START(FSP_IP_USBHS, 0);
    R_BSP_MODULE_START(FSP_IP_LCDC, 0);
    R_BSP_RegisterProtectEnable(BSP_REG_PROTECT_LPC_RESET);

    R_BSP_RegisterProtectDisable(BSP_REG_PROTECT_SYSTEM);
    R_MPU3->RGN[0].STADD  = 0x10000000;
    R_MPU6->RGN[0].STADD  = 0x00000000;
    R_MPU10->RGN[0].STADD = 0x00000000;
    R_BSP_RegisterProtectEnable(BSP_REG_PROTECT_SYSTEM);

    R_USBF->CHa[0].CHCFG   = 0x00066008;
    R_USBF->CHa[0].CHITVL  = 0x00000000;

    R_USBF->CHa[0].N[0].SA = 0xc0000000;
    R_USBF->CHa[0].N[0].TB = 0x00000040;
    R_USBF->CHa[0].CHCTRL  = 0x00000008;
    R_USBF->CHa[0].CHCTRL  = 0x00000005;

    while( R_USBF->CHa[0].CHSTAT_b.EN == 1);

    R_USBF->CHa[0].N[0].SA = 0xc0000040;
    R_USBF->CHa[0].N[0].TB = 0x00000040;
    R_USBF->CHa[0].CHCTRL  = 0x00000008;
    R_USBF->CHa[0].CHCTRL  = 0x00000005;

    while( R_USBF->CHa[0].CHSTAT_b.EN == 1 );

    R_LCDC->VI6_CMD0               = 0x00000000;
    R_LCDC->VI6_SRESET             = 0x00000001;
    R_LCDC->VI6_WPF0_IRQ_ENB       = 0x00011003;
    R_LCDC->VI6_DISP0_IRQ_ENB      = 0x00000120;
    R_LCDC->VI6_RPF0_SRC_BSIZE     = 0x00800004;
    R_LCDC->VI6_RPF0_SRC_ESIZE     = 0x00800004;
    R_LCDC->VI6_RPF0_INFMT         = 0x00000018;
    R_LCDC->VI6_RPF0_DSWAP         = 0x00000000;

    R_LCDC->VI6_RPF0_LOC           = 0x00000000;
    R_LCDC->VI6_RPF0_SRCM_PSTRIDE  = 0x01800000;
    R_LCDC->VI6_RPF0_SRCM_ADDR_Y   = 0xc0001000;
```

(This function continues on the next page.)

```
    R_LCDC->VI6_WPF0_SRCRPF        = 0x00000002;
    R_LCDC->VI6_WPF0_OUTFMT        = 0x00000018;
    R_LCDC->VI6_WPF0_DSTM_STRIDE_Y = 0x00000180;
    R_LCDC->VI6_DPR_RPF0_ROUTE     = 0x00000038;
    R_LCDC->VI6_DPR_RPF1_ROUTE     = 0x0000003F;
    R_LCDC->VI6_DPR_WPF0_FPORCH    = 0x00000500;
    R_LCDC->VI6_DPR_BRS_ROUTE      = 0x1000003F;

    R_LCDC->VI6_LIF0_CTRL          = 0x01000003;
    R_LCDC->VI6_LIF0_CSBTH         = 0x000005DC;
    R_LCDC->VI6_LIF0_LBA           = 0x86000000;

    for( uint32_t i=0; i<100; i++ )
    {
        __NOP();
    }

    R_LCDC->VI6_CMD0 = 0x000000001;
    while( R_LCDC->VI6_DISP0_IRQ_STA_b.MAE == 0 );

    R_LCDC->VI6_SRESET = 0x1;

    uint32_t chcfg = (1    << 22)
                   | (2    << 16)
                   | (2    << 12)
                   | (2    <<  4)
                   | (0 <<  0);

    R_DMAC0->GRP[0].CH[0].N[0].SA = 0xc0001000;
    R_DMAC0->GRP[0].CH[0].N[0].DA = 0xc0002000;
    R_DMAC0->GRP[0].CH[0].N[0].TB = 0x10;
    R_DMAC0->GRP[0].CH[0].CHCFG   = chcfg;
    R_DMAC0->GRP[0].CH[0].CHCTRL  = 0x00000008;

    R_DMAC0->GRP[0].CH[0].CHCTRL  = 0x00000005;

    while( R_DMAC0->GRP[0].CH[0].CHSTAT_b.TC == 0 );

    __DSB();
    volatile uint32_t rdata = *(uint32_t *)0xc0002004;
    FSP_PARAMETER_NOT_USED(rdata);
}
```

2. Add the `Miti_for_DDR_Memory_Controller_issue()` function after initializing the DDR settings in `bsp_ddr_init()`.
   Typically, `bsp_ddr_init()` is called within the `R_BSP_WarmStart()` function.

   (The following source code is identical to lines 22 through 50 of the attached “reference_code.c”.)

```
void R_BSP_WarmStart (bsp_warm_start_event_t event)
{
    if (BSP_WARM_START_RESET == event)
    {
        /* Pre clock initialization */
    }

    if (BSP_WARM_START_POST_C == event)
    {
        /* C runtime environment and system clocks are setup. */

#if BSP_FEATURE_DDR_SUPPORTED
 #if (1 == BSP_CFG_DDR_INIT_ENABLE)

        /* Initialize the DDR settings. */
        bsp_ddr_init();

        /*  Mitigation for DDR Memory Controller issue  */
        Miti_for_DDR_Memory_Controller_issue(); // Add
 #endif
#endif

        if (NULL != g_bsp_pin_cfg.p_extend)
        {
            /* Configure pins. */
            R_IOPORT_Open(&g_ioport_ctrl, &g_bsp_pin_cfg);
        }
    }
```

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	June 13, 2025	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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