Networking Timing Card Synchronization Clock Tree for ClockMatrix™ Devices

Introduction

This application note outlines the design and implementation of a high-performance synchronization clock tree for 5G-Advance networking equipment using Renesas ClockMatrix. These timing solutions are critical in ensuring accurate phase and frequency synchronization in Radio Access Networks (RANs). This document highlights clock tree design requirements, the role of ClockMatrix in enabling frequency synthesis, jitter filtering, and phase alignment, and offers guidance for achieving standards-compliant synchronization in transport and O-RAN deployments.

Contents

Figures

Tables

1. Overview

Accurate timing and synchronization are critical for modern telecommunications networks, particularly for 5G Radio Access Network (RAN). For networking elements (NE), synchronous clocks provide a stable and traceable timing reference for these systems, ensuring phase and frequency synchronization across the network. The core of this synchronization architecture is a well-designed clock tree within the NE, which distributes precise clock signals within the system and to the downstream NEs.

ClockMatrix, a highly-integrated timing solution, supports functions such as frequency synthesis, jitter filtering, and dynamic reconfiguration, making it an ideal choice for use in transport equipment and O-RAN environments. This document explains the design considerations, ClockMatrix features, and implementation strategies for synchronization clock trees.

2. The Clock Tree in Synchronous Equipment

The clock tree is the backbone of synchronization, ensuring that all system components operate with precise and stable timing along with the distribution of the reference timing signals throughout the packet network. A well-designed clock tree enables synchronization with external timing sources and provides jitter-free clock distribution to various subsystems.

2.1 Key Functional Blocks of the Synchronization Clock Tree

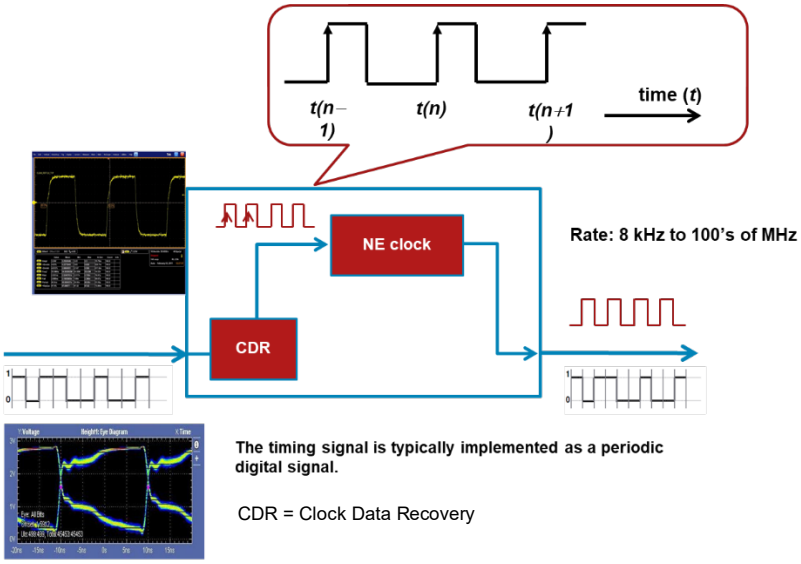

Figure 1. Example Clock Tree for Physical-Layer Synchronization (SyncE)

A robust synchronization clock tree comprises the following core components:

1. **Reference Clock Input**:
   a. Receives timing signals from external references such as Global Navigation Satellite Systems (GNSS), PTP Grandmasters, or Primary Reference Clocks (PRC).
   b. These signals may be distributed as either physical-layer or packet-layer timing references across multiple NEs.
2. **Clock Generation**:
   a. Converts reference signals into the various frequencies required by internal components.
   b. Incorporates wander filtering, jitter filtering, phase alignment, and holdover capabilities to meet applicable ITU-T Recommendations such as G.8262.1 (enhanced SyncE) and G.8273.2 (T-BC/T-TSC Class C/D).

3. **Clock Distribution**:
   a. Delivers synchronized clocks to subsystems such as Ethernet PHYs, radio interfaces, and timing protocols like IEEE 1588.
   b. Supports independent synchronization domains while maintaining phase coherence and traceability.
4. **Monitoring and Calibration**:
   a. Continuously verify timing and clock accuracy.
   b. Adjust for phase deviations using real-time feedback mechanisms and ultra-high precision phase measurement.

2.2 Synchronization Clock Tree Requirements

To support 5G-Advance and O-RAN synchronization, the clock tree must meet stringent performance criteria:

- **Low Jitter**: Ensures minimal phase noise for precise synchronization and use as a reference clock for SERDES and other components.
- **Wide Frequency Range**: Supports multiple output frequencies (for example, 10MHz, 125MHz, 156.25MHz).
- **High Stability**: Maintains traceability to primary reference clocks (for example, PRC, PRTC), including holdover and clock transient mitigation.
- **Redundancy**: Supports failover mechanisms to handle timing source disruptions and network rearrangements.
- **Scalability**: Accommodates additional clock outputs without degrading performance.

3. The Role of ClockMatrix in Clock Tree Design

ClockMatrix is a critical component in Networking Timing Cards, providing essential functions such as frequency synthesis, jitter filtering, and dynamic reconfiguration. It ensures that SEC synchronization meets industry standards.

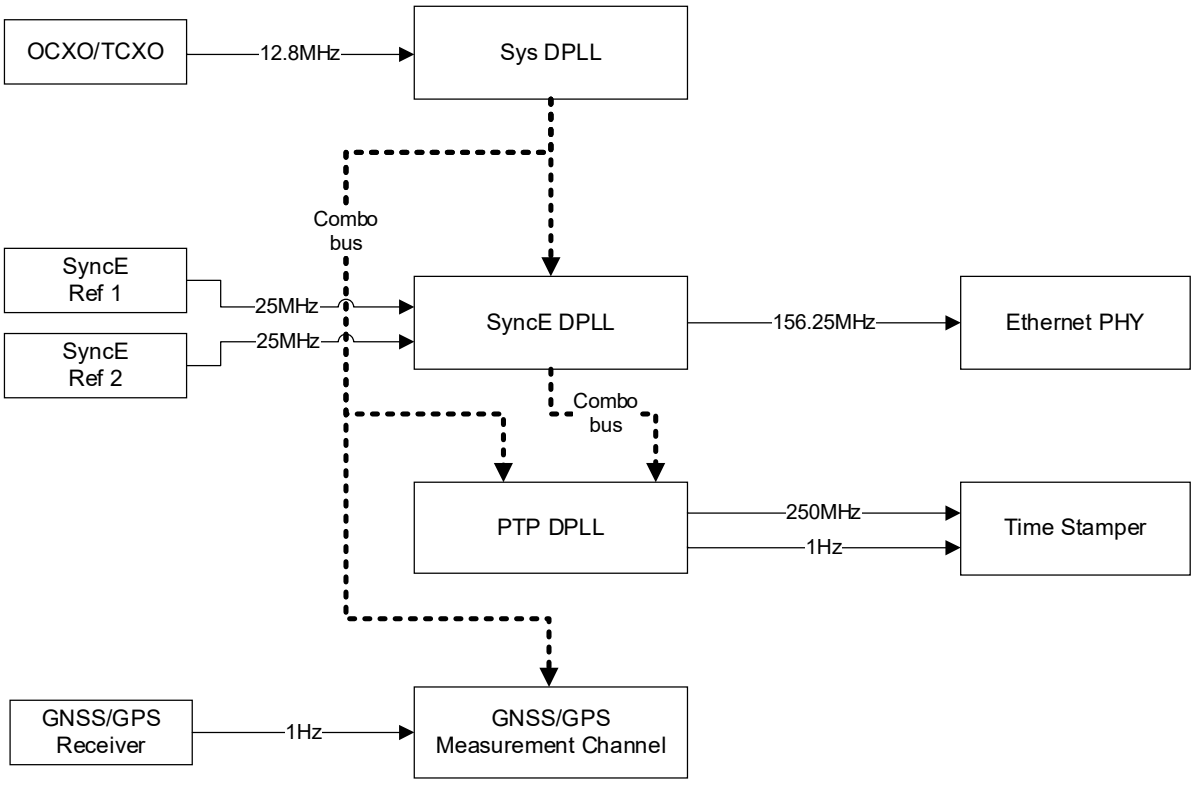

Figure 2. ClockMatrix Simplified Block Diagram

3.1 Core Functions of ClockMatrix

ClockMatrix provides the critical functionality needed to implement a flexible and high-performance clock tree:

- **Frequency Synthesis**: Generates precise output frequencies using fractional-N PLLs.
- **Multi-Channel DPLLs**: Supports multiple independently synchronized domains, with clock combining when needed.
- **Jitter Filtering**: Suppresses high-frequency noise to deliver clean clock signals.
- **Phase Alignment**: Maintains channel-independent phase coherence between timing source and outputs.
- **Dynamic Reconfiguration**: Enables real-time reference switching and hitless transitions to adapt to changing network conditions.
- **High-Resolution Measurement**: Supports picosecond-level timing accuracy for clock monitoring.

3.2 ClockMatrix Advantages for Synchronization

- **Low Jitter**: Meets demanding reference clock requirements for 112G SERDES and similar ASICs.
- **Compact Integration**: Combines multiple PLLs and timing functions into a small footprint.
- **Flexible Output Configuration**: Supports a wide range of input and output frequencies.
- **ITU-T Equipment Clock Compliance**: Meets all ITU-T recommendations, such as: G.8262 (EEC opt1 and opt2, G.8262.1 (eEEC), G.8263 (PEC-S-F), G.8273.2 (T-BC/T-TSC), G.8273.3 (T-TC), G.8273.4 (T-BC-A/P, T-TSC-A/P).
- **Disaggregated Protocol Support**: Servos and filters are protocol-agnostic, allowing for integration with open-source PTP (for example, ptp4l) or ESMC (for example, synced) implementations.

Satellite and network-based synchronization options:

- GNSS on-site
- GNSS on-site and network fallback
- Network-based

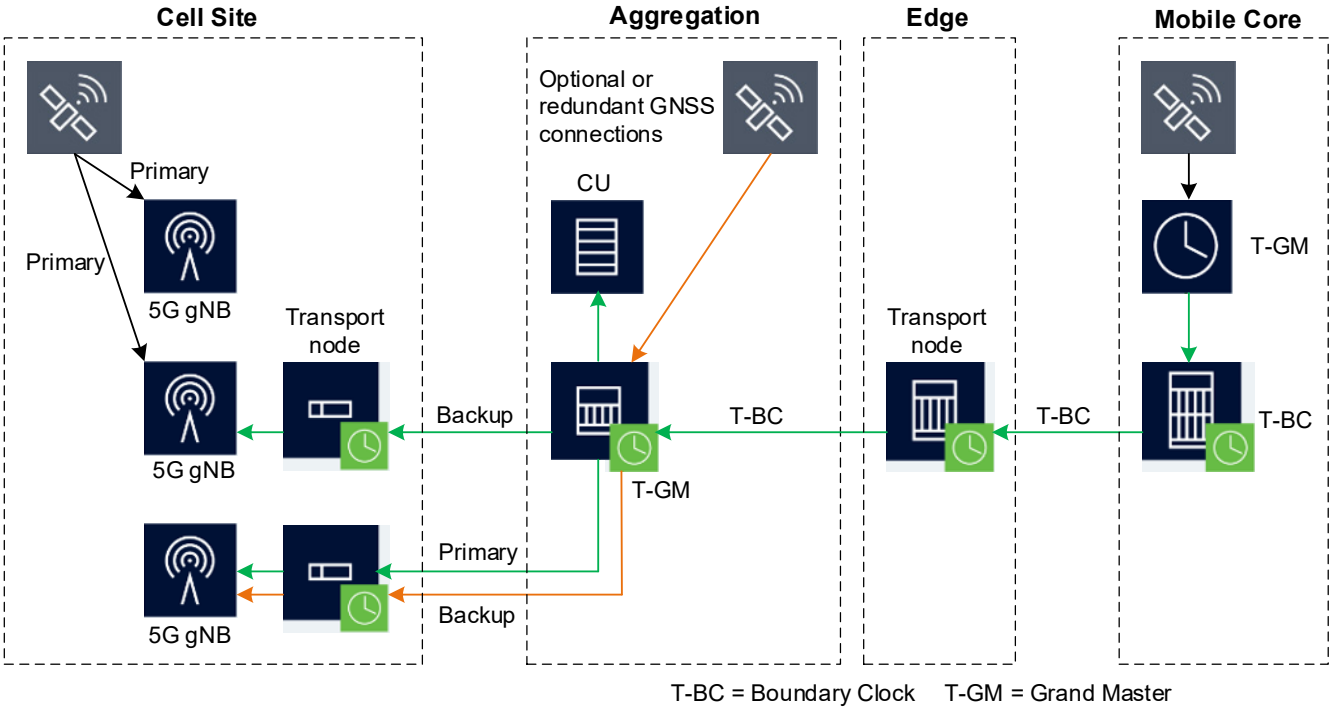

Figure 3. 5G Transport Synchronization

4. Impact of Software Filters on the Clock Tree

In existing packet-switched networks that lack built-in synchronization support, software-based adaptive filters are essential to compensate for packet delay variation in timing packets. These algorithms enhance synchronization performance, achieving time/phase accuracy under 1 microsecond and frequency accuracy within 16 parts per billion (ppb).

Even in networks with full IEEE 1588 support – comprising Boundary Clock (BC) or Transparent Clock (TC) nodes – software-based outlier detection algorithms can further improve synchronization, enabling filtered time/phase accuracy below 5 nanoseconds in compliance with provisional ITU-T G.8273.2 Class D recommendations.

So what is the impact to the clock tree? The use of software-based servos does not impact the hardware-level synchronization clock tree. This is because the adaptive servo controls the Digital Phase-Locked Loop (DPLL) indirectly via the Linux PTP Hardware Clock (PHC) subsystem. The PHC interface abstracts hardware-level clock adjustments for time, phase, and frequency, allowing seamless integration between software algorithms and hardware performance.

Renesas provides a Linux-compatible software solution called the *PTP Clock Manager for Linux (pcm4l)*. This high-performance synchronization engine enables time, phase, and frequency recovery from packet-based timing sources. It includes key features to support ITU-T G.8273.4 telecom time synchronous clocks for use with partial timing support from the network, including a full packet-clock state machine and control architecture. For more information, see the PTP Clock Manager for Linux (pcml4) page.

5. Clock Tree Design Using ClockMatrix

To implement a reliable synchronization clock tree, consider the following design steps:

1. Define System Requirements:
   a. Identify characteristics of input references (for example, frequency, jitter, stability).
   b. Determine required output frequencies (for example, 10MHz, 125MHz, 156.25MHz).
   c. Establish phase noise and jitter performance targets.
   d. Design redundancy mechanisms for resilience.
2. Design the Clock Distribution Network:
   a. When needed, use low-skew fan-out buffers. Consider use of ClockMatrix's external feedback capability for implementation of Zero-Delay Buffer (ZDB).
   b. Optimize trace lengths and control impedance on the PCB. Consider use of ClockMatrix's round trip delay measurements control for backplane delays, PLL input/output delays.
   c. Include proper termination to preserve signal integrity.
3. Implement Monitoring and Feedback:
   a. Use high precision phase detectors and feedback loops to maintain lock.
   b. Support fast re-lock and drift compensation.
4. Validate and Optimize:
   a. Use of Evaluation Boards to evaluate jitter, phase noise, and PLL behavior under various scenarios.
   b. Perform hardware validation against ITU-T and IEEE standards.
   c. Optimize for low power and thermal efficiency.

Renesas offers world-class applications support to help with your clock tree solutions, including applicable notes guiding ClockMatrix configurations to meet applicable ITU-T recommendations.

5.1 Clocking for Broadcom Switch ASIC

Figure 4 depicts a 5G transport solution architecture based on a Broadcom switch SoC.

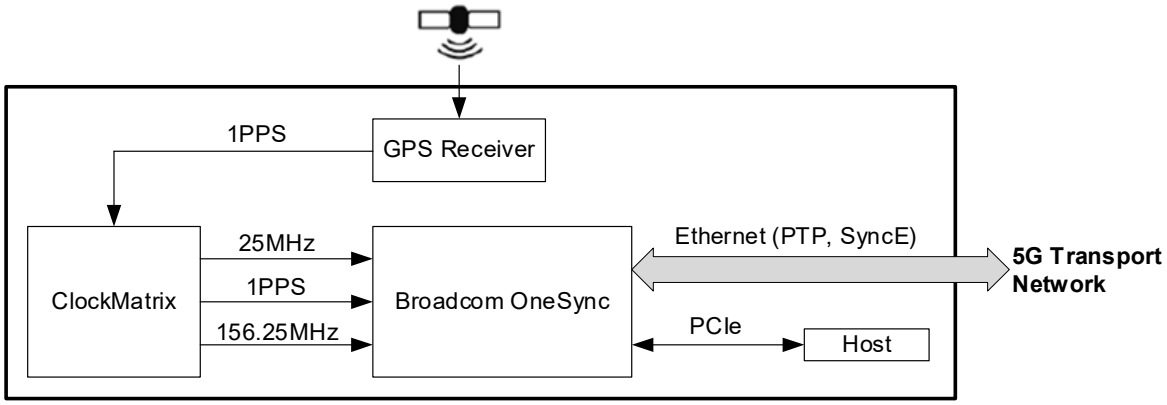

Figure 4. Clocking for Broadcom Ethernet Switch ASICs

The clock connections between ClockMatrix and Broadcom BCM88280 is provided in Table 1. Optionally, connection to a GNSS receiver may be integrated with ClockMatrix locked to a recovered 1PPS signal.

Table 1. Example Clock Connections for Qumran (BCM88280)

Direction	Pin	Frequency	Use	Notes
To BCOM	TS_PLL_REFCLK	25MHz	PTP Clock	From PTP channel on ClockMatrix.
To BCOM	BS_PLL0_FREF	25MHz	PTP Clock	From PTP channel on ClockMatrix.
To BCOM	BS_PLL1_FREF	25MHz	PTP Clock	From PTP channel on ClockMatrix.
To BCOM	TS_GPIO3	1Hz	PTP PPS	From PTP channel on ClockMatrix.
To BCOM	{BH,NIF}_PLL_REFCLK	156.25MHz	SyncE Clock	Filtered SyncE clock from DPLL.
From BCOM	L1_RCVRD_CLK	25MHz	SyncE Clock	Recovered SyncE clock to DPL, this may be rate dependent.
From BCOM	L1_RCVRD_CLK_BKUP	25MHz	SyncE Clock	Recovered SyncE clock to DPL, this may be rate dependent.
To BCOM	CORE_PLL_FREF	50MHz	System Clock	Free-run clock not locked to PTP or SyncE domains. Optional to source from ClockMatrix device.

Note: These clocks were part of the system tested by Renesas. Other BCOM devices may support different pins and clock frequencies. For instance, other GPIOs may be used for the 1Hz input.

6. Conclusion

A high-quality Networking Timing Card, built around ClockMatrix, is essential for maintaining precise synchronization in modern transport and O-RAN deployments. By delivering low-jitter, phase-aligned clock signals across multiple domains, ClockMatrix helps designers meet stringent 5G-Advance requirements and ITU-T standards.

With its combination of advanced features, robust configurability, and standards compliance, ClockMatrix enables engineers to build scalable, reliable clock trees that ensure long-term timing accuracy for next-generation networks.

7. Revision History

Revision	Date	Description
1.00	Apr 18, 2025	Initial release.

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