

RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, RZ/G3S, RZ/A3M, and RZ/G3E PCB Design Checklist

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Introduction


This document summarizes hardware design knowledge required to design PCBs with target devices, along with design examples and a design checklist. It also describes the restrictions and recommendations described in its hardware manuals, as well as includes some hints to reduce troubles in hardware development.

Target Device

- RZ/G2L
- RZ/G2LC
- RZ/V2L
- RZ/G2UL
- RZ/Five
- RZ/A3UL
- RZ/G3S
- RZ/A3M
- RZ/G3E

NOTE

The design of evaluation board kits might not meet items in the checklist due to internal evaluation and realizing multiplexed functions, however, we strongly recommend to design along with the checklist.

In figures in this document,  marks indicate prohibited items, and  marks indicate items to notice.

Please also refer to the following documents.

- User's Manual: Hardware
- Design Data of EV Kit
- Other Application Notes for Hardware Design

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1. Reset

1.1 Circuits for PRST# Input



Points

ALL

- Check the IO voltage of the PRST#.

The PRST# is a reset input with Schmitt trigger, and it is on the 1.8V power domain only for RZ/G3S and the 3.3V power domain for others.

- Do not set PRST# high when the MPU is powered off.

High level input for the PRST# is not supported while the power supply is turned off.

- Make sure that the connection to TRST# is OK.

The TRST# signal from a JTAG ICE should be considered in terms of its connection to the PRST# signal, and the voltages of each signal should be confirmed.

- Make sure the PRST# signal is pulled up.
- We recommend that the pull-up resistor is no greater than 10k Ω

The IO on the PRST# pin is Schmitt-triggered and does not have an internal pull-up; a signal generated by an open drain source must be input to PRST#.

- Also check the reset signals of peripheral devices.

Some peripheral devices may require a reset at the same time as the MPU reset. In such cases, make sure that there is no problem with the voltage of the reset signal of the peripheral device. Also, if an open drain is used to generate the PRST# signal, make sure that the waveform of the PRST# signal is stable.

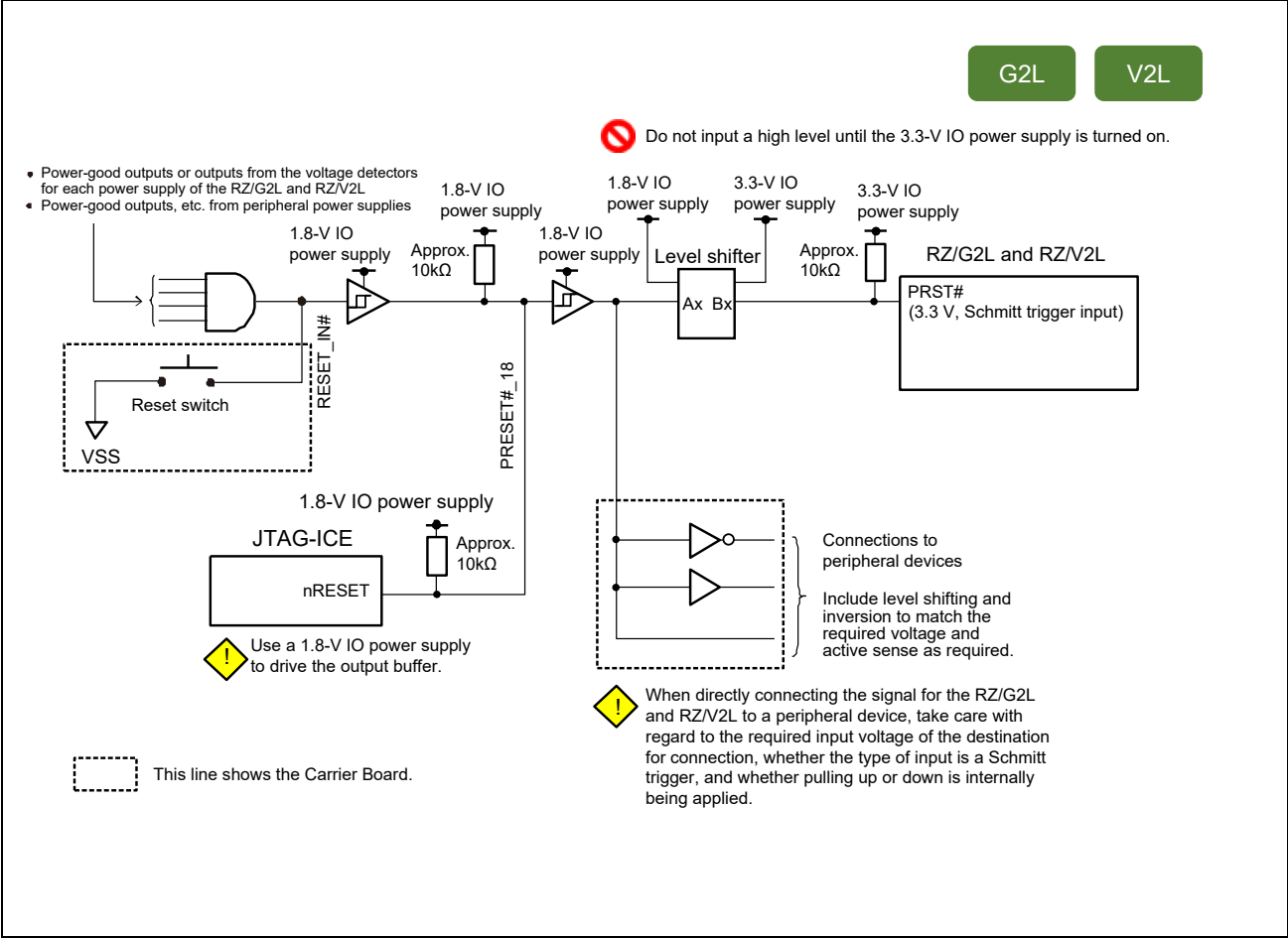


Figure 1.1(a) Example of the Configuration of PRST# for RZ/G2L and RZ/V2L EVKIT Discrete Edition

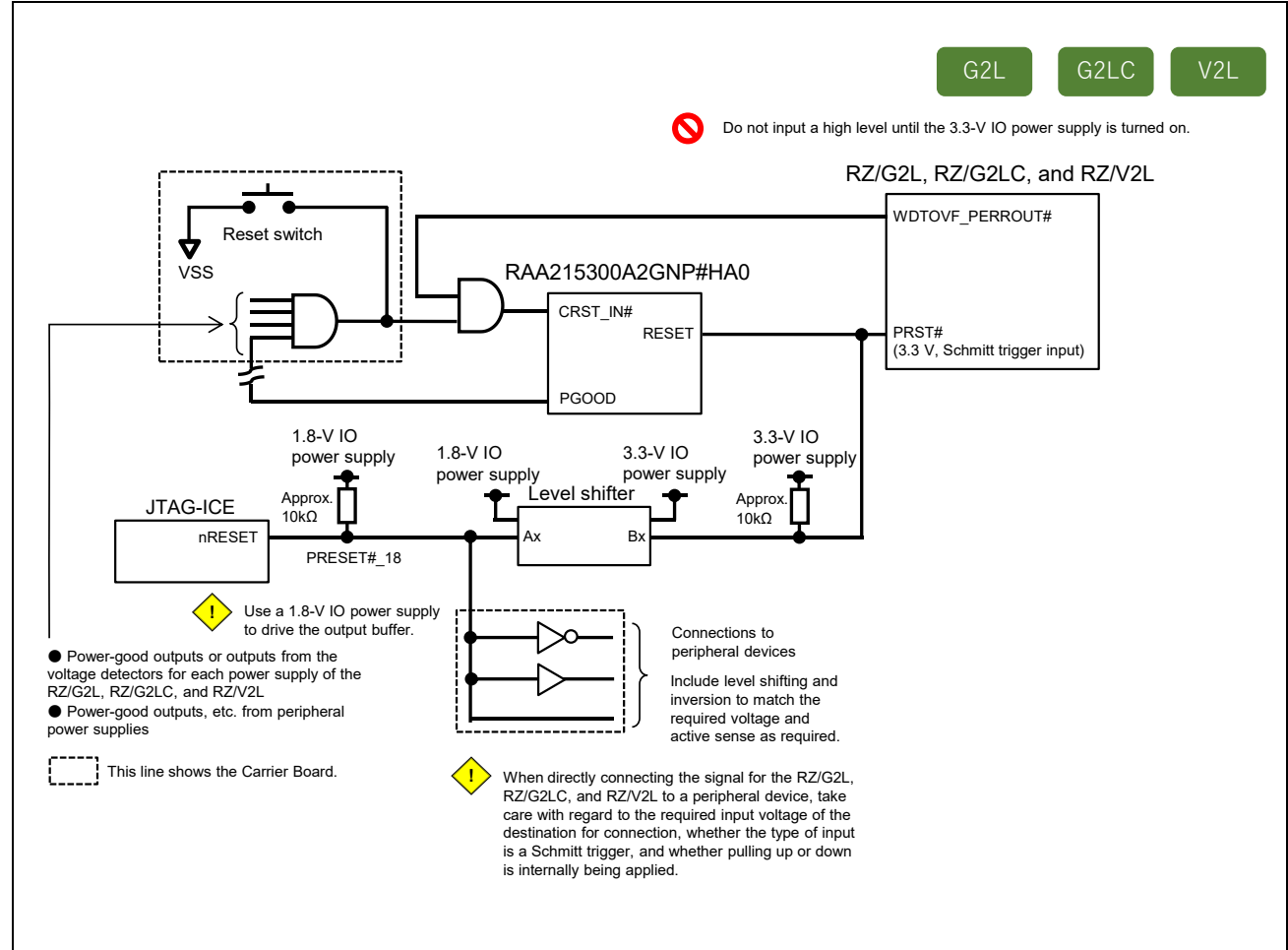


Figure 1.1(b) Example of the Configuration of PRST# for RZ/G2L, RZ/G2LC, and RZ/V2L EVKIT PMIC Edition

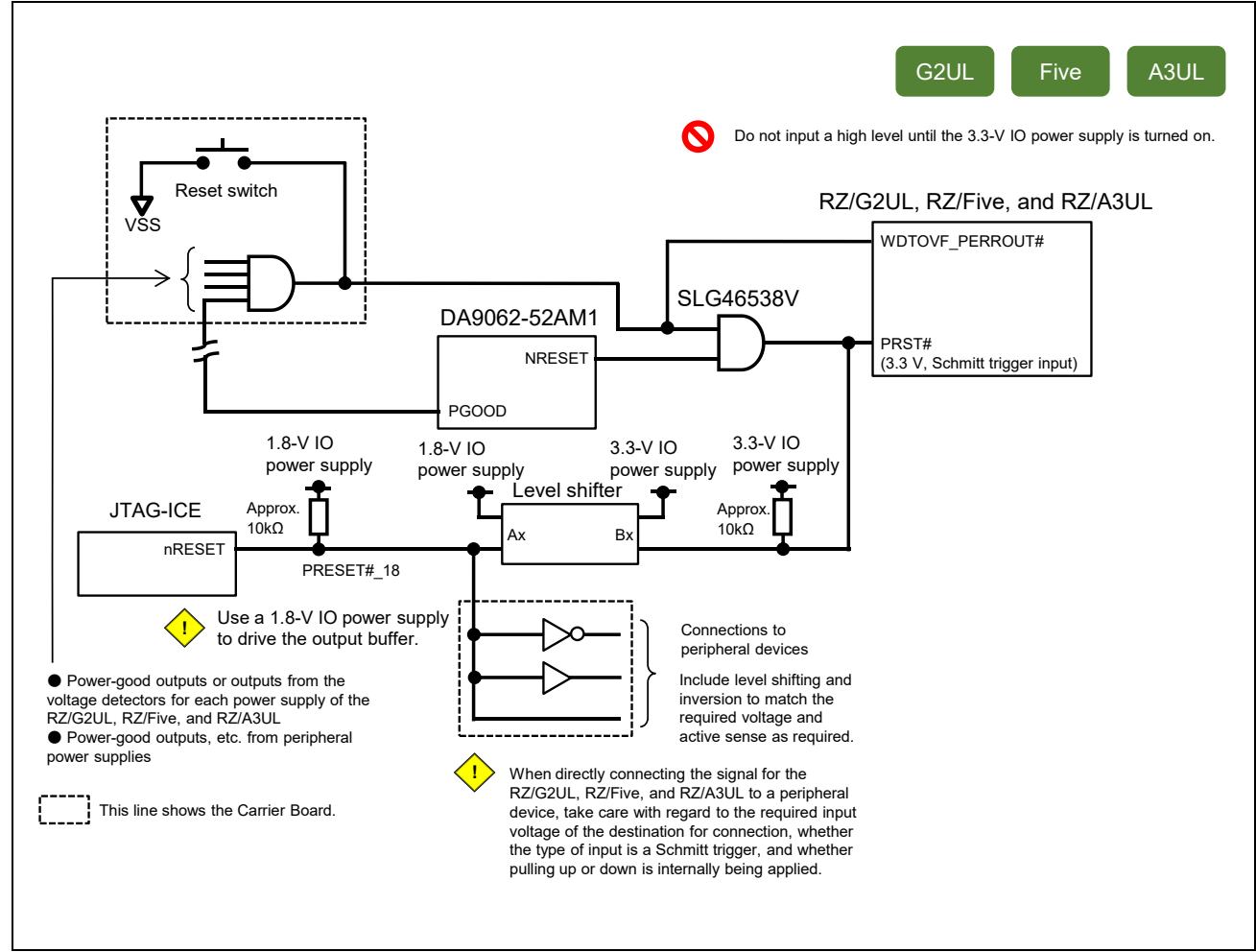
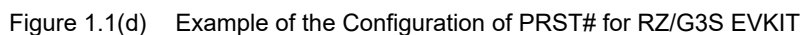


Figure 1.1(c) Example of the Configuration of PRST# for RZ/G2UL, RZ/Five, and RZ/A3UL EVKIT



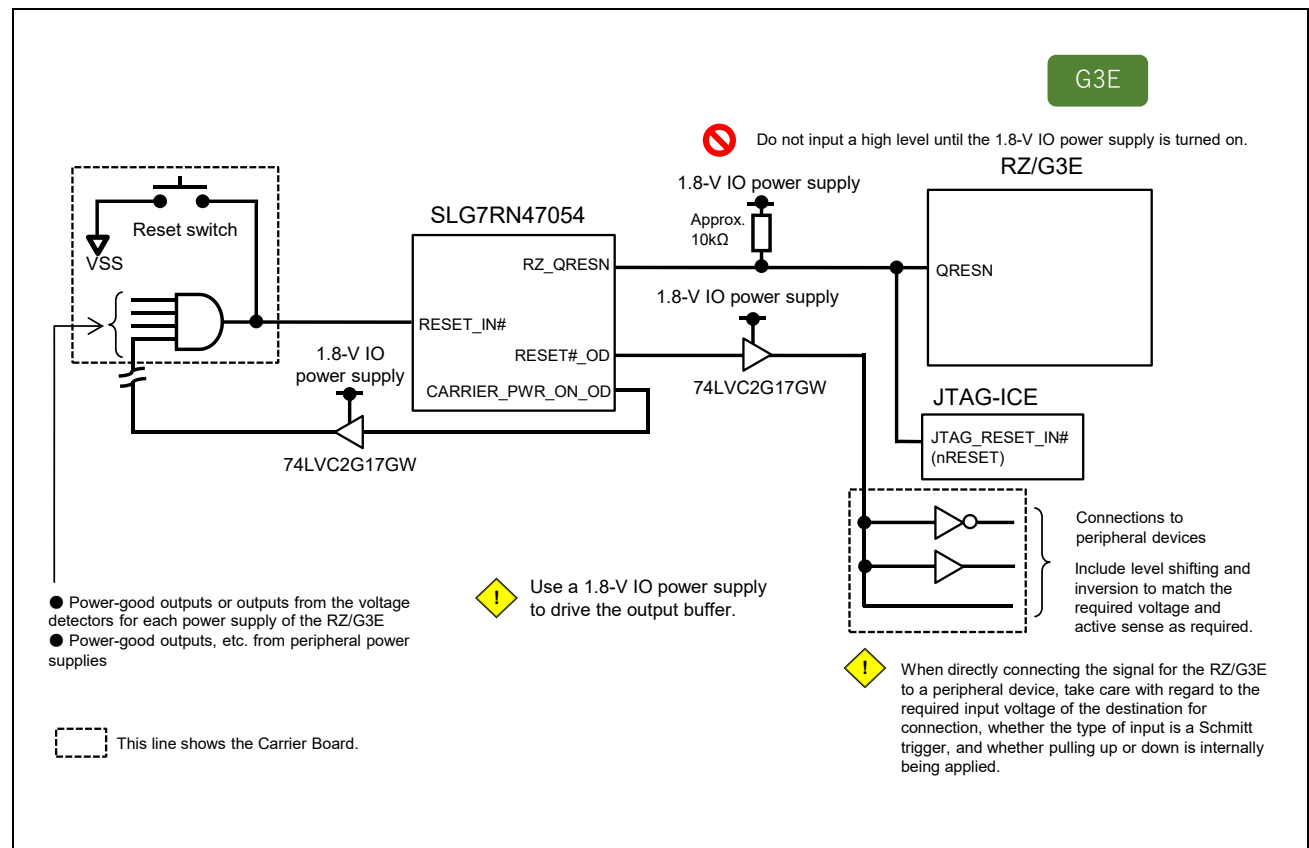


Figure 1.1(e) Example of the Configuration of PRST# for RZ/G3E EVKIT

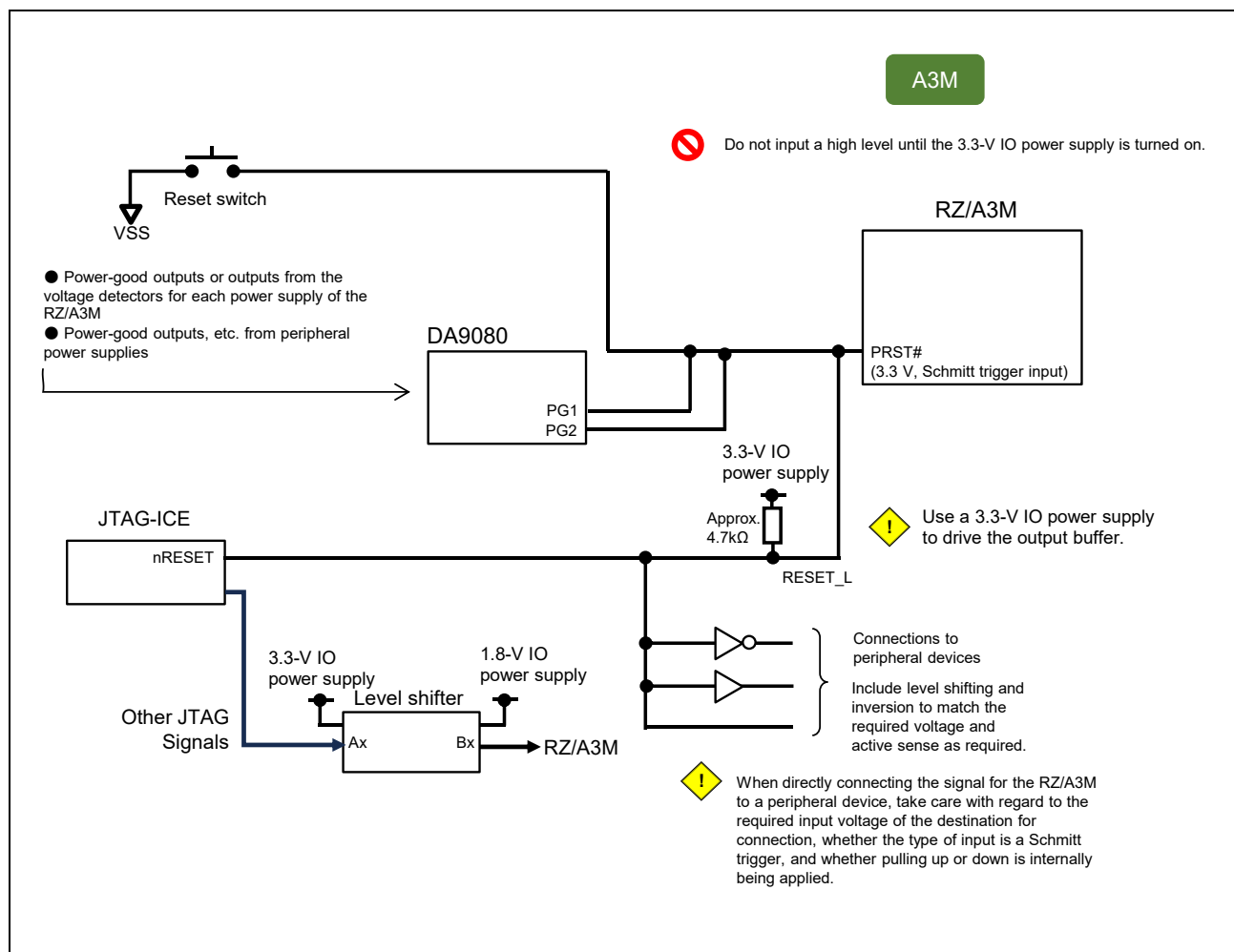


Figure 1.1(f) Example of the Configuration of PRST# for RZ/A3M EVKIT

1.2 Note for the Reset Signal with Open-Drain



Points

ALL

When an open-drain output, wired OR, and voltage level shifter are used in the circuits for generating the reset signals, take care on the following points.

- Peripherals with a reset terminal with Schmitt trigger IO are recommended.
- Take care of the noise.

The effect of noise such as crosstalk is very likely to lead to the incorrect behavior of reset signals. Therefore, apply countermeasures for noise such as separating the reset signal from other signals and applying a grounded guard.

- Determine the pull-up resistor to account for stray capacitance.

The overall wiring length tends to be long because the reset signal branches to other devices and connectors at the edge of the board. As a result, the signal waveform is likely to be dulled by stray capacitance. Consider this when determining the value of the pull-up resistor to be used for the open-drain output.

- Note the pull-up/pulldown resistors scattered throughout the schematic.

If pull-up or pull-down resistors for the reset signal are scattered across multiple pages of the schematic, they may be overlooked and cause unintended operation. For schematic readability, it is recommended that pull-up and pull-down resistors be placed in a single location.

- To clarify the wait time for software initialization to start after reset release, it is recommended to take into account the slow rise of the reset signal.

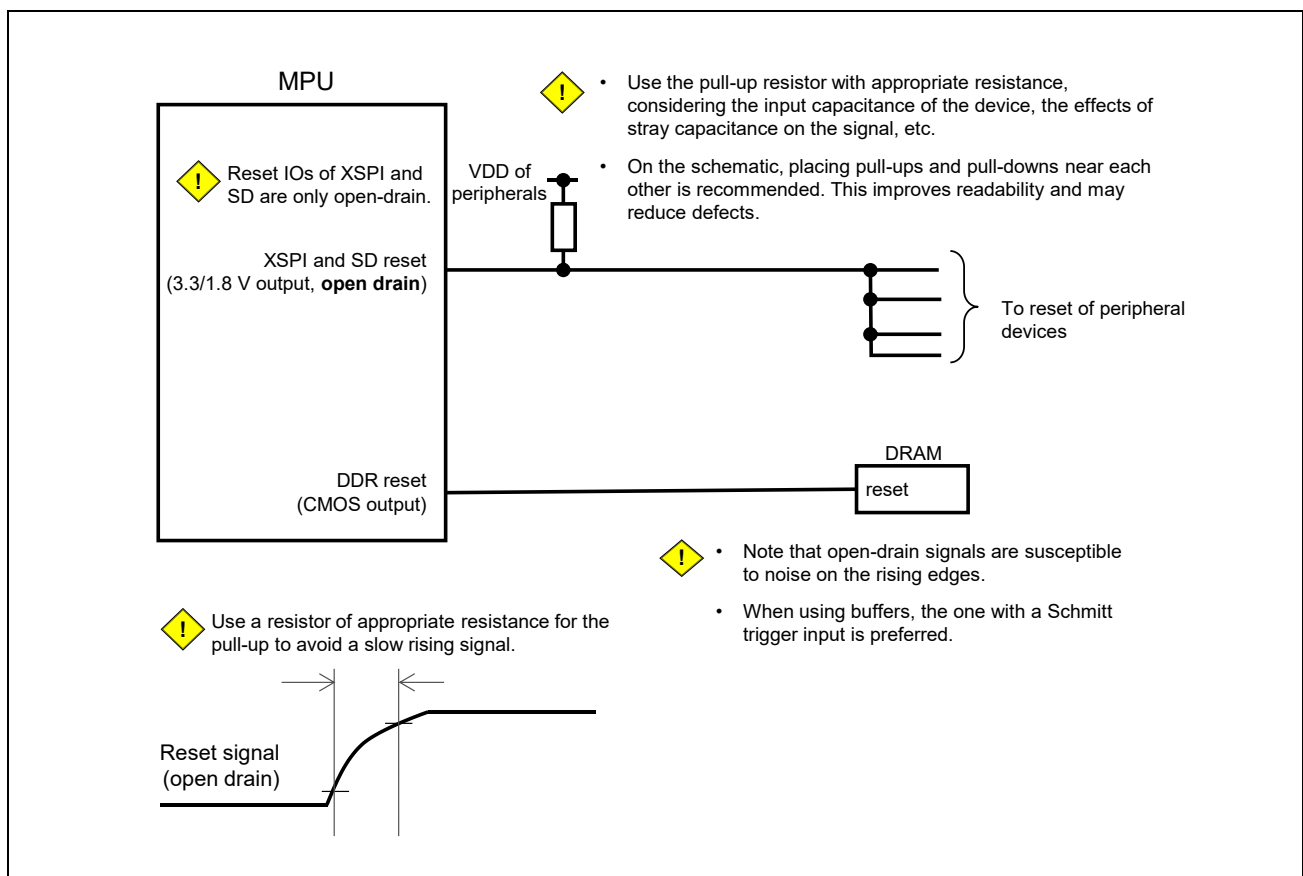


Figure 1.2 Note for the Reset Signal with Open-Drain

1.3 Reset Timing



Points

ALL

- Make sure the following constraints are met for the reset timing.
 - a. During the power-on sequence, the PRST# signal should remain at the low level until all power supplies have been turned on.
 - b. During the power-off sequence, the PRST# signal should be at the low level before any power supply is turned off.
 - c. During power-on sequence, the PRST# signal should be at the low level at least 1ms after the last power supply was turned on. Required 2ms for RZ/G3S.
 - d. When using the PRST# signal to reset the target devices while power is being supplied, hold the signal low for at least 100 ns. RZ/G3S is 0 ms.

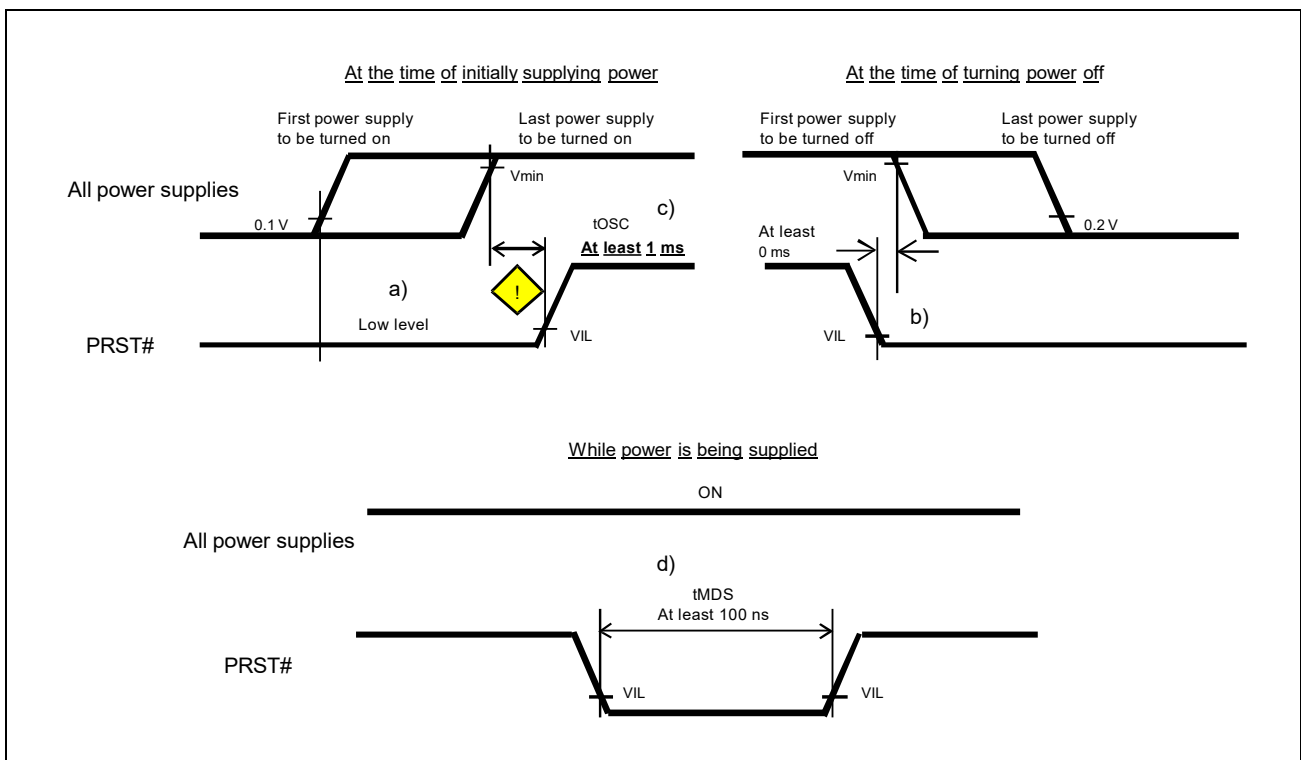
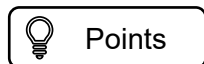


Figure 1.3 Timing of PRST# Input

1.4 Oscillator Stabilization Time



ALL

- When using an external clock through the EXCLK pin, de-assert the PRST# signal after the oscillation is settled. Please refer to the AC characteristics on the User's Manual.

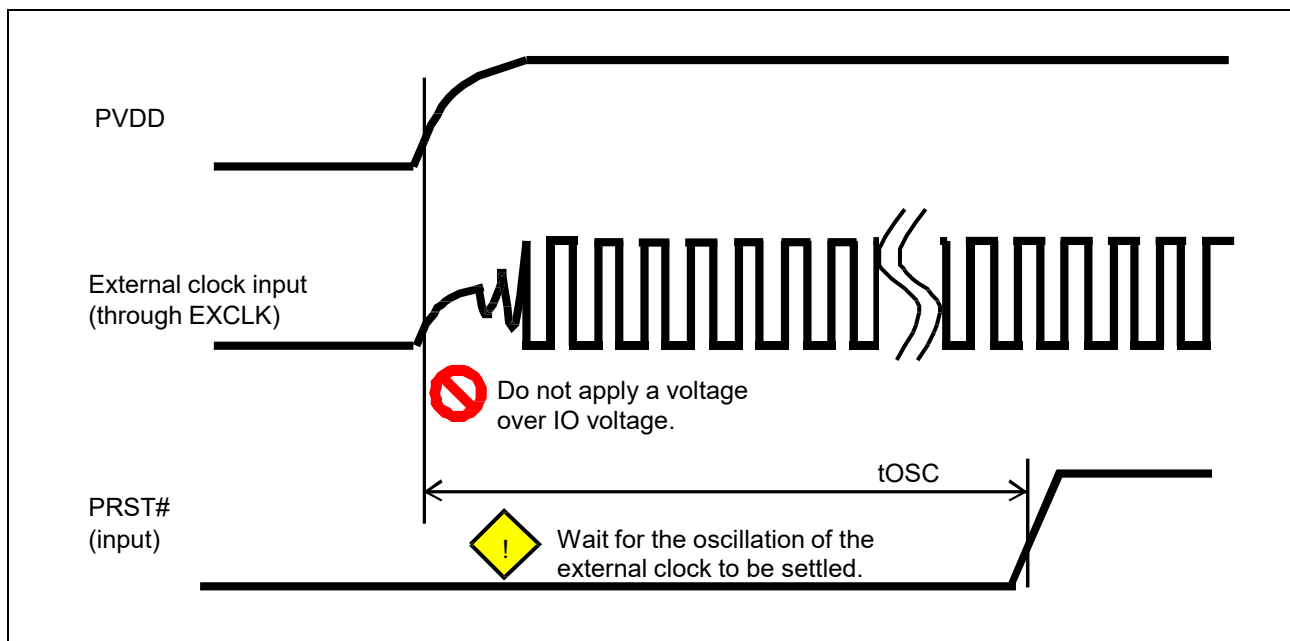


Figure 1.4 Timing between External Clock Input (through EXCLK) and De-assertion of PRST#

1.5 Resetting Peripheral Devices



Points

ALL

- When using the main reset signals PRST# to reset a peripheral device, take care on the following points.
 - Is power to the peripheral device turned on?
 - Are you observing the correct reset sequence for the peripheral device?
 - Is the active sense of the reset signal for peripheral devices correct?
 - When multiple peripheral devices are connected, are you sure that pull-up or pull-down resistors within the individual devices will not cause the voltage of the reset signal to be at an intermediate level?
 - Is the driving ability of the reset signals sufficient?
- When the target devices have reset pins for exclusive use with specific modules such as the DDR_RESET# pin for DRAM and the QSPI_RESET# pin for the SPI Multi I/O interface the SD0_RST# pin for the SD/MMC host interface, use these pins instead of the PRST# pin.

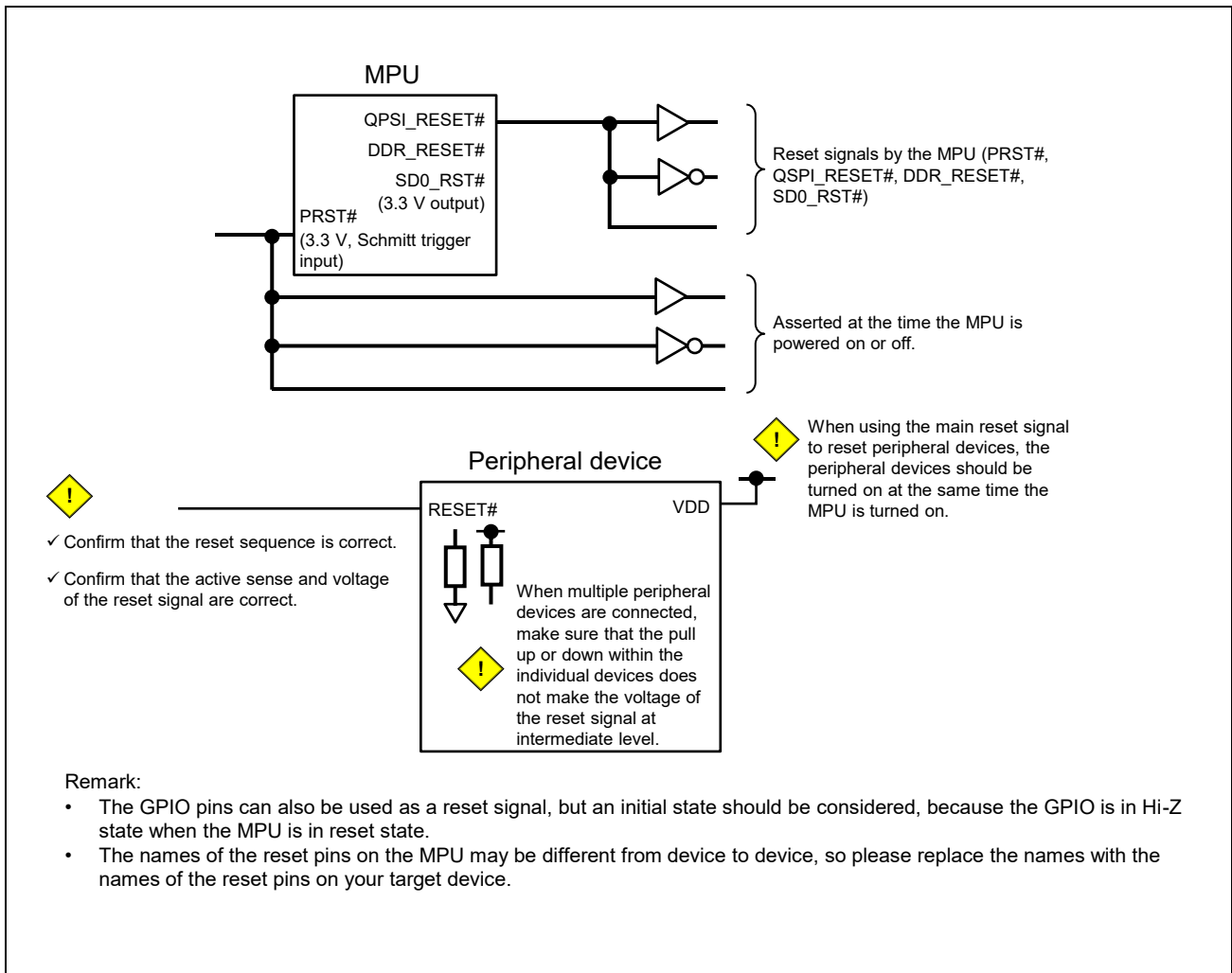
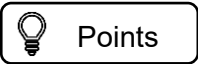


Figure 1.5 Resetting Peripheral Devices

1.6 Mode Pins



The mode pins (MDn) are used to set the initial operating mode. They are implemented with pull-up or pull-down resistors and are captured only one time after the PRST# is released, not after a software reset. The level of the mode pins should be held for a time specified as tMDH.

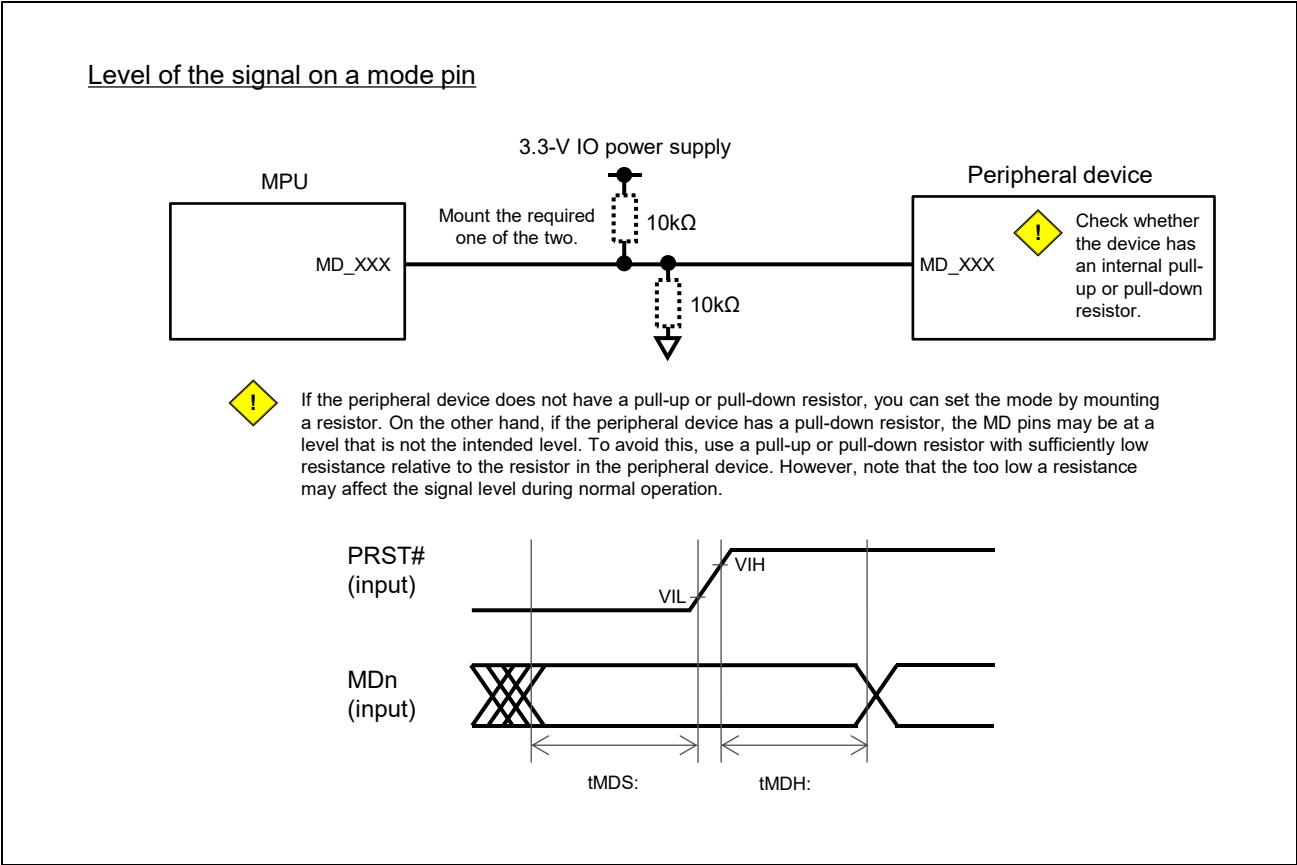


Figure 1.6 Handling the Mode Pins

2. Clock

2.1 Input and Output Clock



Points

ALL

- The voltage of the clock should conform to the voltage of its power domain.

For example of the RZ/G2L, the system clock (EXCLK or XIN) and AUDIO_CLKn are in the 3.3-V IO power domain, but CSI_CLKN/P and DSI_CLKN/P are in the 1.8-V IO power domain. Using a clock input with an incorrect voltage may damage the MPU. Please refer to the “Power” column of the pin function list of the target devices.

- The spread spectrum clock generator (SSCG) cannot be used as the input clock unless specifically stated otherwise in the hardware manual.
- Make sure that the input clock is accurate enough.

The system clock is frequency-multiplied to obtain each kind of clock. Deviation of the oscillation frequency (center frequency) of the input clock (the system clock) affects the center frequency and deviation of the DDR_CK.

- Make sure that whether the output clock of the MPU satisfies with the requirement of the input clock of the external peripheral devices. Refer to the CPG section of the hardware manual.

2.2 Accuracy and Deviation



Points

ALL

- In general, the specifications of crystal resonators are based on the temperature characteristics, the degree to which oscillation may deviate from the oscillation frequency (center frequency), and so on.
- As with crystal resonators, the specifications of crystal oscillators and clock synthesizers are also based on the degree to which oscillation may deviate from the oscillation frequency (center frequency).
- When using the clock generated inside the target devices as the clock source of external peripheral devices or modules, you should be more careful for the deviation of the input clock of the MPU.
- The system clock provides the source of each kind of clock through frequency-multiplication. Any deviation in the frequency of the input clock (the system clock) thus produces deviation in the frequency of clock after multiplication.
- To design a system such that the maximum frequency of the DDR_CK does not exceed the maximum frequency specified for the DRAM, you must select the center frequency of the system clock input in consideration of possible deviation.
- When using MIPI DSI, LVDS, or USB, the jitter of the external clock should be less than the values in **Table 2.1**. On the other hand, when not using any of MIPI DSI, LVDS, and USB, the jitter of the external clock should be less than 80 ps.
- We recommend using clocks with less than 50 ppm frequency deviation. Since the RZ/A3M has no RGMII interface, less than 100 ppm is acceptable.

Table 2.1 Maximum Value of EXCLK Jitter

Module	Symbol	Parameter		Max	Unit
USB 3.2 Gen. 2	RPJ	RMS Phase Jitter	12 kHz – 20 MHz	2.3	ps, rms
			2 MHz – 20 MHz	1.7	ps, rms
	DJ	Reference clock deterministic jitter	1 MHz – 100 MHz	7.4	ps, pp
			3 MHz – 20 MHz	3.7	ps, pp
LVDS	DJ	Reference clock deterministic jitter	—	40	ps, pp
MIPI DSI	DJ	Reference clock deterministic jitter	—	40	ps, pp
USB2	DJ	Reference clock deterministic jitter	—	40	ps, pp
Others	DJ	Reference clock deterministic jitter	—	80	ps, pp

2.3 Crystal Oscillator Circuits



Points

ALL

- For the load capacitance, damping resistance and feedback resistance of the crystal oscillator circuit, determine appropriate values based on the evaluation of oscillation by the selected crystal resonator manufacturer.
- For the provisional value of the load capacitance before evaluating the oscillation, select a value that meets the characteristics of the resonator.
- A feedback resistor can be removed, but it depends on the characteristics of a crystal oscillator and circuit configuration and layout. Please make your decision based on the oscillation evaluation.
- In evaluating the oscillation, adding a feedback resistance is relatively easy, but adding a damping resistance is difficult. Select the value of the damping resistor in consideration of adjustment in evaluating the oscillation.
- Observe the following notes for the crystal oscillator circuit, even though they are not stated in the hardware manual:
 - Bypass Capacitors
Insert laminated ceramic capacitors as bypass capacitors for each VSS/VCC pair. Mount the bypass capacitor near the power supply pins of the LSI. Use components with a frequency characteristic suitable for the operating frequency of the LSI, as well as a suitable capacitance value.
 - Notes on Using a PLL Oscillation Circuit
Keep the wiring from the PLL VDD and VSS connection pattern to the power supply pins short, and make the pattern width large, to minimize the inductance component. The analog power supply system of the PLL circuits is sensitive to noise. Therefore, system malfunction may occur by the intervention with another power supply. Do not supply the analog power supply with the same resource as the digital power supply of VDD and VCC.
 - When Using an External Crystal Resonator
Place the crystal resonator, capacitors C_{in} and C_{out} , and damping resistor R_d as close to the XIN and XOUT pins as possible. To minimize induction and thus obtain oscillation at the correct frequency, the capacitors to be attached to the resonator must be grounded to the same ground. Do not bring wiring patterns close to these components.
- Observe the following other notes for the crystal oscillator circuit:
 - Do not cross the circuit with other signal lines.
 - Keep the circuit away from lines that carry large currents.
 - Do not ground the circuit to ground patterns that carry large currents.
 - Do not bring signals out from the oscillator circuit.
- The result of our crystal marching evaluation is shown below as a reference example. In our case, a feedback resistance is implemented after evaluation. Please check the specification of the crystal oscillator to be used, and implement the appropriate load capacitance, damping resistor and feedback resistor.

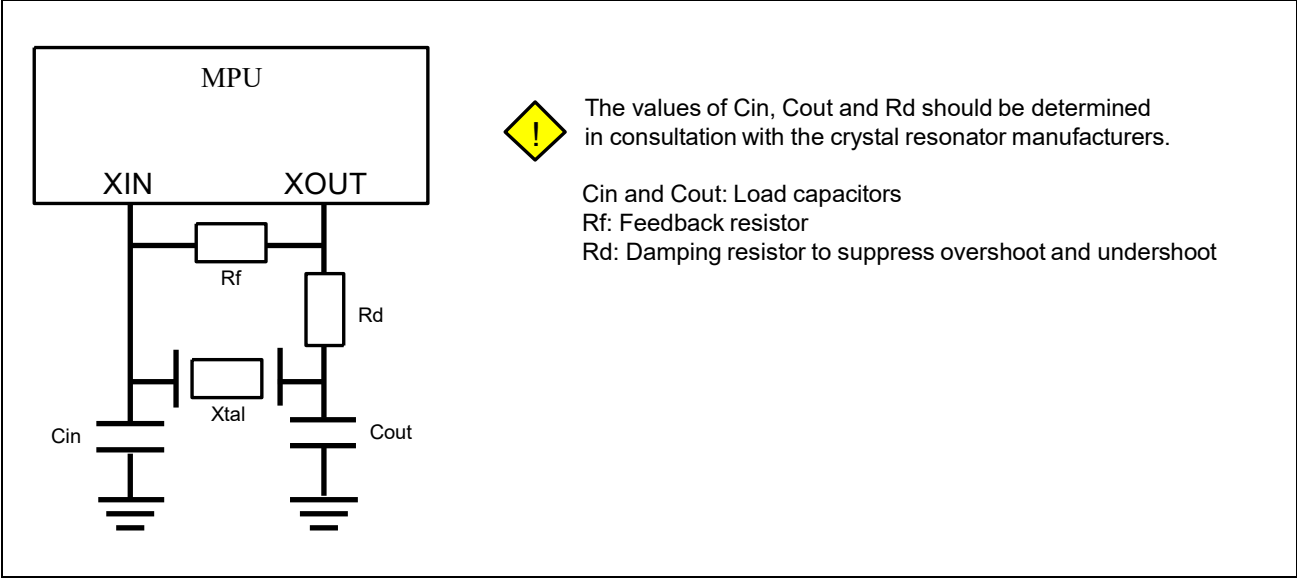


Figure 2.1 Crystal Oscillator Circuit on the EVK

Table 2.2 Characteristics by Recommended Constants (CL = 8 pF)

MPU	Xtal	Rf	Rd	Cin	Cout
G2L, G2LC, V2L	CX1612DB 24 MHz	1MΩ	0Ω	6 pF	6 pF
G3S	CX2016SA 24 MHz	DNF	0Ω	6 pF	6 pF

2.4 Terminal Handling of External Clock Input



Points

ALL

- The MPUs have the XIN and EXCLK pins for crystal clock input and external clock input respectively. Only RZ/G3S has the XIN only for common clock input.
- Check the way to connect a clock source is correct.
- Check the terminal treatments for selecting a clock source, either a crystal resonator or an external clock. Some MPUs require a mode pin setting.

2.5 Oscillator Drive Strength



The MD_OSCDRV pins are for setting the drive strength of crystal oscillators; however, only one setting is supported. Make sure that these pins are connected to ground.

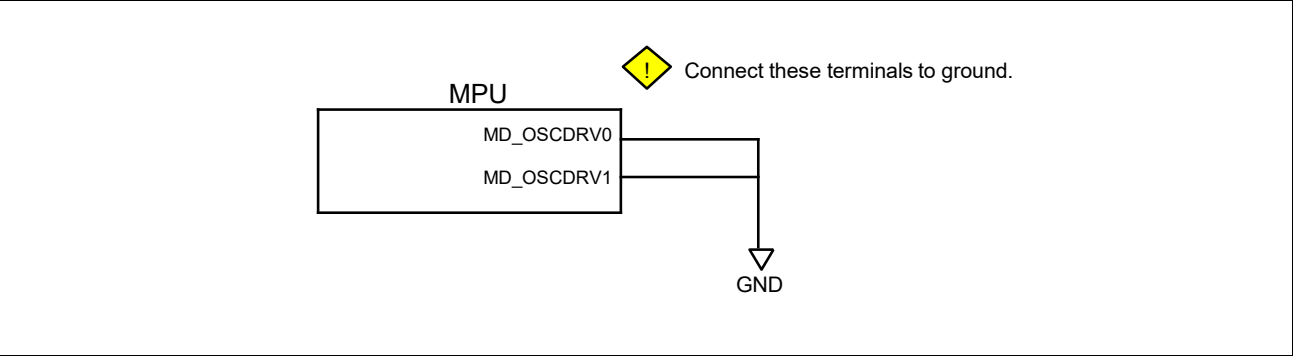


Figure 2.2 Handling of the MD_OSCDRV Pins

2.6 Clock Input for Peripheral Devices



Points

ALL

- It is also necessary to pay attention to the clock input and clock oscillator circuit of peripheral devices. Read the data sheets and manuals of the individual peripheral devices carefully to avoid improper design.
- If you intend to use the output clock of the MPU as the input clock for a peripheral device, pay attention to the voltage of the clock output (the power domain to which the clock pin belongs and the interface level), and the clock frequency and accuracy.
- Please refer to the datasheet of the peripheral devices to be used.

2.7 General Notes on the Clock Circuit and Wiring



Points

ALL

- Pay attention to the following general notes when designing the clock input and clock output circuits. In addition, important points to be considered in PCB pattern design, such as the GND shield, are helpful in circuit diagram review and evaluation after the board is completed. State the important points as notes on the circuit diagram as far as possible.
 - Properly reduce the load on the clock line to prevent malfunctions due to rounding of the clock signals on rising or falling edges. When the load is too large, take measures such as inserting a clock buffer.
 - Avoid unnecessary branches and stubs as much as possible to avoid degradation of the signal quality caused by reflection. Use continuous patterns for branching as much as possible. When the wiring requires a T branch, take measures such as inserting a clock buffer.
 - When inserting a clock buffer, be sure to consider the effect of clock delay. When delay is a problem, take measures such as using a zero-delay buffer.
 - Prepare circuits and pads in consideration of adjustment of the clock quality after the board is completed.
 - Insert a damping resistor such that the resistor is near to the outputting terminal of the clock signal
 - Placing a termination circuit such as a Thevenin termination near to the receiving terminal of the clock signal
 - Use routes that minimize variations in characteristic impedance. Measures for this include keeping routes in the same PCB wiring layer and minimizing the use of via holes in clock wiring.
 - Prevent the wiring for the clock and other signals from running side by side to avoid crosstalk noise and take measures such as applying a ground shield where appropriate.
 - Consider the layout in terms of avoiding excessive noise from switched-mode power circuits and so on.
 - In the case of circuits for selecting from among two or more clock signals, use chip jumper blocks with 0Ω resistors and use a pattern that minimizes the number of stubs.

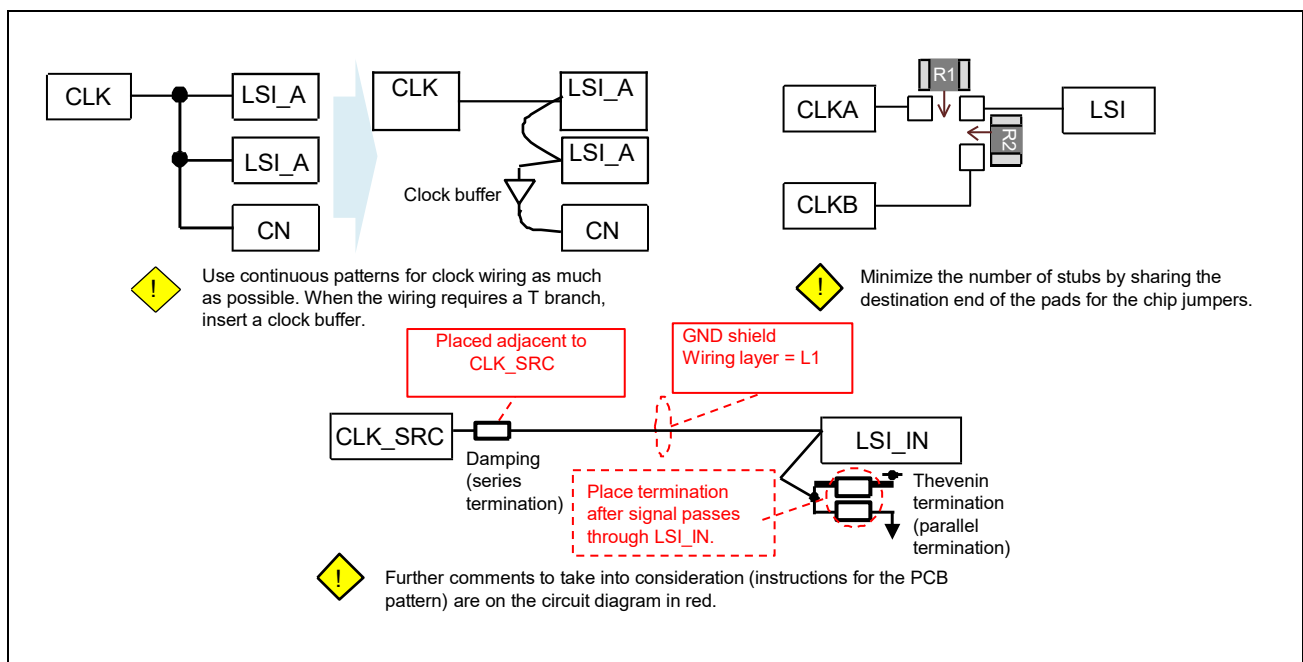



Figure 2.3 General Notes on the Clock Circuit and Wiring

3. Power Supplies

3.1 Capacity for MPU and Peripherals

-  Points

ALL
- In general, the system with the MPU including lots of peripherals such as SD cards, USB, memory devices like DRAMs, and communications devices, etc., requires a wide variety of power supplies. Then its power system is likely to be complex.
 - The logic power supply has to be able to provide particularly large currents, so its capacity to supply power should be designed with a margin that allows for increases above the estimate of current drawn.
 - For a power supply that is to be the source of multiple power supply voltages, take measures in consideration of the efficiency of each power supply IC, such as stepping down voltages in two stages.
 - In order to “visualize” the possibility of power capacity being insufficient, we recommend that you create a calculation sheet, such as a power tree.
 - Please refer to the datasheet for the electrical characteristics of the power supply IC and peripheral devices to be used.

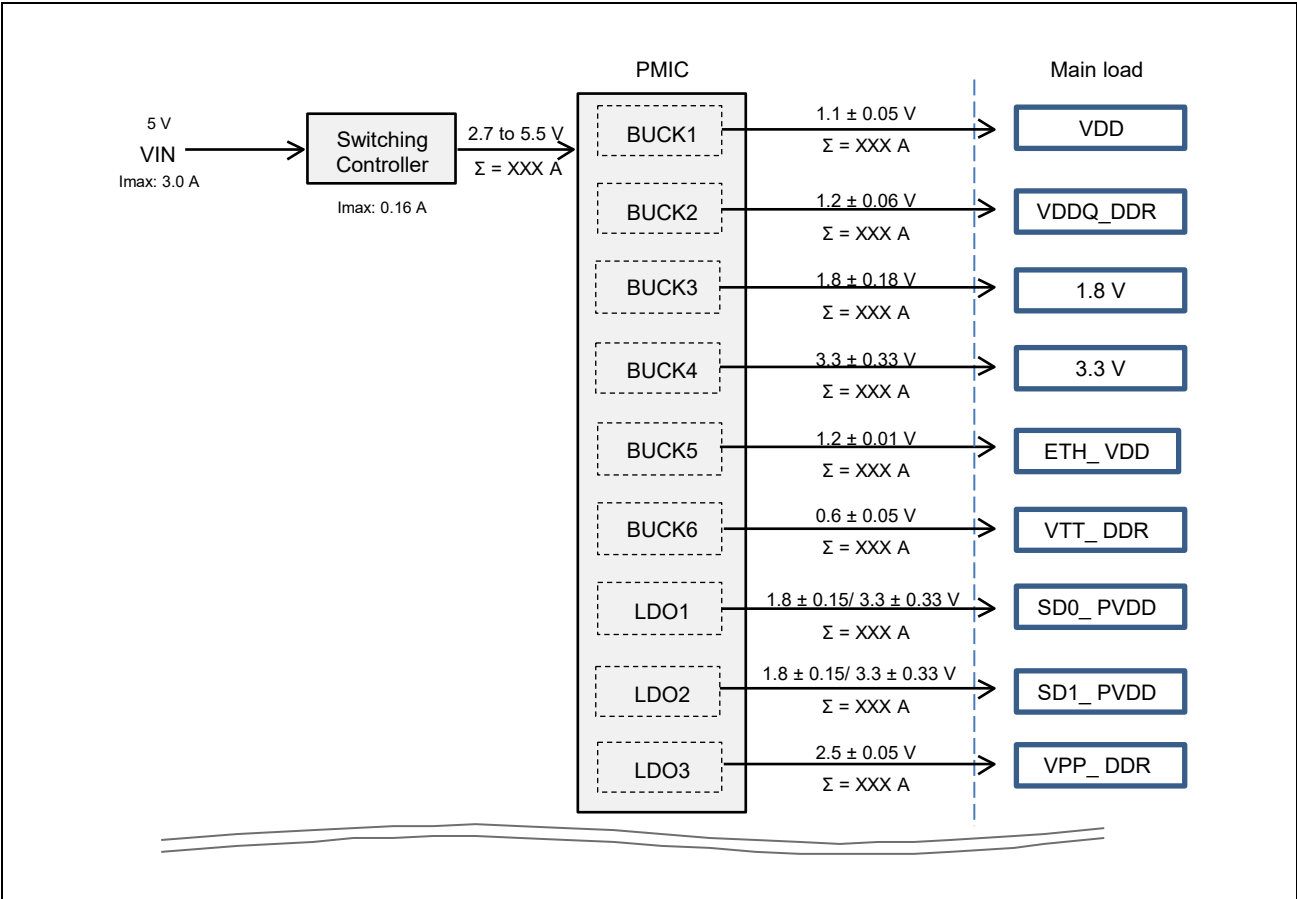


Figure 3.1 Example of a Power Tree

3.2 Capacity for VDD



Points

ALL

- When selecting a power supply IC for the logic power supply, make sure that its specifications satisfy the requirement of all the power supply of the MPU, where the specification includes such as the load regulation and load response. For example, the load regulation ability for the power supply IC should satisfy the VDD specification of the MPU.
- Simply calculating, on a desk, the maximum current drawn from the electrical characteristics, and designing the power supply capacity with a margin based on the results of calculation is desirable. However, designing a power supply that allows a margin of two or three times for the maximum current is not easy without significantly increasing costs. The following methods can be used to reduce the cost of the power supply by estimating the details of the standard power consumption.
 - Setting the power supply voltage to $TYP + \alpha$ (allowing for the accuracy of the power supply voltage) to be set for the power supply IC, rather than to the maximum value in the specification
 - Excluding (from the estimate) modules that are not to be used among the internal modules
 - Using duty ratios based on anticipated use cases rather than current drawn during full operation
 - Implementing a margin based on addition rather than multiplication (for example, using +1 A or 2 A instead of two to three times the maximum value)
- If the margin is reduced, the instantaneous peak of the current drawn might exceed the power supply capacity. The following methods can be used to compensate for this.
 - Using several capacitors with large capacitances, such as 10 to 100 μF , to absorb sudden increases in load current
 - Increasing the response of the power supply IC, by increasing the switching frequency of the power supply IC by a value of the order of several MHz, and implementing a multi-channel power supply IC configuration
 - Limiting the overcurrent protection of the power supply IC to the original maximum current + α to prevent unexpected shutdowns
- Finally, if you have not secured adequate margins on your desk, perform sufficient evaluation with the actual machine and software by increasing the number of boards to be evaluated and verify whether power supply integrity is maintained. In addition, you must consider advance measures for shortages of power capacity.
- Please refer to the datasheet of the power supply IC to be used.

3.3 Supply Voltage and Power Sequence

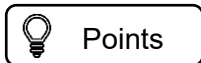


Points

ALL

- Check that the power up and down sequence described in the electrical characteristics of the user's manual.
 - We strongly recommend drawing a timing chart of the power up and down sequences of all the power supplies including the reset system of the MPU and peripheral devices.
 - Regarding the sequence of switching power off, the before-and-after relations of items in the sequence might change depending on whether a discharge circuit is present. Therefore, also consider the effect of a discharge circuit on the sequence.
 - Make sure that the rising or falling of the supply voltage is not excessively long. Although the slope (mV/s) of the rising or falling of the power supply voltages is not specified, a monotonic increase or decrease is assumed.
- In the power supply sequence, the condition for the next power-on is that the power supply voltage must have dropped below the rated value when the power supply was turned off last time. Therefore, it should be noted that turning the power supply back on when the power supply voltage has not sufficiently dropped due to insufficient discharge is strictly a violation of the rated value.
- For the evaluation phase, we recommend configuring the initial hardware to allow adjustment for the defect in the power supply sequence. For example, use a PMIC and a MCU which change the control program of the PMIC, and prepare a pattern for a discharge circuit.
- Note the voltage tolerance of the signal pins with pull-up. Not only pins on the MPU, but also the ones on peripheral devices.

3.4 Noise Filter



Points

ALL

- Make sure to place noise filters for dedicated power rails such as the PLL. It is not recommended merging multiple power rails and filtering with one filter. Refer to the guidelines for each interface.
- The noise filter circuit of the PLL power supply on the EVK has a proven track record, so we recommend reusing the filter circuit.

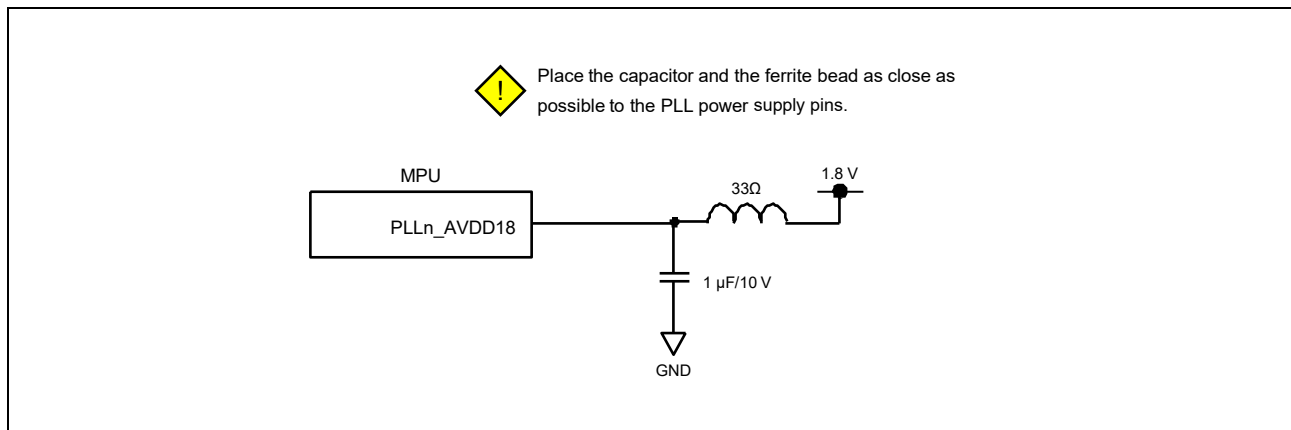


Figure 3.2 Example of the Filter Circuit for the PLL Power Supply

3.5 Impedance Design



Points

ALL

Power supplies that require high current, such as VDD, which is a logic power supply, and power supplies for noise-sensitive high-speed signal interfaces such as DDR require a PCB design that takes signal impedance into account.

We provide the following guidelines. Please refer to them. We strongly recommend that the target value be in accordance with these guidelines to reduce the risk of malfunction.

[VDD]

- PCB verification guide for Core VDD

[DDR]

- PCB verification guide for DDR4/DDR3L
- PCB design guideline for DDR4/DDR3L
- PCB verification guide for LPDDR4/DDR4 (for RZ/G3S)
- PCB design guideline for LPDDR4/DDR4 (for RZ/G3S)

[High speed signal interface]

- PCB design guidelines for High-Speed Signal Interfaces

3.6 Bypass Capacitors



Points

ALL

- There are no recommended capacities for bypass capacitors for the general-purpose digital IO power supplies of the target devices; however, use the evaluation board kit as a reference to determine the appropriate number and capacity of bypass capacitors.
- It is desirable to use a single ceramic 0.1- μ F capacitor per pin of the IO power supply as a bypass capacitor. However, arrange the appropriate number of capacitors in consideration of the signal operating frequencies, the number of operations that will simultaneously be in progress, and the priority of other power bypass capacitors and filter circuits.
- If many signals are operating simultaneously, place a capacitor with a relatively large value of about 10 μ F at the end of the PCB IO power supply pattern.
- Confirm that the bypass capacitors for peripheral devices are appropriate, as well as the MPU. The recommended capacities and PCB wiring patterns might be stated in the provided data sheets and technical documents of some devices.
- Coordinate with the PCB pattern designer with regard to obtaining the best implementation of bypass capacitors, such as their placement near the target power supply pins and the capacitance values, by stating them in notes. For example, bypass capacitors for the BGA parts should be 0.1 μ F or less when located within the area on the other side of the board under the LSI, and at least 1 μ F when not located within the area on the other side of the board under the LSI.
- Please refer to the datasheet of the peripheral devices to be used.

3.7 Selecting Ceramic Capacitors



Points

ALL

- When a multilayer ceramic capacitor is used as a bypass capacitor, the effective capacitance decreases depending on the DC bias characteristics and temperature characteristics.
- For details, check the characteristics provided by the manufacturer of a capacitor. However, the trends are as follows:
 - The rate of decrease of the effective capacitance depends on the dielectric of the capacitor in use.
 - The effective capacitance tends to decrease with the working voltage margin for withstand voltage.
 - For capacitors with relatively high capacitance (10 μF or higher), the effective capacitance decreases significantly with the body size.
- Note that when a capacitor with a large capacitance is used to support sudden changes in the load current, the desired effect might not be fully obtained due to a decrease in the effective capacitance.
- Make sure that the withstand voltage of the capacitor is at least three times the working voltage.
- If the decrease in the effective capacitance is a problem, also consider the capacitor characteristics: F, X5R (= the dielectric in use).
- When you select a capacitor with a small body, pay attention to the decrease in the effective capacitance. In terms of the effective capacitance, the effective capacitance of two small capacitors can correspond to that of a single larger capacitor.
- Please refer to the datasheet for the electrical characteristics of the multilayer ceramic capacitor to be used.

3.8 Design of the Power Supply IC Circuit



Points

ALL

- The datasheets and technical documents for power supply ICs usually cover the reference circuits useful for configuring power supply circuits.
- Especially for switching regulators, the power supply quality might be significantly degraded depending on the circuit constants, or oscillation might occur. Therefore, the manufacturer and model number of the components used in the provided reference circuits are amply stated in many cases.
- Verifying the selection of specific components and the margins (for phase and gain) by using a simulation tool might be possible.
- When you design power supply circuits, use the technical information and reference circuits provided by the power supply IC manufacturers to make sure that the recommended circuits and constants are observed.
- The recommended designs for PCB wiring patterns and heat dissipation might also be stated, follow the recommendations.
- Carefully confirm the specifications of the coils, FETs, diodes, and other components that need to be selected according to the current drawn in the actual use cases so that they do not violate the ratings. We also recommend writing comments regarding the confirmed characteristics on the circuit diagram to help in component selection at design reviews and in response to changes of specifications.
- Pay attention to the allowable losses (W) when inserting a shunt resistor into the power supply line for current measurement.
- Please refer to the datasheet of the power supply IC or peripheral device to be used for the electrical characteristics.
- Please refer to the datasheet for the electrical characteristics of the components used in power supply circuits and power supply IC to be used.

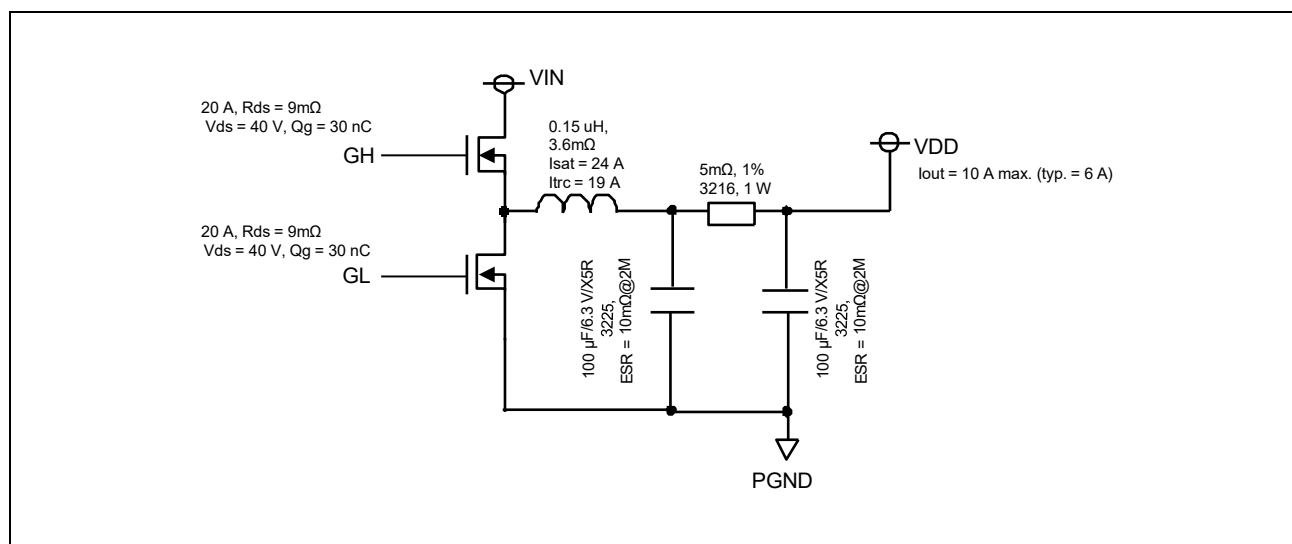


Figure 3.3 Example of Stating the Characteristics of Peripheral Power Supply Components

3.9 Remote Sensing of the Output Voltage by the Power Supply IC



Points

ALL

Recently, current for the logic power supply has increased and the power supply voltage has gotten lower. So the power supply ICs that have a function sensing the output voltage to improve the quality of a power supply have been appearing. The quality of supplying power can be maintained by placing a remote sensing pin near the load (the LSI) and canceling out IR drops in the power supply line. We provide some general notes here.

- Sense the voltage at the point as close to the power supplies as possible. Sensing the voltage at the pin of the power supply on the MPU is preferable; however, this is often difficult.
- As with other noise-sensitive signals, take countermeasures to avoid noise, such as avoiding parallel runs of remote sensing and other signal wiring, and using ground shields.
- If a paired GND signal is provided, wire the GND signal and the remote sensing signal in a pair, and take the above precautions against noise as well.

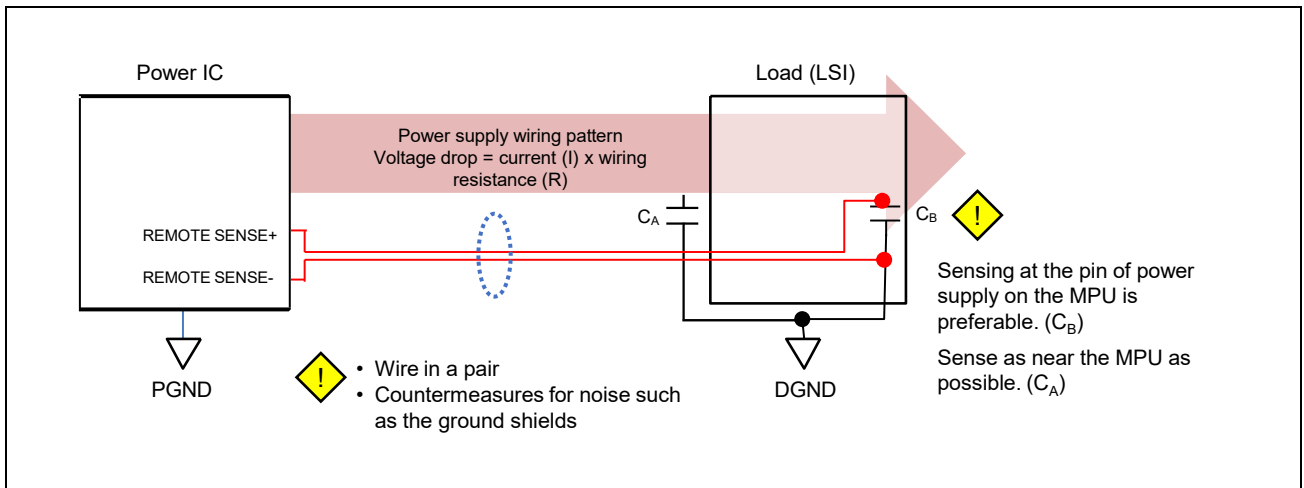


Figure 3.4 Remote Sensing Input of a Power Supply IC

3.10 Supplying Power through Connectors



Points

ALL

- When supplying power through a connector, be sure to provide sufficient power supply pins and GND pins for the maximum current value.
- Calculate the amount of current per pin from the allowable current and contact resistance of the connector pin.
- According to the amount of current near the connector, place a capacitor with a relatively large capacitance and generally consider the design in terms of making sure that changes in the power supply voltage due to changes in the current drawn will not become a problem.
- Please refer to the datasheet of the connectors to be used.

3.11 SD

3.11.1 Power Supply Circuit for the SD card Interface



Points

ALL

- When power is applied to an SD card, the inrush current may place a heavy load on the source power supply and make the system unstable.
- Depending on the card in use, the current may have large fluctuations. Determine the capacitance of a bypass capacitor for the card power supply based on actual evaluation.
- If the inrush current when the power is turned on is excessively large, you can reduce it by using a high-side switch with a soft start function.
- If the bypass capacitor placed adjacent to the SD card and SD card power connector needs to be discharged quickly when power to the SD card is switched off due to removal of the card, use a high-side switch with a discharge function. If quickly discharging the capacitor is not necessary, discharge it through a resistor with a value of about 1k Ω .
- Please refer to the datasheet of the peripheral devices to be used.

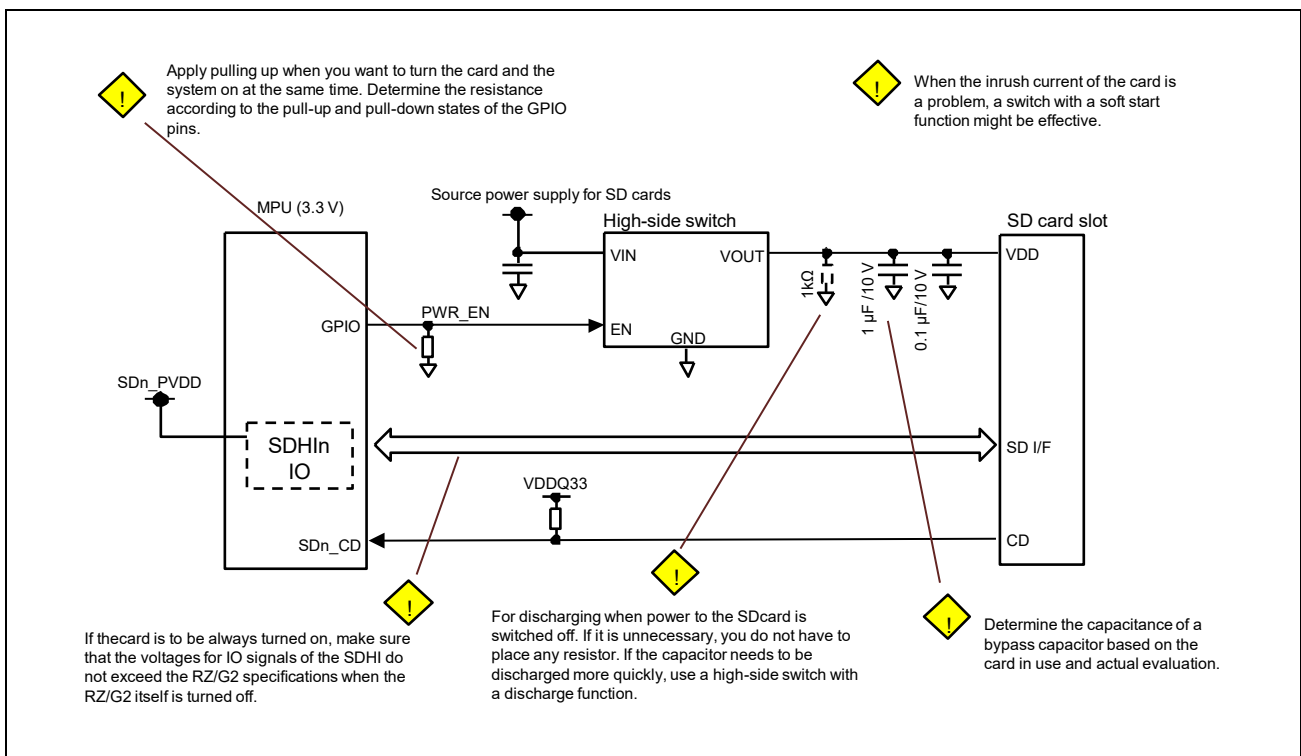
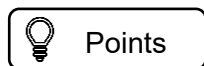


Figure 3.5 Example of a Power Supply Configuration for an SD Card Slot

3.11.2 Switching the IO Power Supply Voltage



ALL

The MPU supports the 1.8 V and 3.3 V IO power supply voltage for SDHI.

- When dynamically switching the IO power supply voltage, make sure that the voltage does not exceed the specifications.
- In particular, when using a two-input high-side switch, be careful not to have a guard band that prevents the switches from being turned on at the same time during switching.

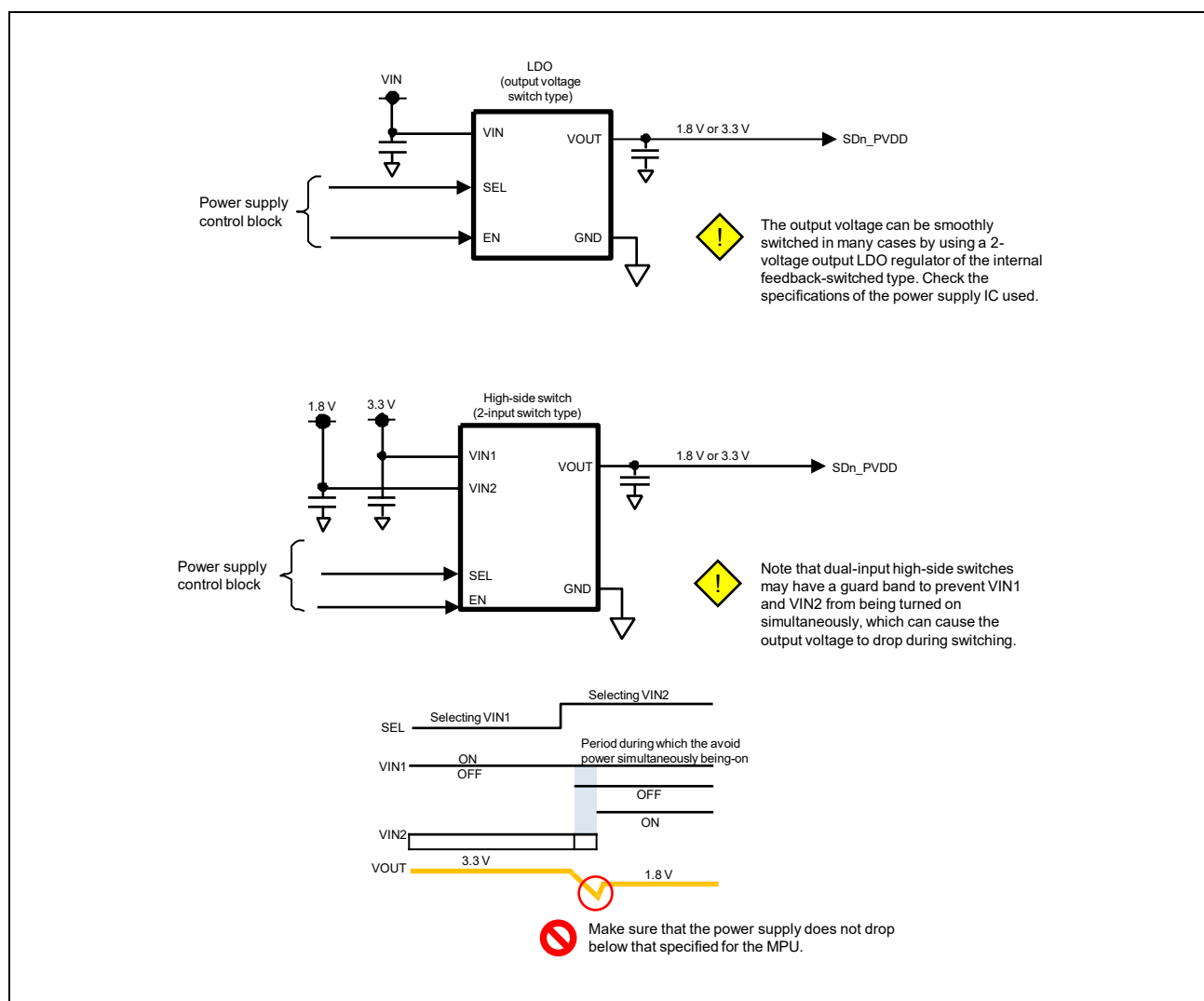
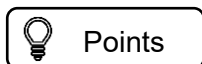


Figure 3.6 Switching the IO Power Supply Voltage of the SDHI

3.12 Reverse Current through USB 2.0 Power Supplies



G3E

The reverse current can flow in the following two cases: when the VBUS is powered while the MPU is powered off, and when the USB is in suspend mode. Please take care of them according to your case with the following examples.

A load switch or similar component should be placed between the VBUS and the USB20_VUBUSIN so that 5 V is supplied from the VBUS to the USB20_VUBUSIN after the USB power supplies such as the USB2_VDD33 and the USB20_VDD18 are turned on. This prevents the reverse current via the USB20_VUBUSIN from flowing from the power supply terminal of the MPU to the power supply IC during the USB2_VDD33 and the USB20_VDD18 are turned off. (**Figure 3.7**)

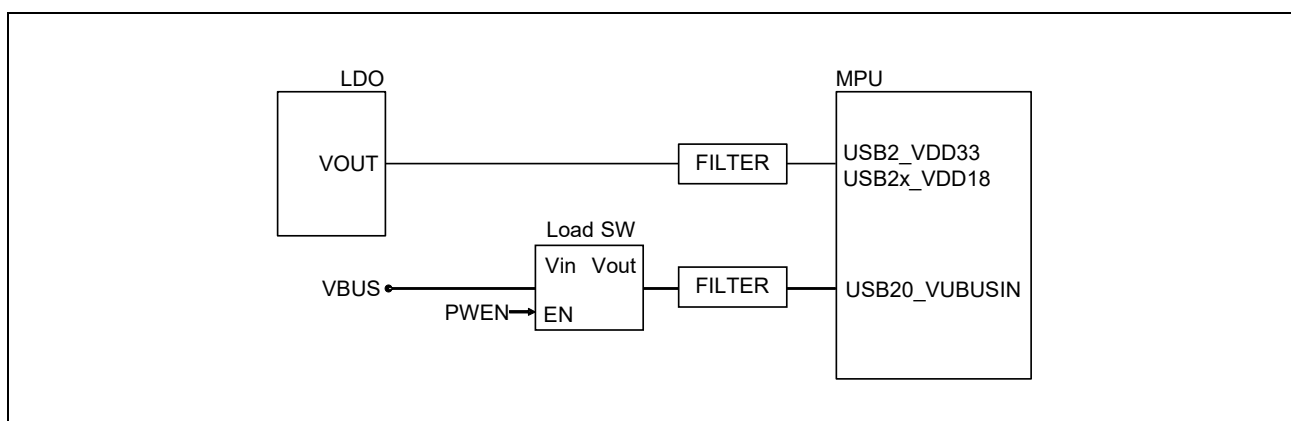


Figure 3.7 Reverse Current from the VBUS

If the USB2_USDVDD 0.8 V power supply is powered by a single power supply and is not shared with other 0.8 V power supplies, a 2.2kΩ resistor should be placed between USB2_USDVDD and GND. This prevents the reverse current from flowing from the power supply terminal of the MPU to the power supply IC during USB suspend. (**Figure 3.8**) If the USB2_USDVDD is shared with other power supplies, the resistor is not needed because the leakage current flows to other power supply terminals (**Figure 3.9**).

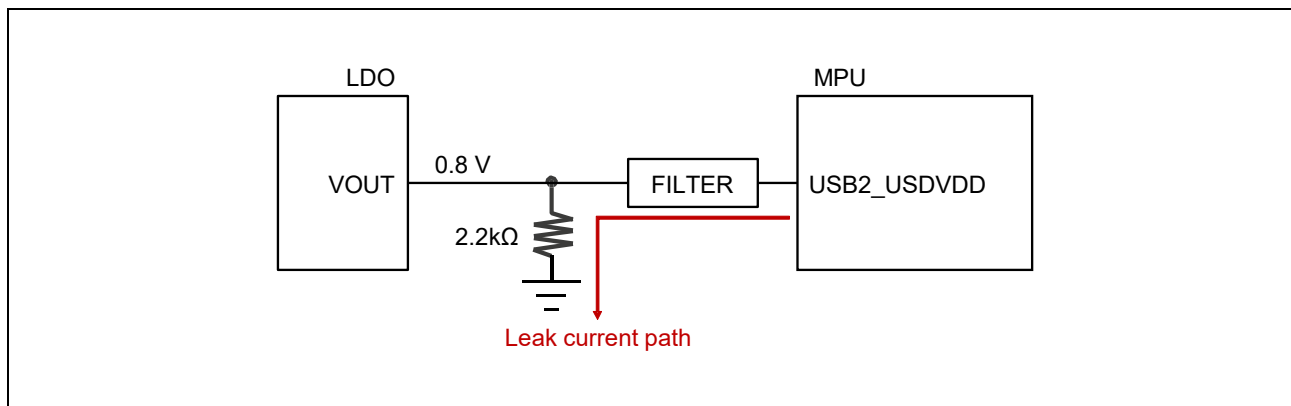


Figure 3.8 Reverse Current from USB2x_USDVDD without Branch

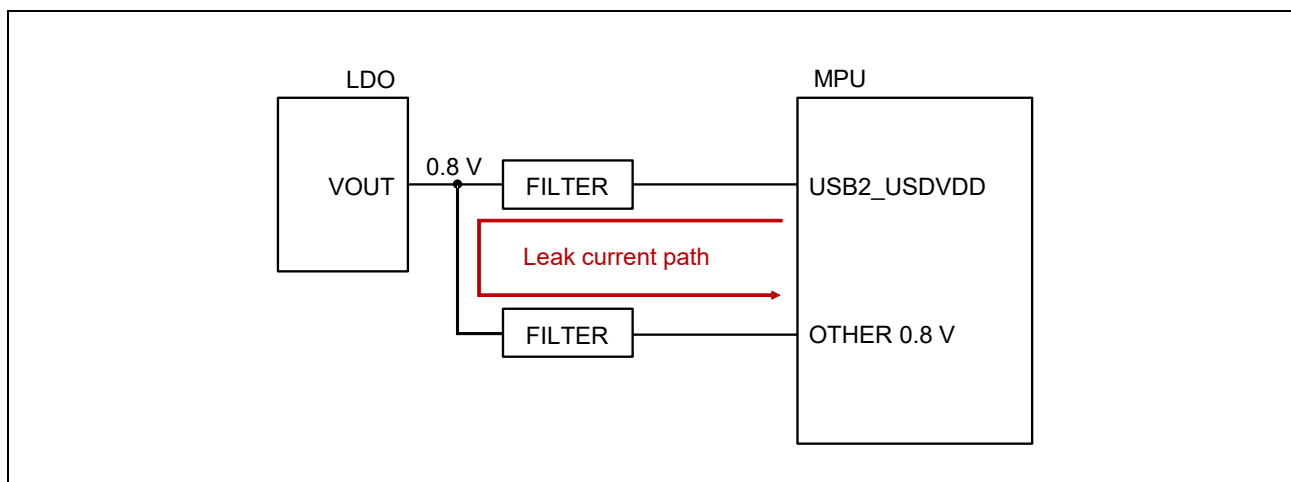


Figure 3.9 Reverse Current from USB2x_USDVDD with Branch

4. High-Speed Interfaces

4.1 Other Guidelines and Documents

 Points

ALL

We are providing the design guidelines for high-speed signal interfaces except for DDR interface. Be sure to follow the guidelines to verify the design.

Table 4.1 Guidelines Related to the PCB Design of High-Speed Serial Interfaces

Interface	Guideline/External Guideline Documentation Referred to by the Renesas Guidelines
USB 2.0	<ul style="list-style-type: none">• PCB design guidelines for High Speed Signal Interfaces• High Speed USB Platform Design Guidelines Rev1.0 Download from https://www.usb.org/
CSI	<ul style="list-style-type: none">• PCB design guidelines for High Speed Signal Interfaces
DSI	<ul style="list-style-type: none">• PCB design guidelines for High Speed Signal Interfaces
PCIe	<ul style="list-style-type: none">• PCB design guidelines for High Speed Signal Interfaces• Board Design Guidelines for PCI Express™ Architecture Download from https://members.pcisig.com/

4.2 DDR

This chapter describes the points to note regarding DDR design. For detailed design methods, please refer to the following guidelines.

Reference Documents:

- PCB design guideline for DDR4/DDR3L
- PCB design guideline for LPDDR4/DDR4
- PCB design guideline for LPDDR4/LPDDR4X
- PCB verification guide for DDR4/DDR3L
- PCB verification guide for LPDDR4/DDR4
- PCB verification guide for LPDDR4/LPDDR4X
- DDR board config structure generation tools for individual target devices

4.2.1 Supported DRAM Interface

 Points

ALL

The following tables show the DRAM interfaces supported by the target MPU.

Table 4.2 Supported DRAM

MPU		Type	Maximum Memory Size	Speed (Mbps)	Maximum Number of Ranks
RZ/G2L RZ/G2LC RZ/V2L RZ/G2UL RZ/Five RZ/A3UL		DDR4	4 GB	1333 to 1600	2
		DDR3L		800 to 1333	
		LPDDR4	1 GB	1600	1
		DDR4	4 GB		
	15 mm PKG	LPDDR4	8 GB (Dual rank)	2133 to 3200	2
		LPDDR4X	4 GB (Single rank)		
RZ/G3E	21 mm PKG	LPDDR4/4X	4 GB (Single rank)	2133 to 3200	1
RZ/A3M		DDR3L	128 MB (internal)	1600	1

4.2.2 PCB Verification Guide

 Points

G2L

G2LC

V2L

G2UL

Five

A3UL

G3S

G3E

The target devices have guidelines for performing SI verification, timing verification, and PI verification for DDR circuit and pattern design. The PCB design guidelines describe design examples of evaluation board kits.

Table 4.3 PCB Verification Guidelines for DRAM Interface Design

MPU	Guideline
RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL	<ul style="list-style-type: none">PCB verification guide for DDR4/DDR3LPCB design guideline for DDR4/DDR3L
RZ/G3S	<ul style="list-style-type: none">PCB verification guide for LPDDR4/DDR4PCB design guideline for LPDDR4/DDR4
RZ/G3E	<ul style="list-style-type: none">PCB verification guide for LPDDR4/LPDDR4XPCB design guideline for LPDDR4/LPDDR4X

4.2.3 Model Number of a DRAM for Simulation

 Points

G2L

G2LC

V2L

G2UL

Five

A3UL

G3S


G3E

- Make sure the DRAM model number is correct.

Please make sure that the model number of the DRAM you are installing matches the model number of the DRAM you are using as a model in the pre-design simulation. If the model numbers do not match, the DRAM may not operate properly.

When installing multiple types of DRAMs with different capacities or from different manufacturers on the same PCB, please verify by simulation with all model numbers of DRAMs to be used according to the PCB verification guide. In addition, due to shrinking of silicon dies and changes in internal structure, model parameters may differ if the model number is different even for DRAMs of the same capacity from the same vendor. There is a risk in judging that there is no problem only by observing the waveform on the current PCB. Be sure to obtain a new model from the DRAM vendor and check the compatibility according to the PCB verification guide.

4.2.4 Topology for Connecting with the DRAM

 Points

G2L

G2LC

V2L

G2UL

Five

A3UL

G3S

G3E

- Make sure the topology you are using is correct.

The command and address connection between the MPU and the DRAM is only supported point-to-point on our reference board. It is shown in the figure below.

If you design with a different topology than our reference board, please refer to the PCB verification guide and run the simulation yourself. Even if you design with the same topology as our reference board, we strongly recommend that you run the simulation because the PCB structure, materials, and target DRAM are not exactly the same.

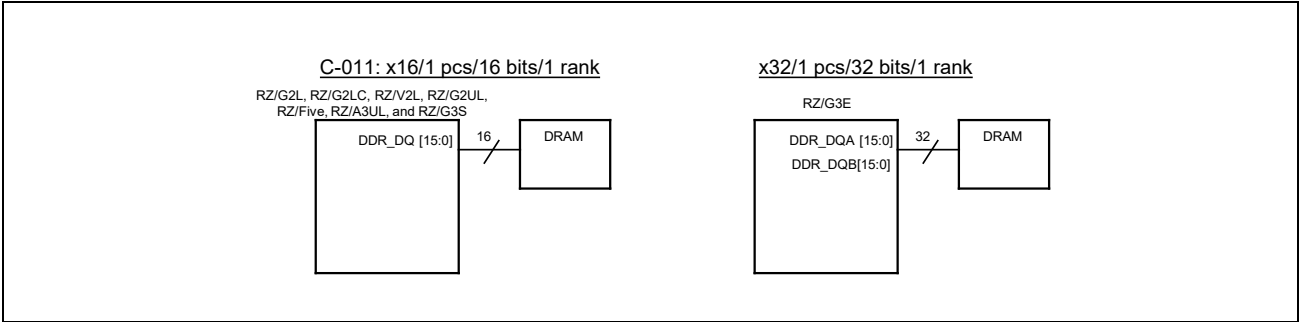


Figure 4.1 Topology Example of RZ/G2L, RZ/G2UL, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, RZ/G3S, and RZ/G3E

4.2.5 DRAM Interface Circuits



G2L	G2LC	V2L	G2UL
Five	A3UL	G3S	G3E

- Make sure the DRAM interface circuit constants are correct.


The DRAM interface circuit constants are listed in our PCB verification guide, so please refer to the latest guidelines to make sure the circuit constants are correct. The following is a general guideline for the example constants, but please note that the corrective action may differ depending on the board.

Constant examples

- Differential signal (CLK, DQS) termination handling
- Address/command signal termination handling (Rs resistor)
- Address/command signal VTT termination handling
- RESET signal termination handling (Rs resistor, pull-up resistor)
- VREF generation circuit
- ZQ pin handling

and so on

4.2.6 VREF Circuit for DDR3L

 Points

G2L	G2LC	V2L
G2UL	Five	A3UL

You should refer to the datasheet of the DRAM or contact its vendor for the appropriate VREF circuit for the DDR3L SDRAM side; however, we describe an example of the implementation for the evaluation board kits.

The VREF implementation has two ways, dividing resistors or dedicated power supply. The later way is implemented on our evaluation board kits. A 1.0-μF capacitors connected between the power supply and GND for stable voltage as shown in the following figure.

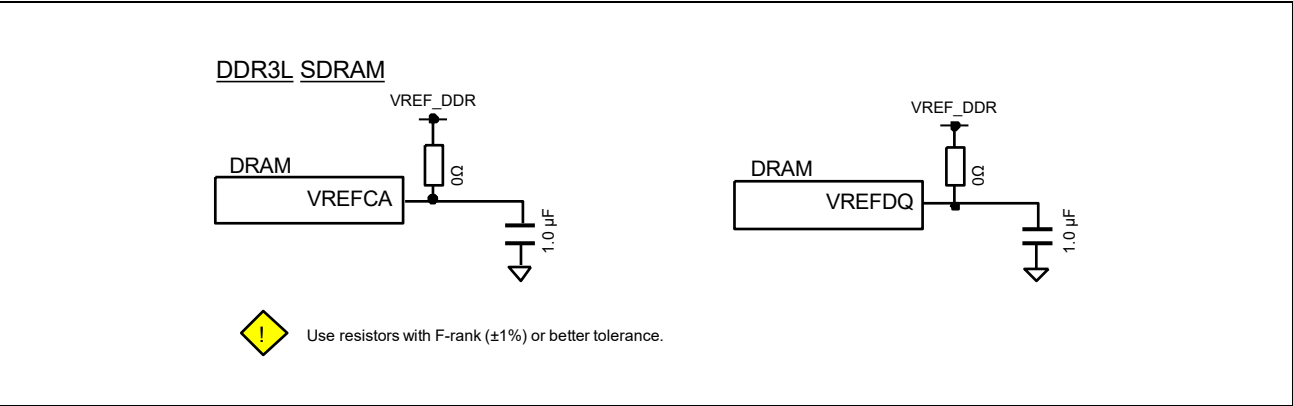



Figure 4.2 VREF Circuit for DDR3L

4.2.7 VREF Circuit for DDR4

 Points

G2L	G2LC	V2L	G2UL
Five	A3UL	G3S	

- For the VREF circuit on the DDR4 SDRAM side, contact the DRAM vendor and use an appropriate circuit configuration. On the evaluation board kits for the target devices except for G3S, each VREF are generated by the dedicated power supply, with 1.0-μF capacitors connected between the power supply and GND. For the evaluation board kit for G3S, each VREF are generated by resistor dividers with 1.0-μF capacitors connected in parallel between the power supply and GND for stabilization.

VREF generation by resistive division

- To generate VREF input from the VDD/GND pin nearest to each VREF input pin, the VREF voltages can be generated by using the VDD/GND in the presence of noise. The VREF generated by a VREF power supply IC, etc. near the DRAM power supply may be inferior in precision to VREF independently generated by resistive division in terms of the reference VDD/GND being near a DRAM power supply IC and at a distance from each VREF input pin and of the effect of the application of noise to the VREF wiring.
- The VREF generation circuit must be placed as close as possible to the DRAM VREF pin.
- Input leakage current on the VREF pin leads to a voltage shift that depends on the dividing resistor values.
- Current flows through the resistor during backup.

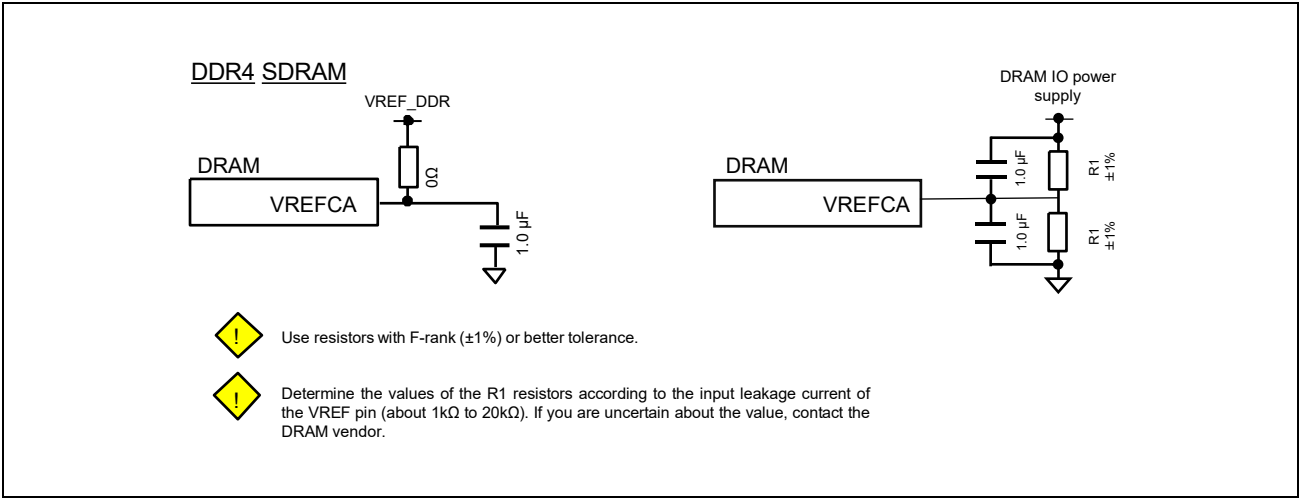



Figure 4.3 VREF Circuit for DDR4

4.2.8 ZQ Resistor (Value and Tolerance)

 Points

G2L	G2LC	V2L	G2UL
Five	A3UL	G3S	G3E

- Install ZQ resistors with the value specified in the PCB verification guide both on the SoC side and DRAM side.
- Select a resistor with a tolerance of $\pm 1\%$ or better and place it as close as possible to the pin.

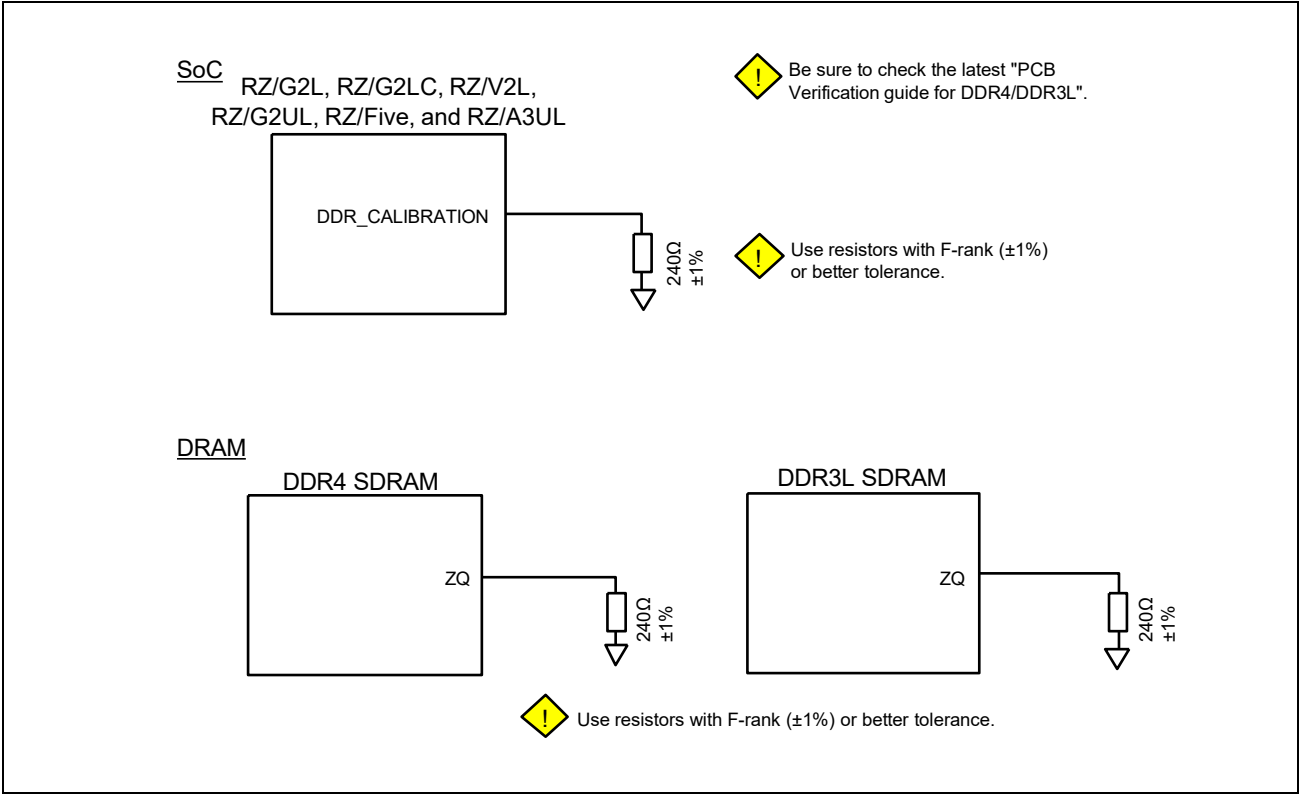


Figure 4.4(a) ZQ Resistor for DDR4 and DDR3L

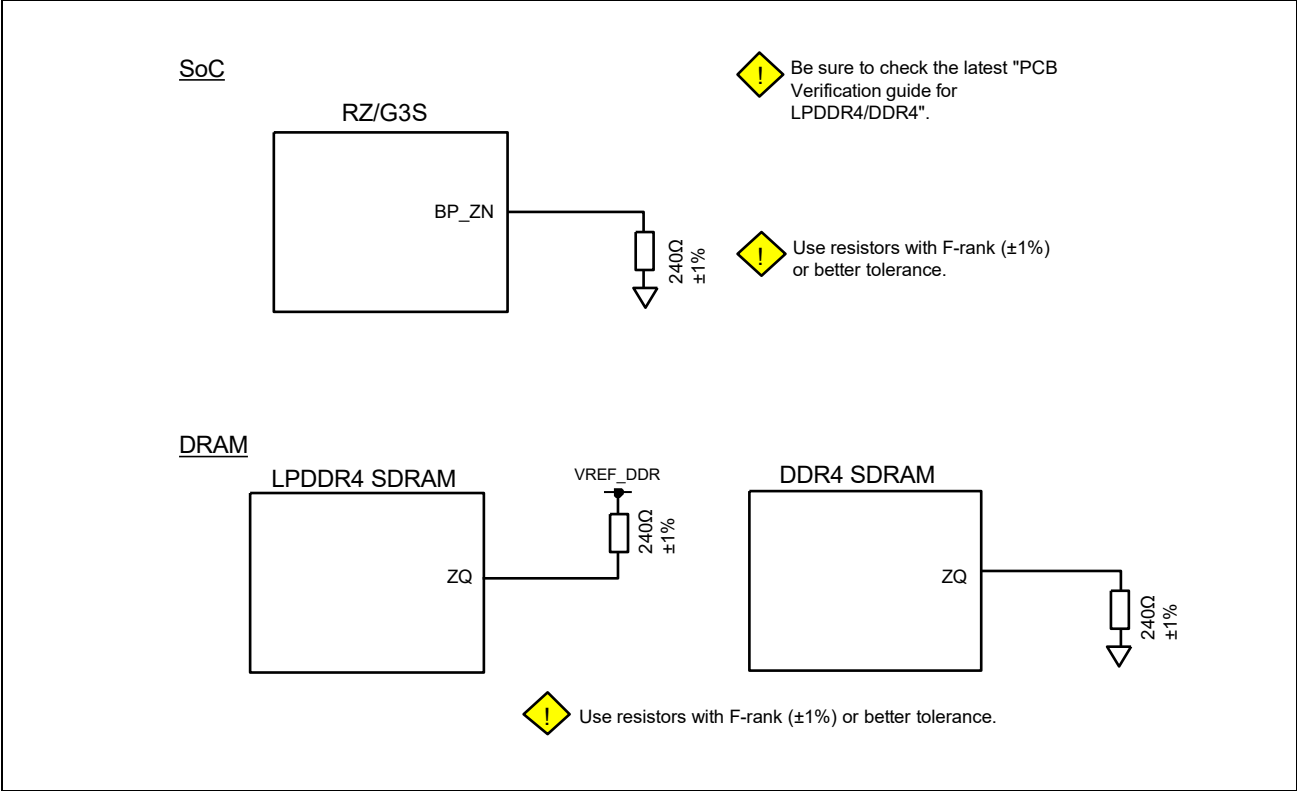


Figure 4.4(b) ZQ Resistor for DDR4 and LPDDR4

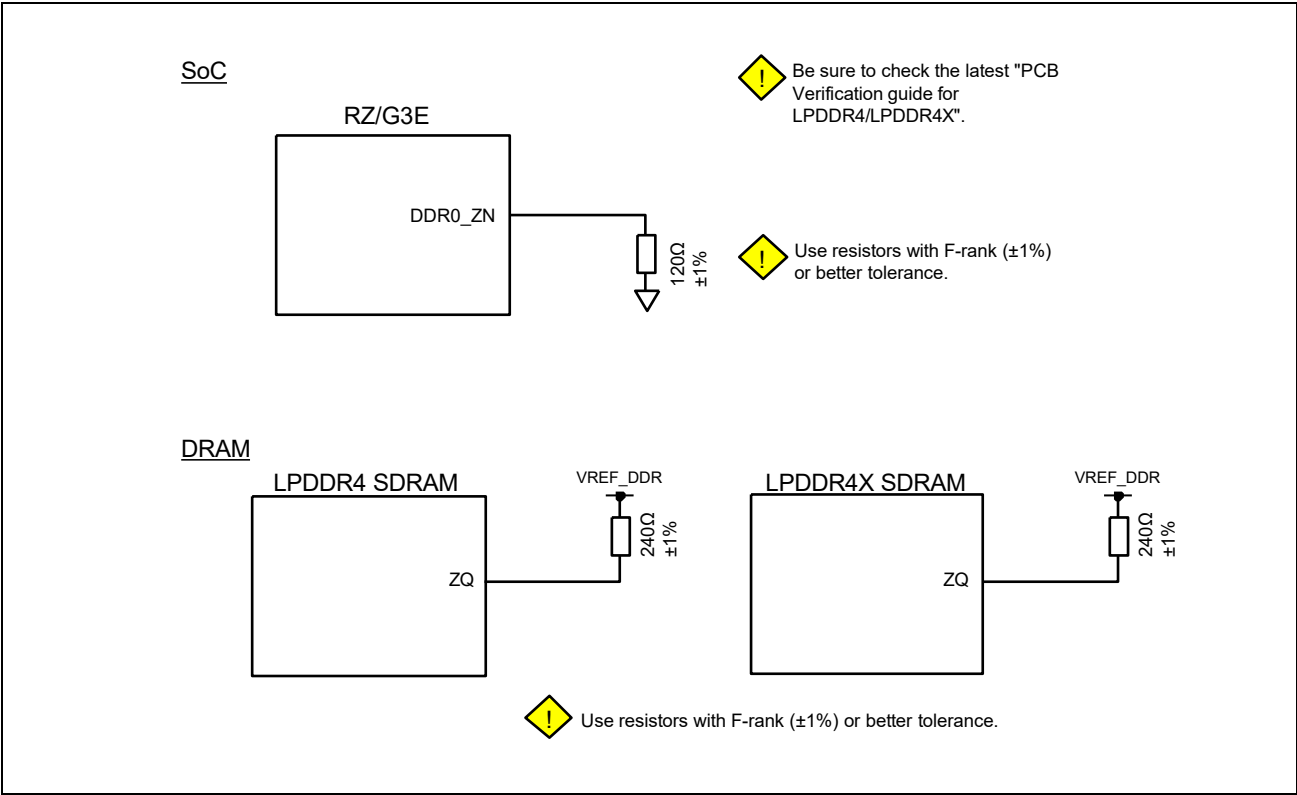


Figure 4.4(c) ZQ Resistor for LPDDR4X and LPDDR4

4.2.9 Pin Swapping for DDR3L



G2L	G2LC	V2L
G2UL	Five	A3UL

The MPU's DDR interface has a signal pin swapping function and has some restrictions.

- Make sure that the following restrictions are met:
 - Signals of DDR_A[15:0], DDR_BA[2:0], DDR_ODT[1:0], DDR_CS[1:0]#, DDR_RAS#, DDR_CAS#, DDR_WE# can be swapped.
 - During write leveling, the SoC side monitors changes in all DQ signals. Designers can switch DQ signals in the same byte lane at their own discretion.
 - The DQS/DQS#[1:0] signals can be swapped per differential pair. The positive or negative logic of the DQS signals cannot be swapped.
 - DM signals cannot be swapped with DQ signals.
 - The initialization software must contain information about pin swapping (a generation tool is provided).

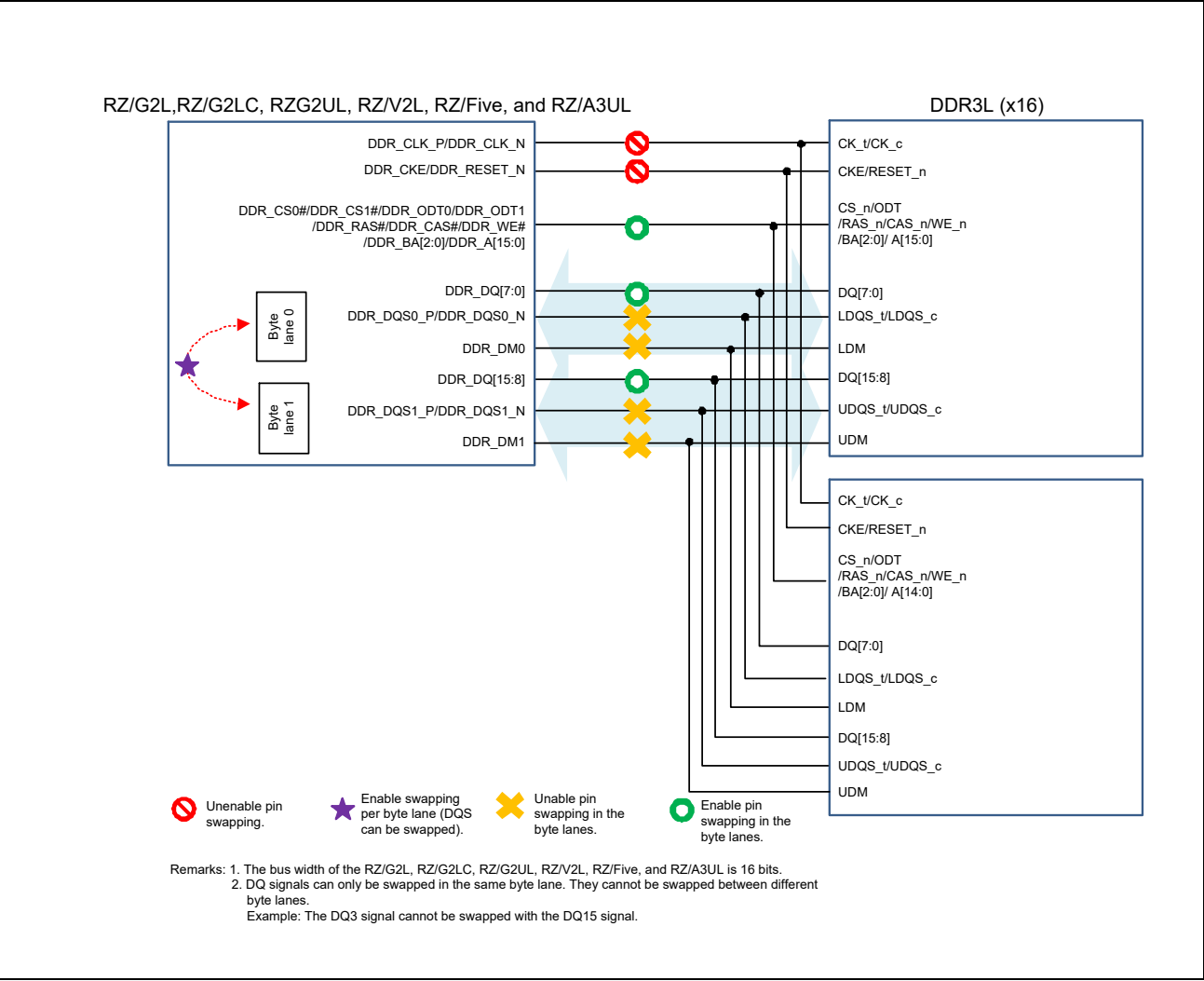
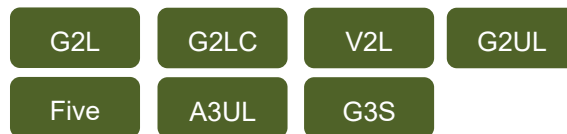
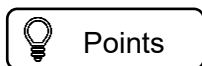


Figure 4.5 Pin Swapping between the MPU and DDR3L Interface

4.2.10 Pin Swapping for DDR4



The MPU's DDR interface has a signal pin swapping function and has some restrictions.

- Make sure that the following restrictions are met:
 - Address/command signals can be swapped.
 - During write leveling, the SoC side monitors changes in all DQ signals. Designers can switch DQ signals in the same byte lane at their own discretion.
 - DM signals cannot be swapped with DQ signals.
 - The initialization software must contain information about pin swapping (a generation tool is provided).

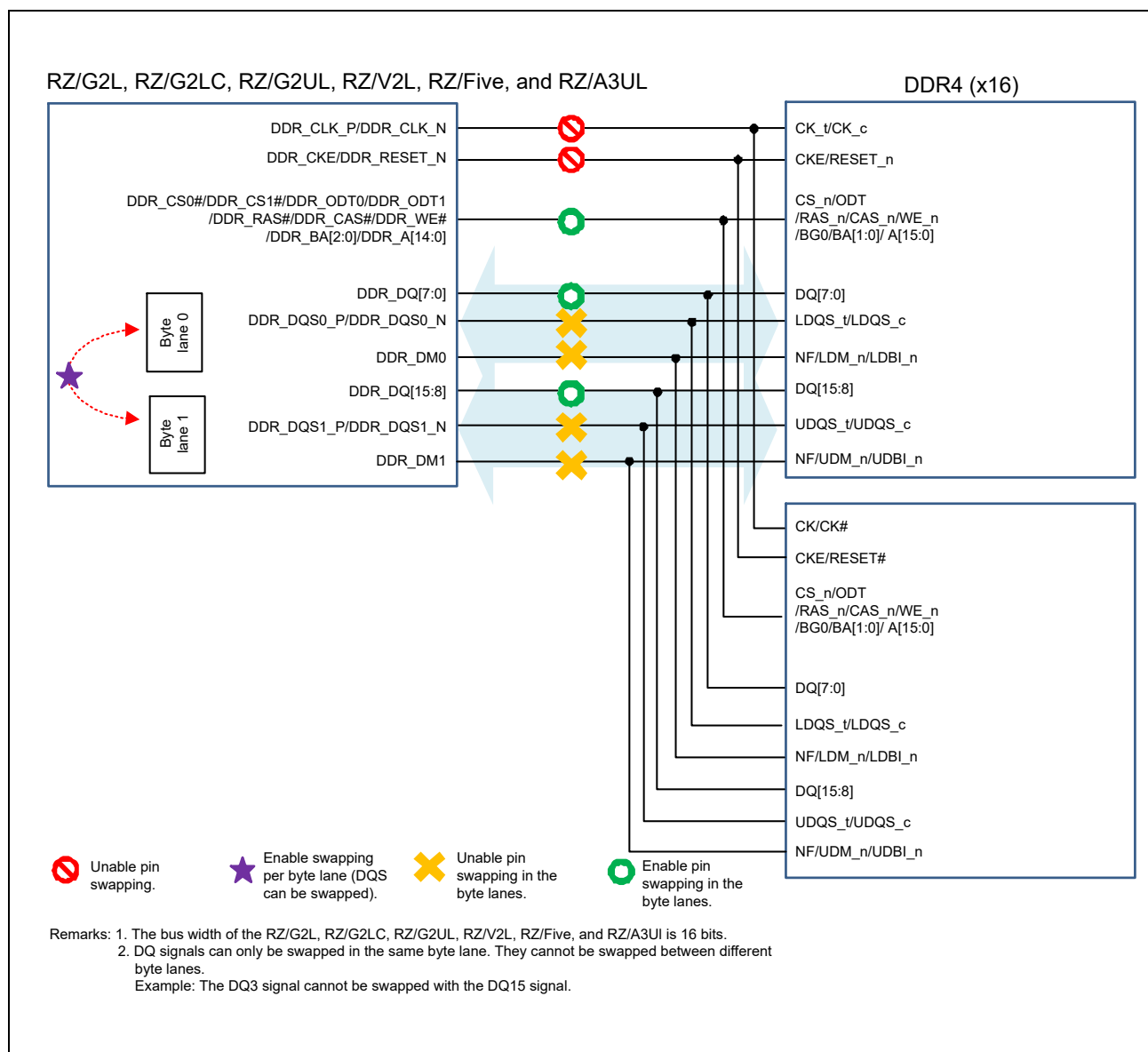


Figure 4.6(a) Pin Swapping between the MPU and Two DDR4 DRAMs

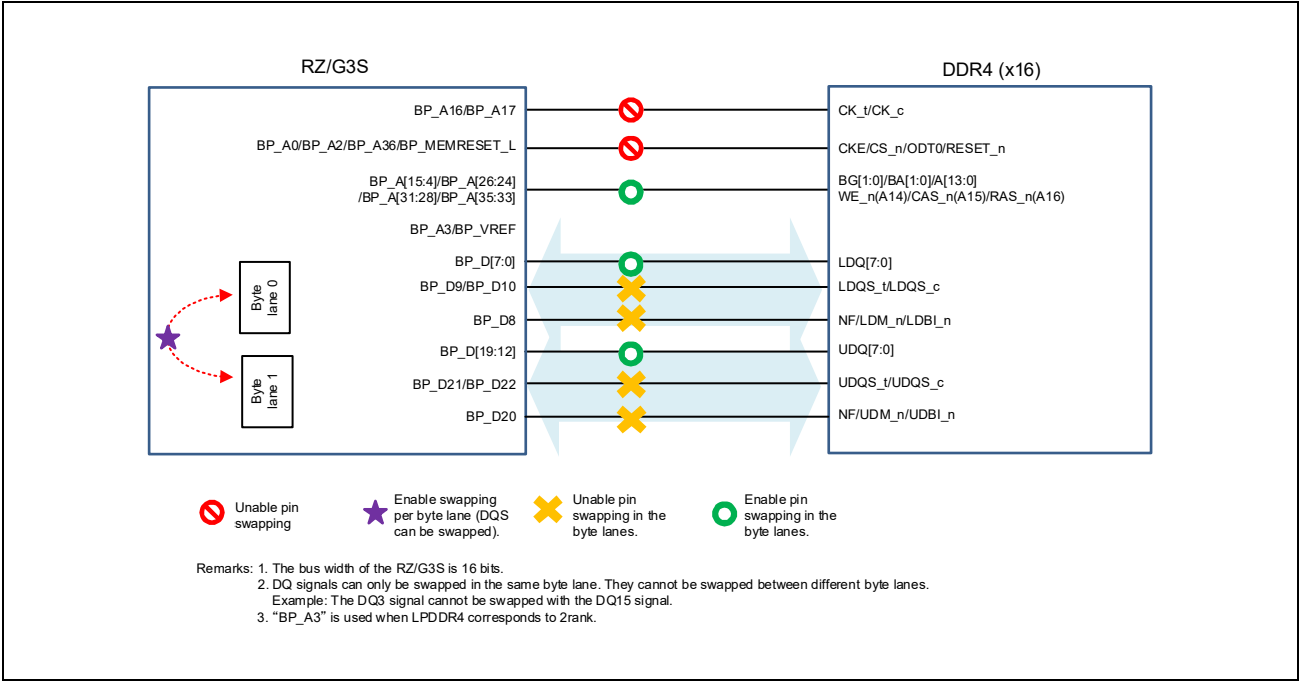


Figure 4.6(b) Pin Swapping between the RZ/G3S and the Single DDR4 DRAM

4.2.11 Pin Swapping for LPDDR4



Points

G3S

The MPU's DDR interface has a signal pin swapping function and has some restrictions.

- Make sure that the following restrictions are met:
 - Address signals CA[5:0] can be swapped within that range.
 - Control signals cannot be swapped.
 - The positive or negative logic of the DQS signals cannot be swapped.
 - DMI signals cannot be swapped with DQ signals.
 - The initialization software must contain information about pin swapping.

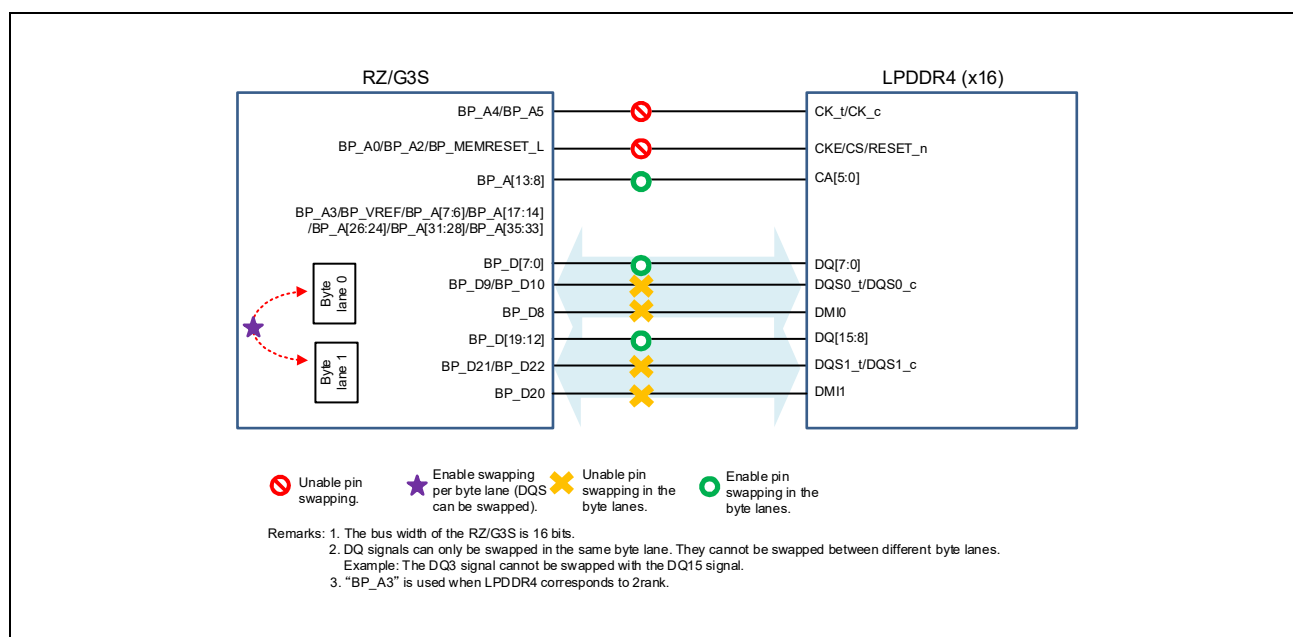
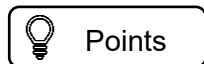


Figure 4.7 Pin Swapping between in the MPU and the LPDDR4 DRAM

4.2.12 Pin Swapping for LPDDR4/LPDDR4X



G3E

The MPU's DDR interface has a signal pin swapping function and has some restrictions.

- Make sure that the following restrictions are met:
 - Address/command signals can be swapped per rank. These signals can also be swapped per channel.
 - Control signals can be swapped per rank. These signals can be swapped per channel.
 - During write leveling, the SoC monitors changes for all data signals. The PCB designers can swap data signals in the same byte lanes such as byte lanes between lane 0 and lane 1 as needed. These signals are swappable per channel.
 - The positive or negative logic of the clock and data strobe signals cannot be swapped. These signals can be swapped per channel.
 - Swapping DQS differential signals are possible as long as it is byte-by-byte. These differential pairs can also be swapped per channel.
 - DMI signals cannot be swapped with DQ signals. These signals can be swapped per channel.
 - The initialization software must contain information about pin swapping.
 - For details, see section 3.4.3 in the RZ/G3E Group User's Manual: Hardware.

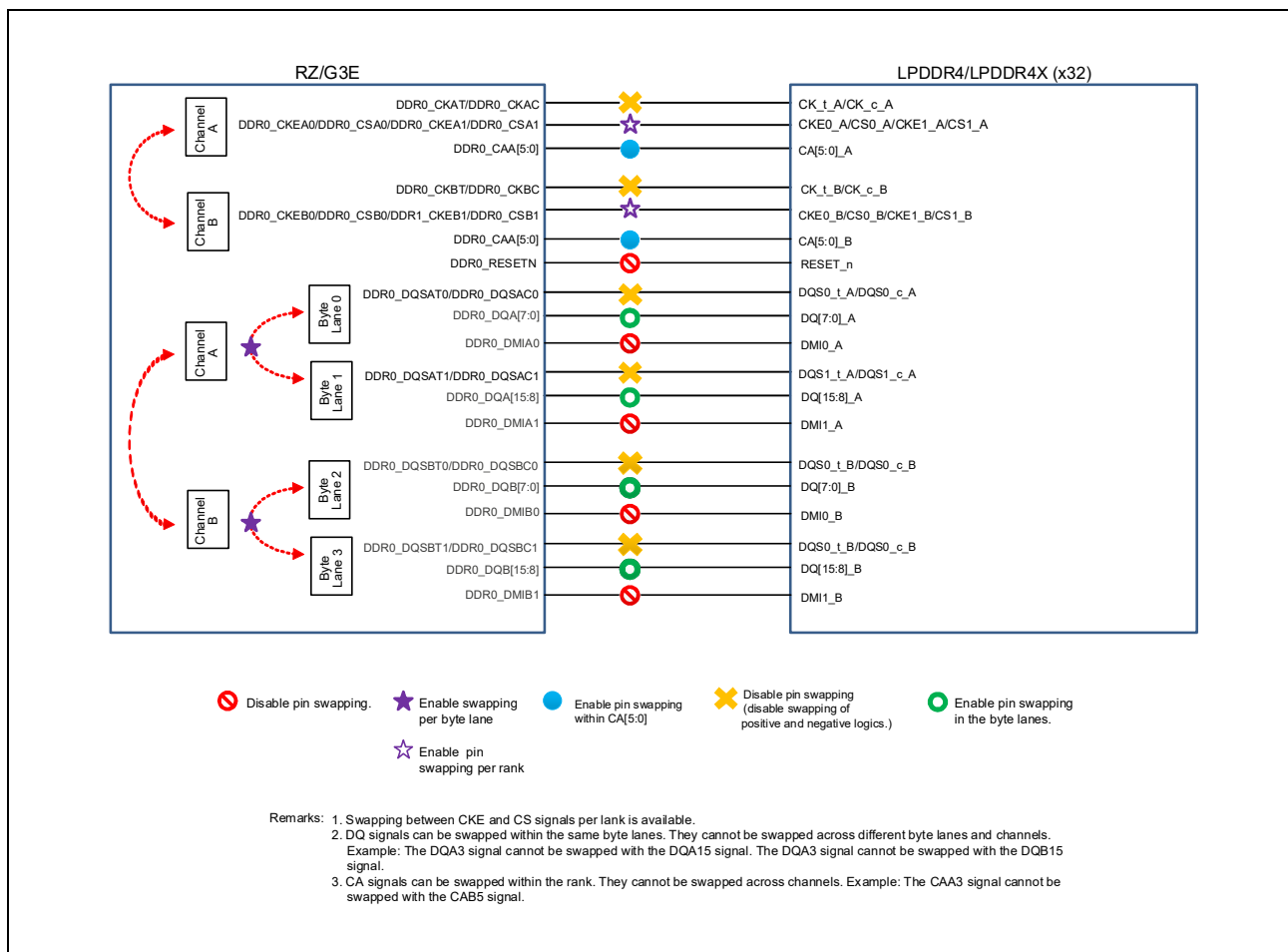
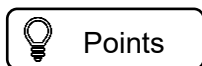


Figure 4.8 Pin Swapping between the MPU and the LPDDR4/LPDDR4X DRAM

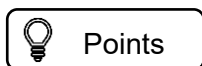
4.2.13 Power-on Sequence for DDR3L



G2L	G2LC	V2L
G2UL	Five	A3UL

- DDR3L SDRAM has VDDn (n = 0 to 9, typ.1.2 V) and VDDQn (n = 0 to 9, typ.1.2 V) as power supply pins. Please supply VDDn (n = 0 to 9) and VDDQn (n = 0 to 9) for DDR4 and DDR3L from the same power supply system.
- When DDR3L is connected to the target devices and both the power supplies are shared with the target devices, the power supply should be adjusted for the power supply interface of the DDR3L SDRAM.
- Please refer to JEDEC (JESD79-3F and JESD79-3-1A.01) for more information on power-on order restrictions.

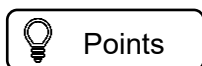
4.2.14 Power-on Sequence for DDR4



G2L	G2LC	V2L
G2UL	Five	A3UL

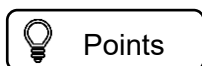
- DDR4 SDRAM has VDDn (n = 0 to 9, typ.1.2 V) and VDDQn (n = 0 to 9, typ.1.2 V) as power supply pins. Please supply VDDn (n = 0 to 9) and VDDQn (n = 0 to 9) for DDR4 and DDR3L from the same power supply system.
- When DDR4 is connected to the target devices and both the power supplies are shared with the target devices, the power supply should be adjusted for the power supply interface of the DDR4 SDRAM.
- Please refer to JEDEC (JESD79-4-1B and JESD79-4D) for more information on power-on order restrictions.

4.2.15 Power-on Sequence for LPDDR4



- LPDDR4 SDRAM has VDD1 (typ.1.8 V), VDDQ (typ.1.1 V) and VDD2 (typ.1.1 V) as power supply pins.
- The power-on sequence is defined for each power supply of LPDDR4.
- When LPDDR4 SDRAM is connected to the target device, and both the power supplies are shared with the target device, the power supply must be adjusted for the power supply interface of the LPDDR4 SDRAM.
- Please refer to JEDEC (JESD209-4) for more information on power-on order restrictions.

4.2.16 Power-on Sequence for LPDDR4X



- LPDDR4X SDRAM has VDD1 (typ.1.8 V), VDDQ (typ.0.6 V), and VDD2 (typ.1.1 V) as power supply pins.
- The power-on sequence is defined for each power supply of LPDDR4.
- When LPDDR4X SDRAM is connected to the target device, and both the power supplies are shared with the target device, the power supply must be adjusted for the power supply interface of the LPDDR4X SDRAM.
- Please refer to JEDEC (JESD209-4-1) for more information on power-on order restrictions.

4.2.17 VREF, DDR_CALIBRATION, ZQ , CS, and CLK for A3M



Points

A3M

- To generate VREF input from the VDD/GND pin nearest to each VREF input pin, the VREF voltages can be generated by using the VDD/GND in the presence of noise.
- The VREF generation circuit must be placed as close as possible to the VREF pin.
- Input leakage current on the VREF pin leads to a voltage shift that depends on the dividing resistor values.
- Install the DDR_CALIBRATION and ZQ resistors with the values specified in the PCB verification guide to the pins.
- Select a resistor with a tolerance of $\pm 1\%$ or better and place it as close as possible to the DDR_CALIBRATION and ZQ pins.
- The CS pins of A3M, DDR_CS_SOC and DDR_CS_DRAM, are not for external DDR3L but for external resistor. The DDR_CS_SOC and DDR_CS_DRAM implementation is as follows.
- The CLK pins of A3M, DDR_CLK_P and DDR_CLK_N, are also not for external DDR3L but for external capacitor and resistor. The DDR_CLK_P and DDR_CLK_N implementation is as follows.

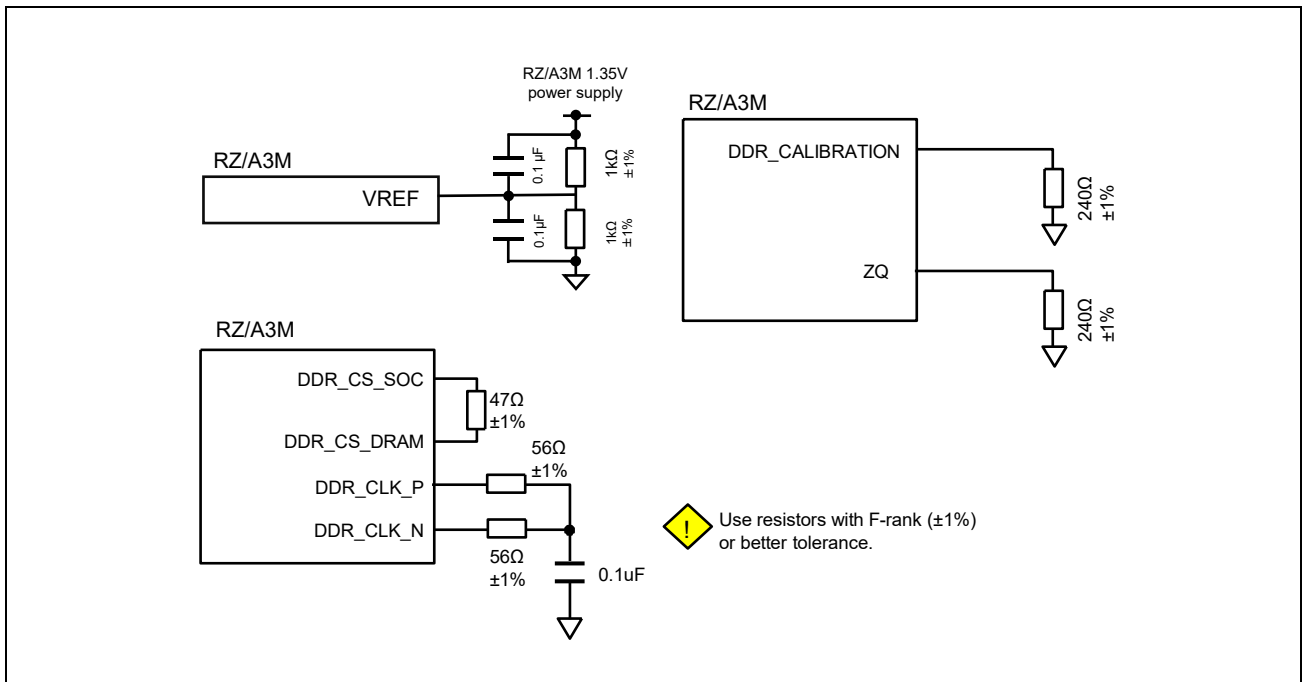


Figure 4.9 DDR VREF, CS, and CLK Circuit for A3M

4.3 Resistor and Capacitor



Points

ALL

- Follow the guidelines for selecting bypass capacitors. High-speed interfaces have dedicated power pins, and the High-Speed Interface Design Guidelines provide recommended capacitance values for bypass capacitors for power pins.
- As with power supply decoupling, place small-capacity bypass capacitors close to the MPU's power supply pins.
- Resistors used as current references may specify not only resistance values but also accuracy and temperature coefficients, so follow the design guidelines.

4.4 Clock

- The guidelines provide requirements for external clock input, so follow the guidelines for designing. A spread-spectrum clock (SSC) cannot be connected as the external clock.
- Make sure that a clock is not input before the power of the MPU is turned on.

4.5 PCIe

4.5.1 AC Coupling Capacitor

 Points

G3S

G3E

- Make sure the transmitter has a coupling capacitor installed.

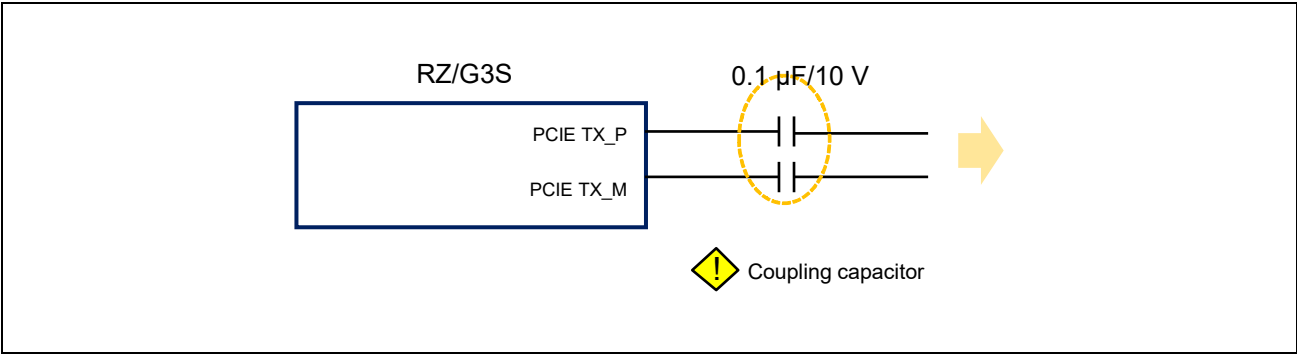


Figure 4.10(a) Coupling Capacitor at the Transmitting End for the PCIe

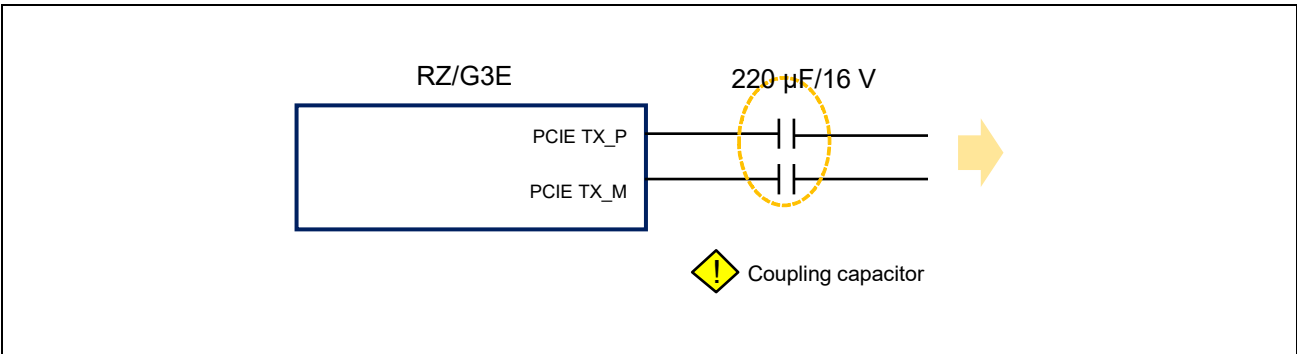


Figure 4.10(b) Coupling Capacitor at the Transmitting End for the PCIe

4.5.2 Clock

- Make sure you provide an external clock for PCIe. PCIe requires an external clock.

4.6 Instructions in schematic for PCB Layout



ALL

The guideline provides recommendations and restrictions for wiring patterns. We recommend including indications in the circuit diagram to give pattern designers a secure understanding of how recommendations and restrictions in the guidelines have been applied.

For general reference information on PCB pattern design, see **section 6, PCB Layout Design** in this guideline.

4.7 Observing High-Speed Serial Interface Signals

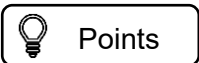


Points

ALL

- Note that installation of an observation pad on high-speed serial signal wiring may cause degradation in the signal quality.
 - Unnecessary stubs are constructed to set observation points.
 - Wiring runs that can only be arranged in the inner layer are brought out to the surface layer to set observation points on the surface layer.
 - Setting observation points for differential signals may lead to the symmetry of the differential wiring collapsing.
- The possibility of signal degradation increases with the signal speed, due to the addition of observation circuits. In order to improve the design quality, avoiding the unjustifiable setting of observation points is also necessary.
- High-speed signals might be distorted due to ISI or reflection deriving from observation points. In such cases, ideal waveforms such as are shown in the documents for reference might not be observed.
- In cases such as the above, you must proceed with advanced simulation of the intended observation points and the input circuits of the observation equipment by using the S parameter of the wiring and confirm the suitability by using the observation point movement function of the observation equipment.

4.8 Disturbance Noises and Static Electricity



- For interfaces such as USB2.0, that can be hot-plugged or connected to external devices, insert components for countermeasures against static electricity and external common mode noise.
- Dedicated components that can handle the signal level and signal frequency of each of the interfaces and components with noise filters having an ESD protection function are also available. Select components by reference to the circuit diagram of the evaluation board kits.

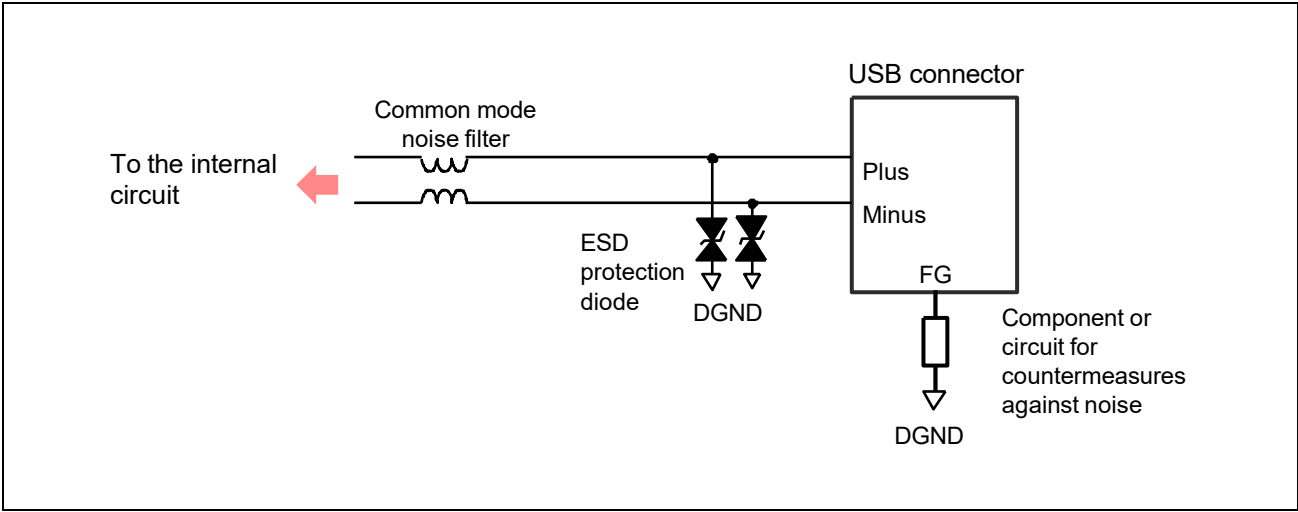


Figure 4.11 Example of Measures Against Disturbance Noises and Static Electricity

4.9 USB

4.9.1 Overcurrent or VBUS Input



Points

ALL

- When the overcurrent inputs are used, the input signal level should be 3.3 V. On the other hand, when a USB host is used but the overcurrent inputs are not used, these pins should be pulled up as the overcurrent interrupt from the VBUS controller may not be disabled.
- While the power supply to the MPU is turned off, the overcurrent input should not be the high level.
- When the VBUS input is used, connect it to the MPU through external dividing resistors with a value of $1\text{k}\Omega \pm 1\%$ and $1.8\text{k}\Omega \pm 1\%$.

The following figure shows a design example on the EVK; however, please refer to the datasheet of the USB VBUS control IC to be used.

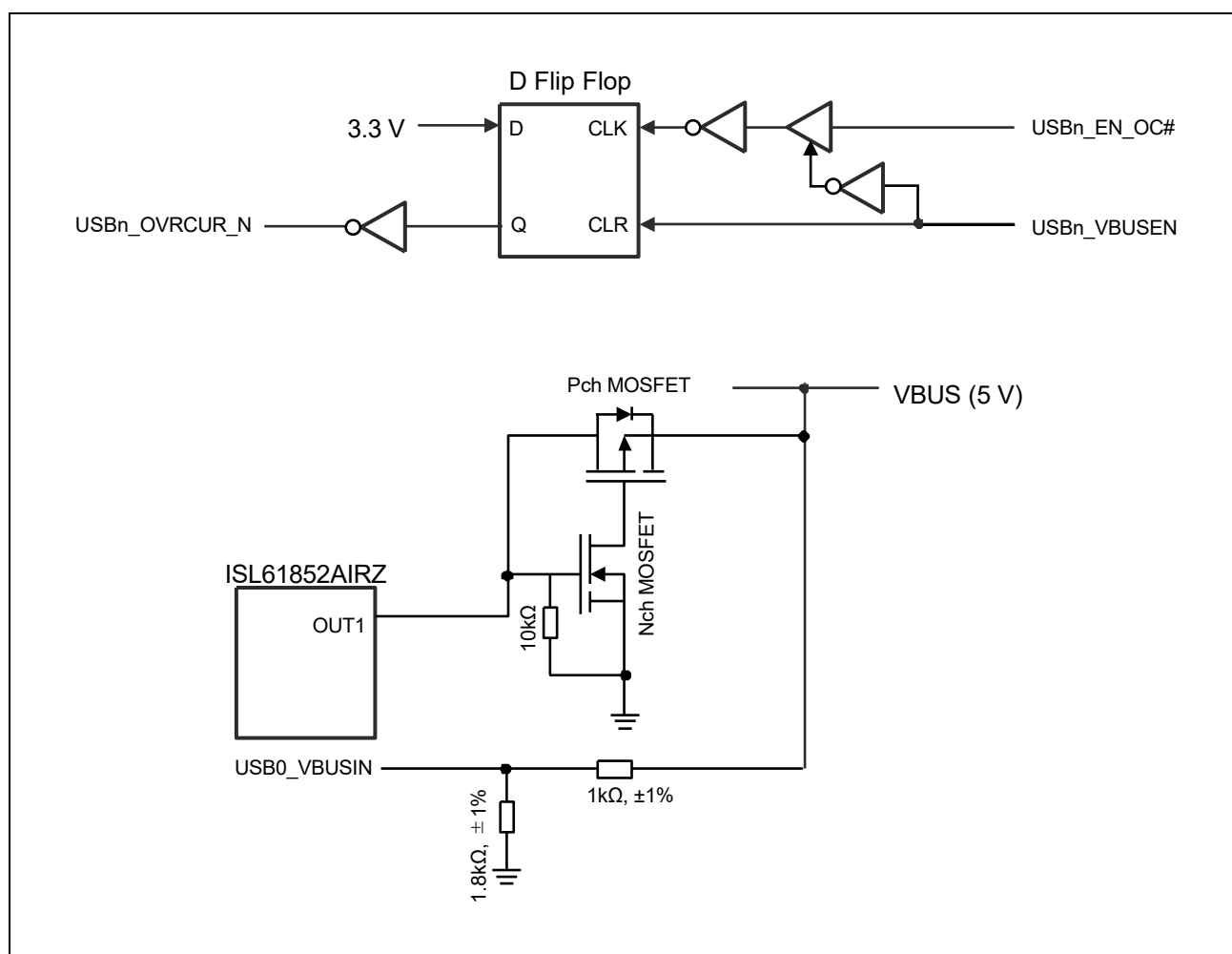


Figure 4.12 Overcurrent or VBUS Input

4.9.2 VBUS Enable



ALL

- Select an USB VBUS controller IC with an active-high EN input.

The VBUS enable signal of the USB interface is assumed as active high. And during a hardware reset (PRST# is low), the VBUS enable pin is high impedance. Examples of implementation are seen on our EVK. Please refer to their schematics and also refer to the datasheet of the USB VBUS controller IC.

4.9.3 USB 3.0



G3E

- USB 3.0 interface requires coupling at the transmitting end.

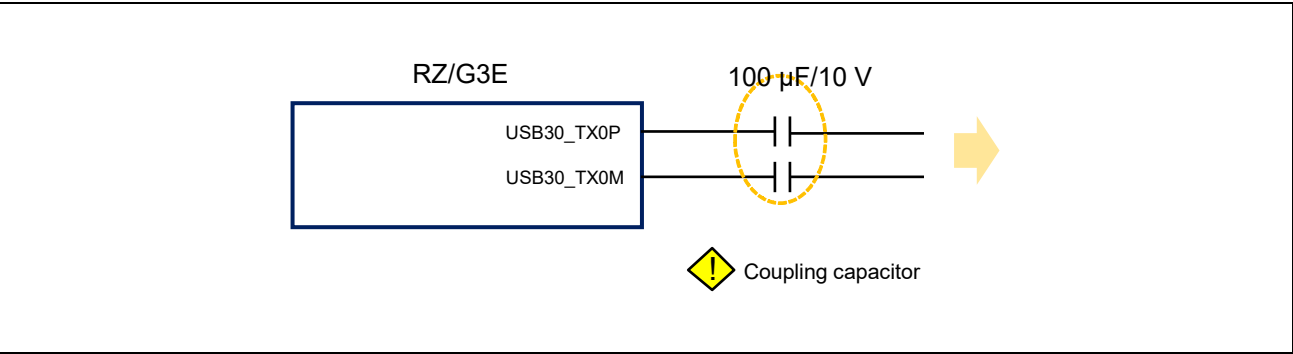
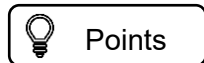


Figure 4.13 Coupling at the Transmitting End for USB 3.0

5. Others

5.1 Unused Pins



G2L

G2LC

V2L

- If there are unused function pins, handle these pins in accord with the statements on the handling of unused pins in the hardware manual.
- Please connect to GND via 1- μ F capacitor about the terminal processing of ABG_NCP_OUT.
- Even if you do not use all the functions, be sure to turn on the relevant power supplies.

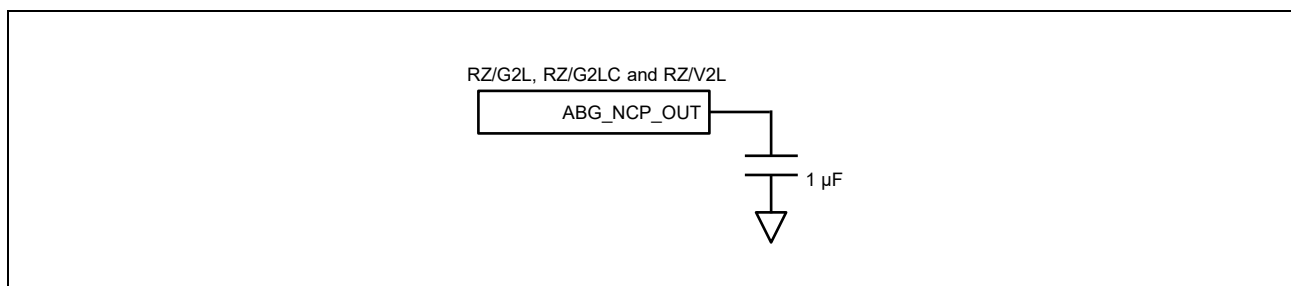
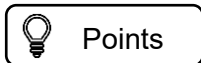


Figure 5.1 Terminal Processing of ABG_NCP_OUT

Documents for Reference

- RZ/G2L Group, RZ/G2LC Group User's Manual: Hardware
- RZ/V2L Group User's Manual: Hardware
- Lists of pin functions for RZ/G2L, RZ/G2LC, and RZ/V2L

5.2 NC pins



G2UL

Five

- Check how to treat NC pins. Please refer to the pin function list of the MPU.

In general, a pin being labeled non-connection (NC) means that the pin is not connected to the silicon die inside the MPU. NC pins do not generally need to be connected to anything, but some products may specify recommended pin treatments, such as connecting to GND or a power supply. Therefore, even if a pin is marked NC, be sure to check whether the recommended pin treatment is listed in the technical documentation for each IC. If the treatment method is not listed, we recommend that you contact the chip vendor. Similarly, be careful with LSI test pins and internal regulator output terminals.

5.3 Countermeasures against Overshoots and Undershoots



Points

ALL

- Larger than expected signal overshoots and undershoots must be prevented from causing the device ratings to be exceeded.
- A common method of doing so is to insert damping resistors near the signal outputting ends before determining the necessity and, if one is required, value of the resistor through evaluation. However, in such cases, you must pay attention to the following points.
 - The placement of damping resistors increases the number of parts near the MPU and peripheral devices, significantly affecting the placement of other important parts.
 - The connection of damping resistors necessitates the movement of signals to the surface layer. As a result, via holes and through holes significantly affect the properties of the wiring.
- When inserting a damping resistor to prevent overshooting and undershooting, carefully determine their necessity rather than inserting them unnecessarily.
 - Obtain IBIS models of the buffers, simulate typical transmission paths such as the longest one and shortest one, and estimate the possible amounts of overshoot and undershoot in advance.
 - Reduce the amounts of overshoot and undershoot by bringing the wiring layer (surface layer/inner layer) and wiring width close to the output impedance of the buffer.
 - Check if the driving ability of the output buffers is adjustable or can be set.
 - Apply impedance matching with parallel termination at the receiving ends instead of inserting damping resistors.

Documents for Reference

- Hardware user's manuals for individual target devices
- Lists of pin functions for individual target devices

5.4 Level Shifting



Points

ALL

- Some types of IO of the target device such as SD/MMC and QSPI allow two power supply voltages. The IO type of Gigabit Ethernet allows three power supply voltages.
- When the signal voltage differs between the MPU and a peripheral device, level shifters should be used and pay attention to the following points.
 - Is the IC to be used voltage tolerant?
 - Does the high-level voltage of signals and the VIH of the IC raise a problem?
 - Does the IC operate at a speed sufficient for the operating frequency of the signals?
- Pay attention to the power supply and output enable of the IC used for level shifting so that the signals do not go to the high level while power for the target device is cut off.
- In order to prevent misuse and misconnection of signals before and after level shifting, we recommend using net names that include signal voltages on the circuit diagram.

Documents for Reference

- Hardware user's manuals for individual target devices
- Lists of pin functions for individual target devices

5.5 IO Characteristics between MPU and Connected Devices



Points

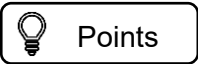
ALL

- When connecting the target device and a peripheral device, there will generally be no problem if the CMOS inputs and outputs have the same power supply voltage, even if the connections are direct at the DC level. If the AC timing also raises no problems, the connection will be problem-free. However, the DC specifications might differ slightly from device to device, so we recommended checking the AC and DC margins of both sides.
- The main external factors that may reduce the AC and DC level margins are as follows.
 - Minor differences in power supply voltage, such as where different power supply sources are used, or an FET switch is used
 - Superimposition of ground bounce and signal reflections due to simultaneous switching output (SSO) on rising and falling of the signals
 - Signal rounding due to excessive wiring length or load capacitance
 - Under-driving of the output buffers due to excessive resistive loads
 - Degradation in the signal quality due to crosstalk or ISI
- If there is a possibility that the AC and DC margins for the connected device are insufficient, consider measures such as inserting a pull-up resistor or buffer in the circuit design stage.

Documents for Reference

- Hardware user's manuals for individual target devices
- Circuit diagrams of individual evaluation board kits

5.6 IO Voltage Level Restriction for the PVDD182533 Power Domain



The IO voltage of the pins belonging to the PVDD182533_0 or the PVDD182533_1 power domains are selectable from 1.8 V, 2.5 V, and 3.3 V when used as Ethernet function; however, when used as other than Ethernet, the IO voltage should be 3.3 V. Please also refer to the pin function list.

Table 5.1 Supported IO Voltage Levels for the PVDD182533 Power Domain

	As Ethernet	As other than Ethernet
IO voltage usable	1.8 V, 2.5 V, 3.3 V	3.3 V

5.7 Conflict between Pull-Up and Pull-Down



Points

ALL

- Many devices including the target devices might have pull-up and down resistors. Although internal pulling up and down help to reduce the number of parts, conflicts may occur when devices are connected to each other, leading to unexpected problems.
- The following is a common case. Device A has a pull-up resistor and device B has a pull-down resistor. Connecting A and B leads to the signal potential becoming intermediate.

Cases

- An intermediate potential is produced because the internal pulling up and down compete against each other.
- The internal pulling up or down competes with the pulling down or up in an external circuit.
- When a device is turned off, pulling up in another device may apply a voltage exceeding the standard, and the power that should have been turned off does not become 0 V because of external pulling up or a device-protection diode.
- In particular, pay attention to pulling up and down for use in setting the mode of the target device.
- Check the data sheets and technical documentation of each device for details to avoid conflicts.
 - The presence of internal pulling up or down, values of the resistors used, and method of control (such as in terms of always being on, and pin and register settings)
 - Interface equivalent circuit including pulling up or down
 - Behavior in special cases such as during and immediately after a reset, etc.
- The pin function table of the target device describes the information and control of the internal pulling up and down, and the pull-up or -down resistor values are described in the electrical characteristics.

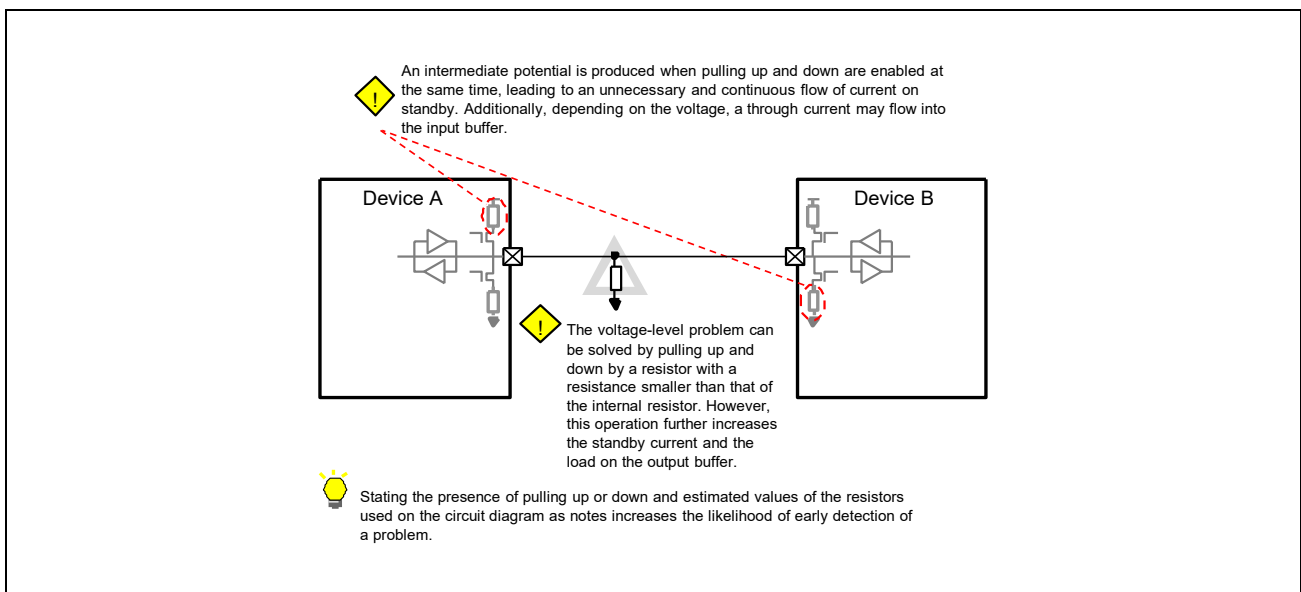


Figure 5.2 Conflict between Internal Pulling Up and Down

5.8 Relatively High-Speed Interfaces (about 10 to 100 MHz)



Points

ALL

We provide design guidelines for high-speed signal interfaces such as MIPI-CSI, MIPI DSI, and USB, but it does not specially provide those for relatively high-speed synchronous parallel interfaces (such as Parallel Input/Output, Ether MII, SD/MMC, and QSPI).

- When designing a relatively high-speed interface, we recommend that you observe the following general precautions:
 - Include wiring instructions, such as equal-length wiring, in the schematic diagram to avoid problems in the layout design.
 - Route all wiring on a single layer to prevent delay differences between layers. If possible, calculate the delay from a transmission simulation in advance and instruct the designer to design an equal delay pattern.
 - Leave sufficient wiring spacing to prevent crosstalk. If possible, the wiring spacing should be three times the distance to the reference layer.
- When using a flexible cable to connect to a peripheral device, be sure to provide a return path and provide a sufficient number of ground wiring to prevent crosstalk and unnecessary radiation.

5.9 Notes on Signal Connection



Points

ALL

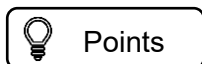
- Make sure that the CMOS input ports are not left open-circuit (Hi-Z).
 - If they are left open-circuit, a through current may continue to flow, leading to deterioration and destruction of elements.
 - Also pay attention to hidden open-circuit states of input ports, such as when a part or IC that is a destination for connection is not mounted.
- Confirm that output signals do not conflict between devices including the MPU.
 - If such conflict continues for a long time, elements may deteriorate or be destroyed.
 - Also, pay attention to hidden conflicts arising from special situations such as during a reset.
- Be careful when connecting ICs that operate under special conditions, such as ICs that operate with the power of an external USB bus even if the main power of the board is not on.
 - Do not drive high or pull up pins that do not have tolerance.
 - In the Renesas evaluation board kits, the USB-UART bridge IC is an LSI chip that partially operates with USB bus power.
- Be careful when using WDTOVR_PERROUT# terminal of RZ/G3S. When PRST# signal level is low, the pin condition of WDTOVR_PERROUT# terminal is Hi-Z, not the high level. So, an external pull-up resistor is required.

Remarks:

Technically, the pins of the target device that are capable of pulling up and down control remain open-circuit from the time the power is turned on until reset is released or until pulling up or down is enabled by the PFC settings, if there is no external component or IC that determines the signal level.

If the reset period is short and the PFC settings proceed quickly after startup, deterioration and destruction due to heat generated by the IO through current will not occur. If you do not need the LSI to perform any processing, we consider turning off the power to be normal. However, if there is a special circumstance, such as when it is necessary to leave the power on or have a longer reset period, use an external device for additional pin handling, although this will increase the number of components.

5.10 Interrupt Signals



ALL

- The MPU has interrupt inputs like the NMI and IRQs. Note that these interrupt inputs differ in the IO power supply they are supplied with, whether the IO buffer is a Schmitt trigger, and whether there is a built-in pull-up/pull-down or not.
- Also, the RZ/G2LC has IRQ0 to IRQ7, but IRQ2 and IRQ3 cannot be used, so be careful.

5.11 eMMC

5.11.1 Connection with eMMC



G2L	G2LC	V2L	G2UL
Five	A3UL	G3S	G3E

- Since the eMMC interface is a relatively high-speed parallel interface, we recommend that you perform SI simulation with the IBIS model.
- If you are concerned about overshooting or undershooting during eMMC boot, add a series damping resistor to the interface.
- When using an eMMC as a boot device, the output impedance should be 50Ω. So please design the capacitive load according to the electrical specification in the user's manual and the transmission line of the board to be 50Ω.

5.11.2 eMMC Interface Circuit



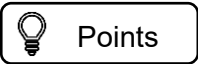
G2L	G2LC	V2L	G2UL
Five	A3UL	G3S	G3E

- Determine the pull-up resistor values for the CMD and DAT signals according to the operating voltage in reference to the recommended values provided in the eMMC standard documentation.
- Insert a series termination resistor (series resistor) for the CLK signal as necessary.
- We recommend that you confirm that the signal quality is free of problems by simulating transmission.
- When booting from an eMMC is used, eMMC must be reset before the start of booting up the CPU. *1

Note 1. Some eMMC devices may not activate reset pin function just after the factory shipping.

- Please refer to JEDEC(JESD84-B51) for more information.

5.12 Octa Memory Controller



A3UL

G3S

- When using an OctaFlash as boot memory, connect the QSPI_RESET# pin to the OctaFlash RESET# pin. An OctaFlash can be only connected to the Octa Memory Controller, not to the SPI Multi I/O Bus Controller.

An implementation example of an OctaFlash and controller connection is illustrated in following figure.

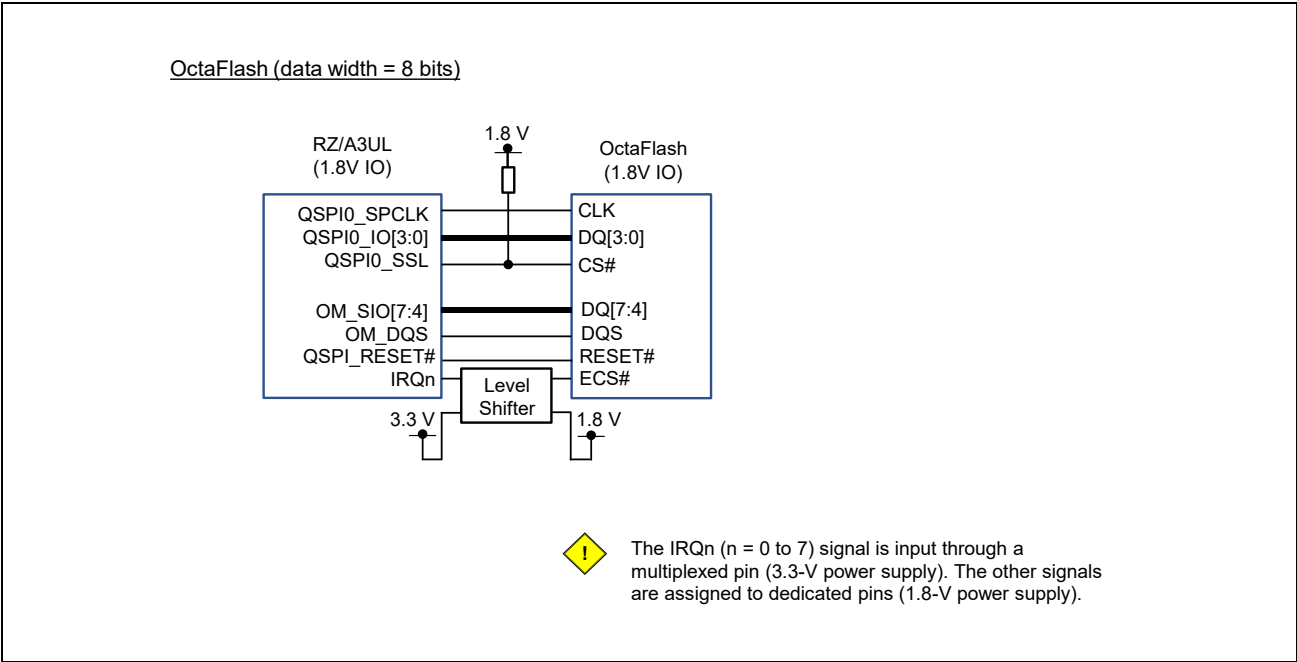


Figure 5.3 Connection to the OctaFlash

Also an example of an OctaRAM connection is illustrated in following figure.

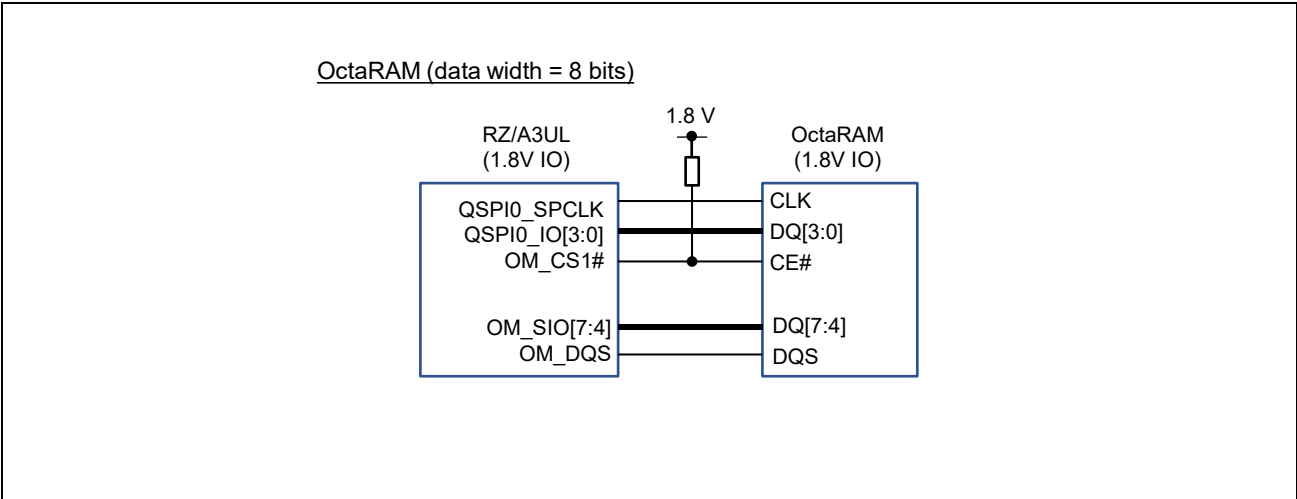


Figure 5.4 Connection to the OctaRAM

5.13 SPI

5.13.1 SPI Multi I/O Interface



Points

G2L	G2LC	V2L
G2UL	Five	A3UL
		A3M

- The SPI multi I/O interface consists of two internal QSPI interfaces; however, these two interfaces do not support independent operation.

When QSPI0 is used as the Single-SPI or Quad-SPI interface, QSPI1 cannot be used. Although connecting two units of Quad-SPI flash memory to QSPI0 and QSPI1 in parallel and using them as 8-bit width is possible, QSPI0 and QSPI1 cannot be used as two independent interfaces for Quad-SPI flash memory.

- The QSPI boot mode only supports QSPI0 interface. In order to use Octal SPI interface by combination of QSPI0 and 1, software should change configuration after boot.
- The SPI multi-I/O interface is a relatively high-speed interface. Although we do not have a specific guide, we recommend that you use equal-length wiring and perform a transmission simulation in advance to check that there are no problems with the signal timing or quality.

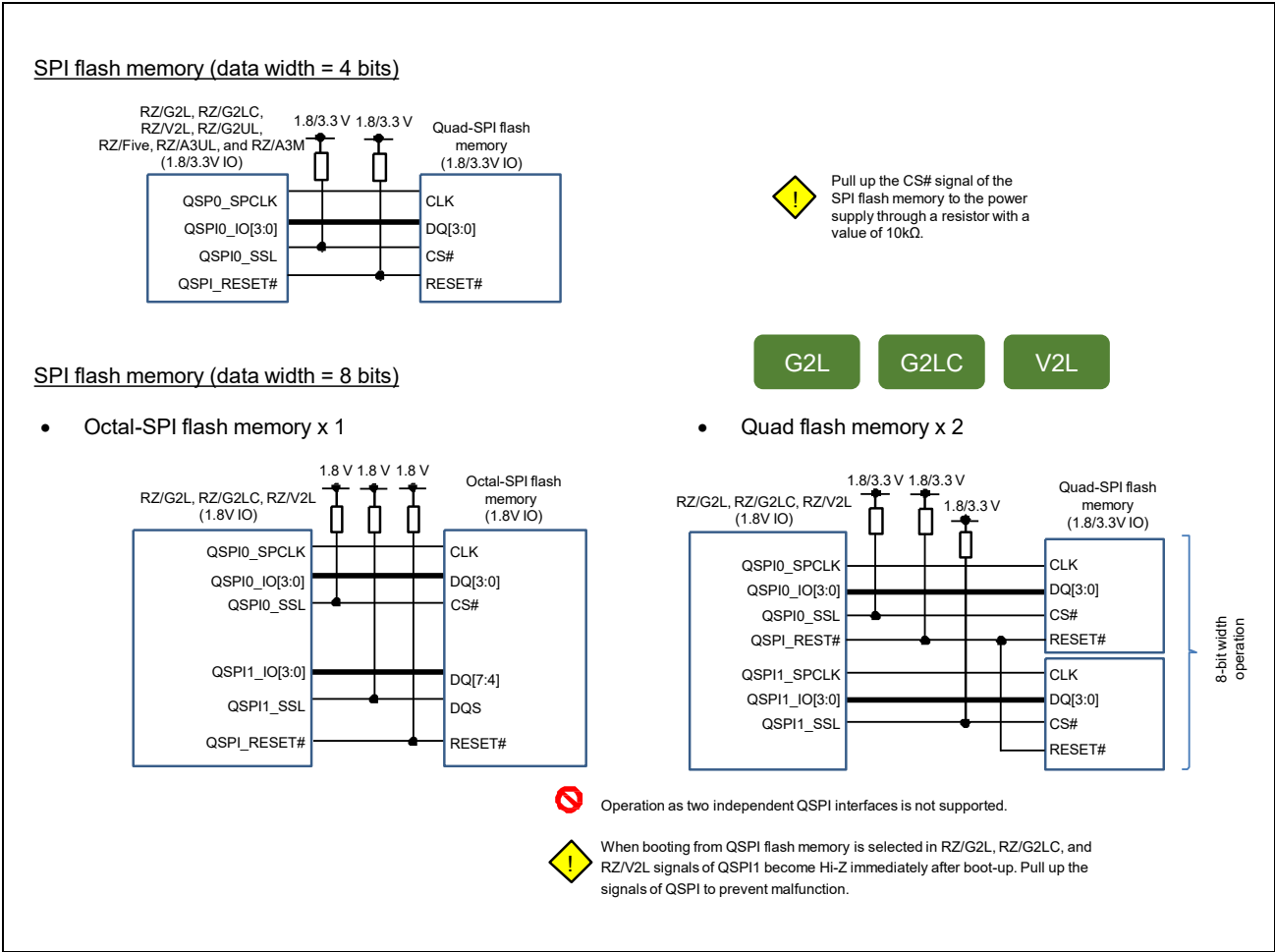


Figure 5.5 Connection of SPI Flash Memory

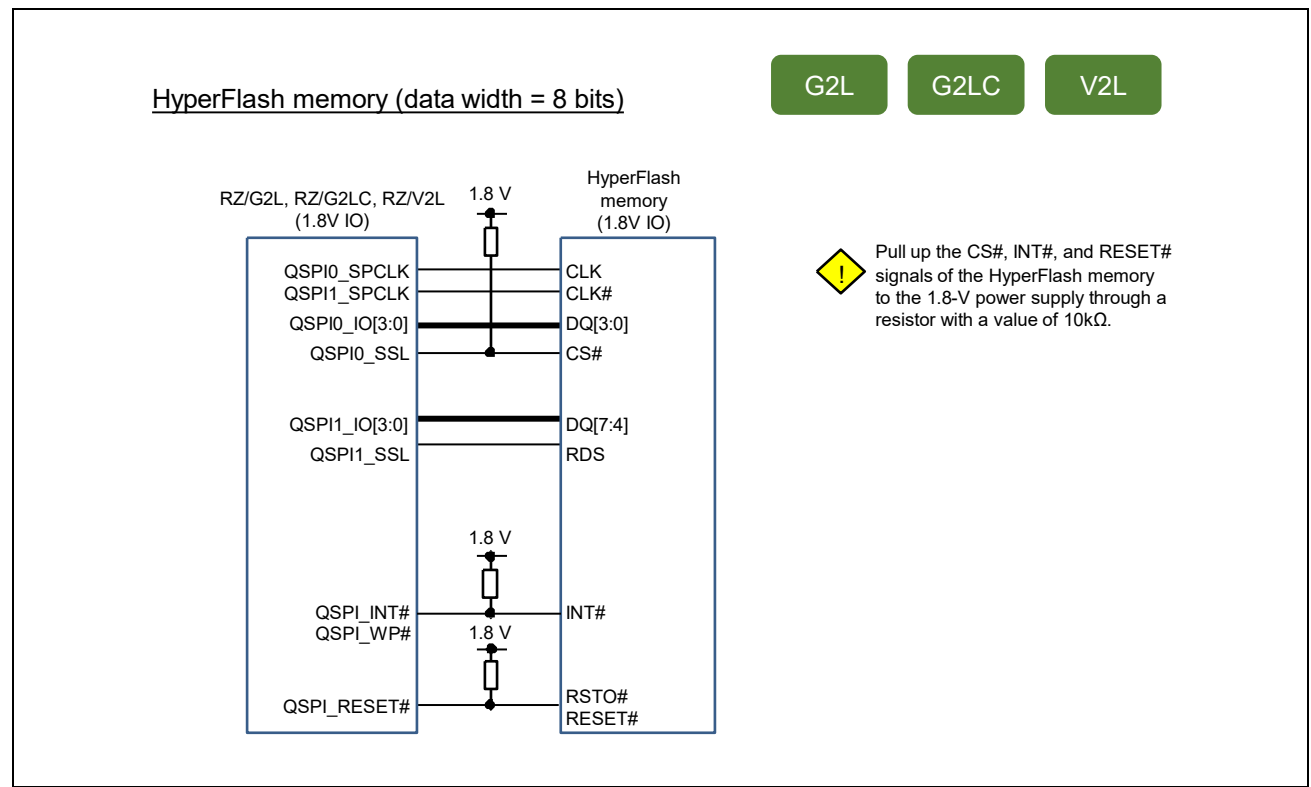


Figure 5.6 Connection of HyperFlash Memory

5.13.2 eXpanded Serial Peripheral Interface (xSPI)



Points

G3S

G3E

- The xSPI enables the direct connection of Quad/Octal-SPI flash memory and OctaRAM to the MPU.
 - Note that the RZ/G3E cannot be connected to OctaRAM.
- When two Quad-SPI flash memories are connected to the MPU, the two Quad-SPI flash memories operate exclusively of each other.
 - By default, CS1 does not have an address space. The address space of CS0 and CS1 can be set by registers in the SYSC section. When setting the address spaces of CS0 and CS1, overlapping addresses is prohibited.
- The xSPI is a relatively high-speed interface. Although we do not provide any guide in particular, we recommend that you confirm that the signal timing and quality are free of problems by providing instructions about equal-delay (equal-length) wiring or simulating transmission in advance.

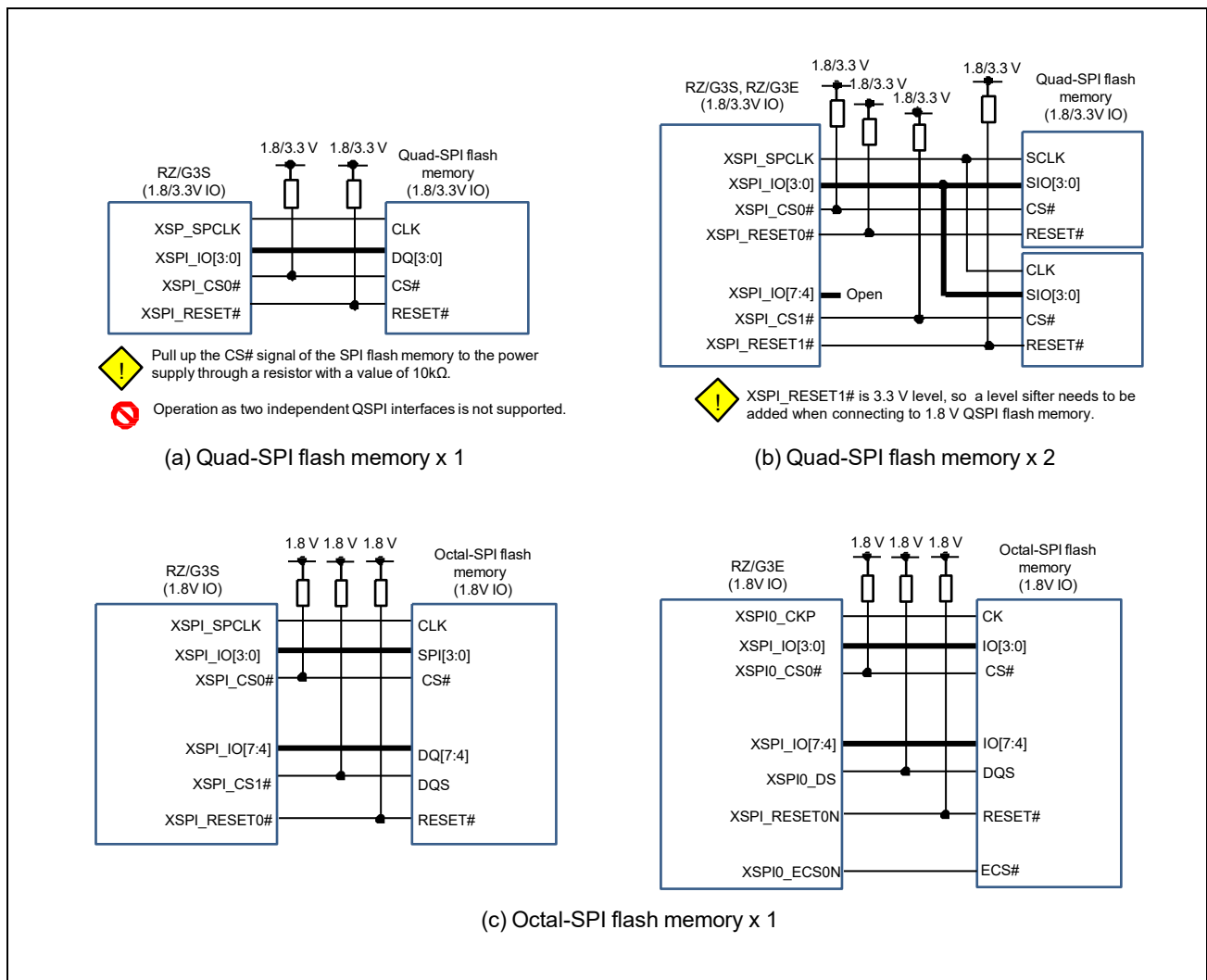


Figure 5.7 Connection of SPI Flash Memory

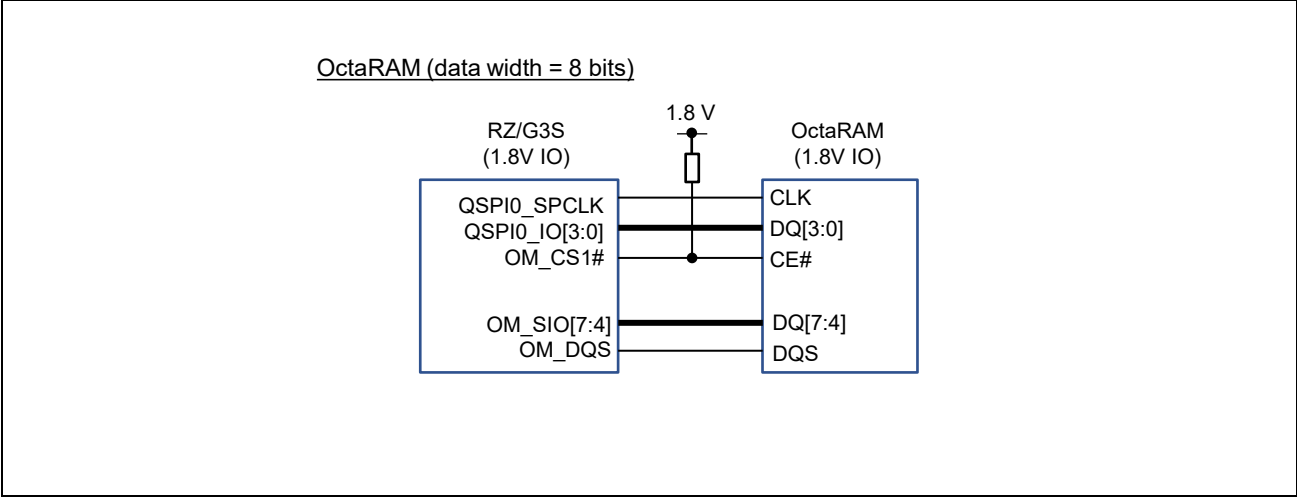


Figure 5.8 Connection of OctaRAM

5.13.3 Master and Slave



Points

ALL

- The SPI Multi I/O interface supports only master mode and the Renesas Serial Peripheral interface, RSPI, supports master and slave modes.
- When the RSPI is used in master mode, the SSL signal is fixed to the low level.
- When the RSPI is used in slave mode, the SCK input is not a Schmitt-trigger input. Therefore, pay attention to glitches and rounding of the clock waveform due to pin capacitances and wiring branches.
- When the RSPI is used in both master and slave modes, such as on a multi-master SPI bus, make sure that the two outputs do not become short-circuited.

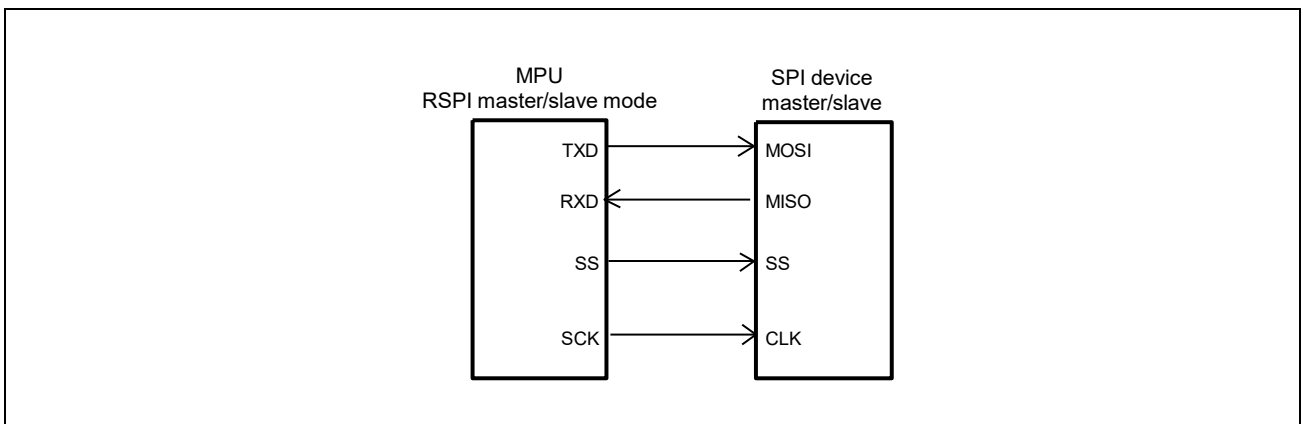


Figure 5.9 Connection of SPI and RSPI

Documents for Reference

- Hardware user's manuals for individual target devices
- Lists of pin functions for individual target devices
- Datasheets or technical documents for the individual peripheral devices

5.13.4 Selection of QSPI flash memory



Points

ALL

Using a QPSI flash memory with RESET pin is recommended.

When accessing over 16MB memory area, the following changes are needed.

- (1) change from 3-byte address access to 4-byte address access (enter 4-byte addressing, Address: B7h)
- (2) switch to a BANK other than the first 16MB (read extended address register, Address: C8h)

When a reset occurs after these changes, the SoC will be reset, but the flash memory will not be reset. Then changes on the flash memory will remain. The boot ROM code on the SoC will try to read the first 16MB of the flash memory with “3-byte address”; however, the flash memory cannot accept that request. Therefore, the SoC will fail to reboot.

With a QSPI flash memory less than 16MB capacity, this issue will not occur because the changes (1) and (2) for 4-byte address read are not needed.

Besides the software reset, the following events should be considered.

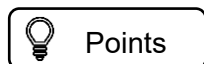
- A watchdog timer reset
- A physical reset button

If an over 16MB QSPI flash memory without RESET pin is used, it is needed to take some measures by hardware and/or software for this issue.

This is why using a QPSI flash memory with RESET pin is recommended.

5.14 SDHI

5.14.1 CD and WP Signals



ALL

The CD (card detect) and WP (write protect) input signals of the SDHI are 3.3V IO (3.3 V) signals.

- When pulling up these signals, be sure to use 3.3 V, and do not pull these signals up to the SD card power supply (SDn_PVDD).

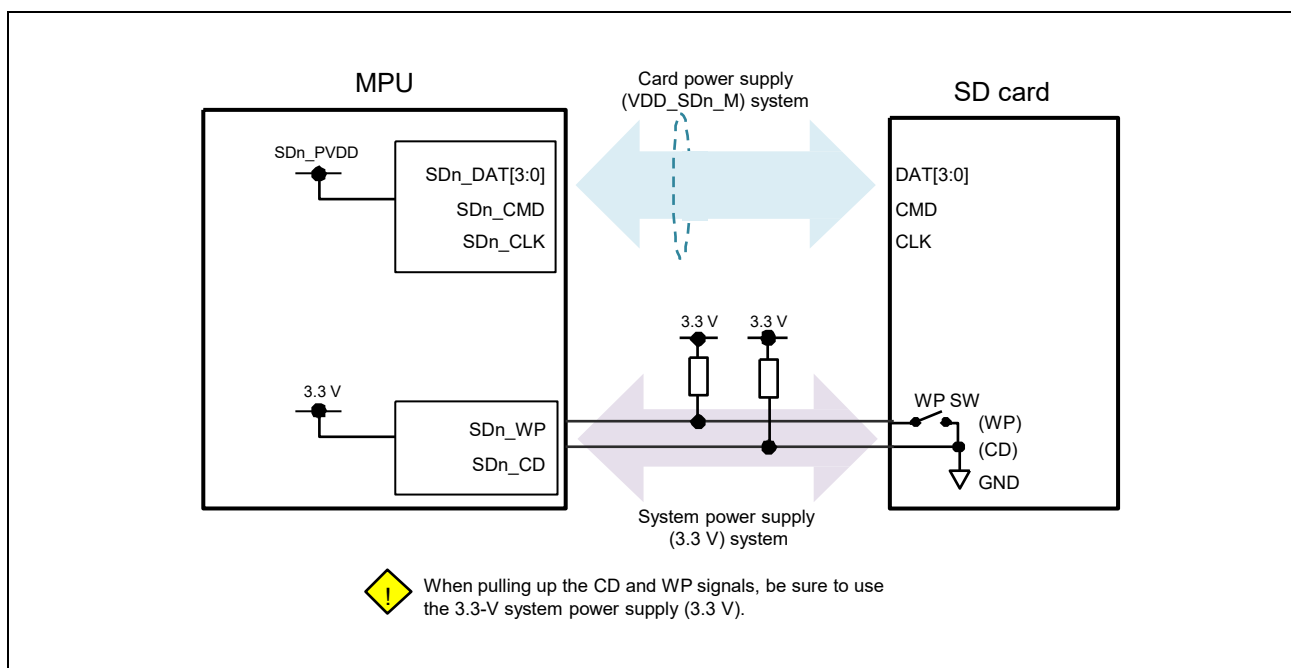


Figure 5.10 CD and WP Signals

5.14.2 SDHI Circuit



Points

ALL

- Since SDHI (MMC) is a relatively high-speed parallel interface, we recommend that you perform SI simulation with the use of an IBIS model.
- When pulling up the CMD and DAT3 to DAT0 signals, use the SDHI IO power supply (SDn_PVDD).

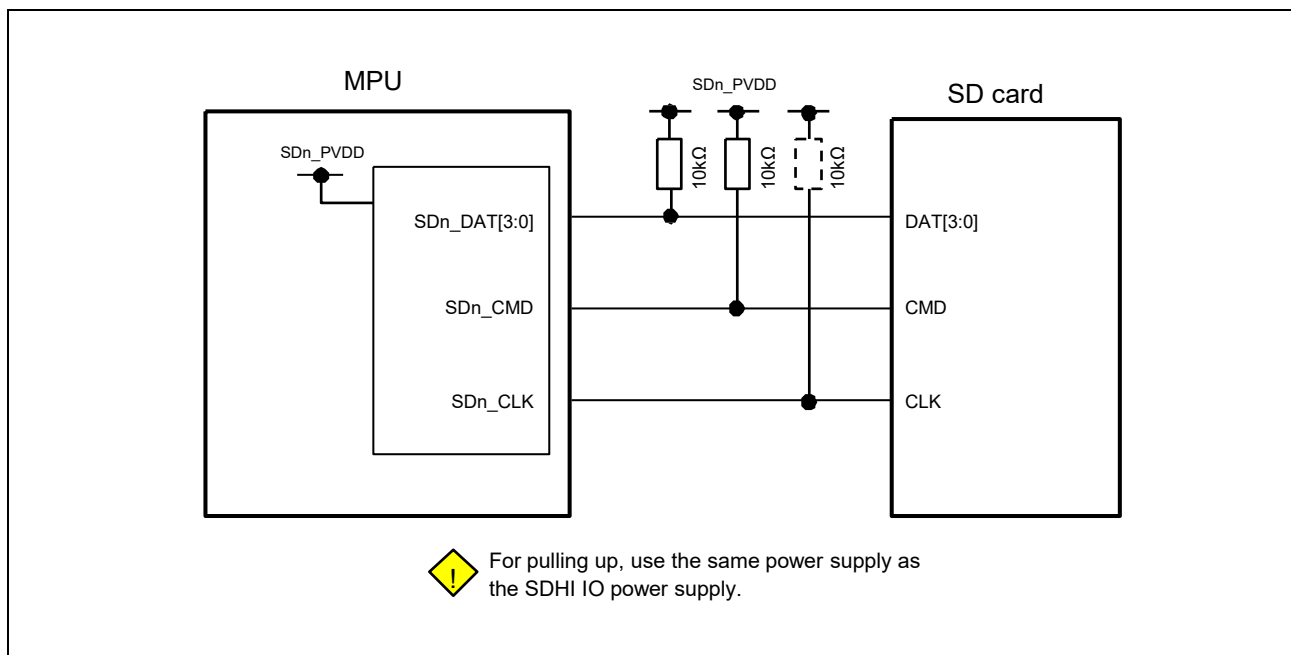



Figure 5.11 Pulling up of SDHI Signals

5.15 Connecting Ethernet PHY

 Points

G2L

G2LC

V2L

G2UL

Five

A3UL

G3S

G3E

Using gigabit Ethernet requires connection to an external PHY IC via the RGMII or MII.

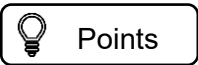
- For connection of RGMII or MII, refer to the following application notes and the datasheet of the peripheral device.

Table 5.2 Guidelines for Connection of the Ethernet PHY

Interface	Guideline
RGMII	<ul style="list-style-type: none">PCB Design Guideline for RGMII Interface

5.16 JTAG

5.16.1 Mode Setting



- Make sure that the mode pin DEBUGEN is set to preferable state.

JTAG can be used as a normal operation mode or a debug mode by switching a mode setting (DEBUGEN). If used as a debug mode, DEBUGEN must be pulled high. If using as a normal operation mode, DEBUGEN must be pulled low.

Table 5.3 Pull-Up/Pull-Down Processing of JTAG

Signal	Pull-up/Pull-down Processing
	JTAG
TDO	—
TRST	Pull-up
TCK/SWDCLK	Pull-up
TMS/SWDIO	Pull-up
TDI	Pull-up

5.16.2 TRST# pin



Points

ALL

- TRST# should be at the low level when the power is supplied.
- TRST# should be changed from the low level to the high level before PRST# is changed from the low level to the high level. Note that the EVK of RZ/G2L, RZ/G2UL, and RZ/V2L do not meet these criteria.
- The maximum TRST# input rise time is 180 ns. We recommend inserting a Schmitt trigger buffer into TRST# as shown in **Figure 5.12**.

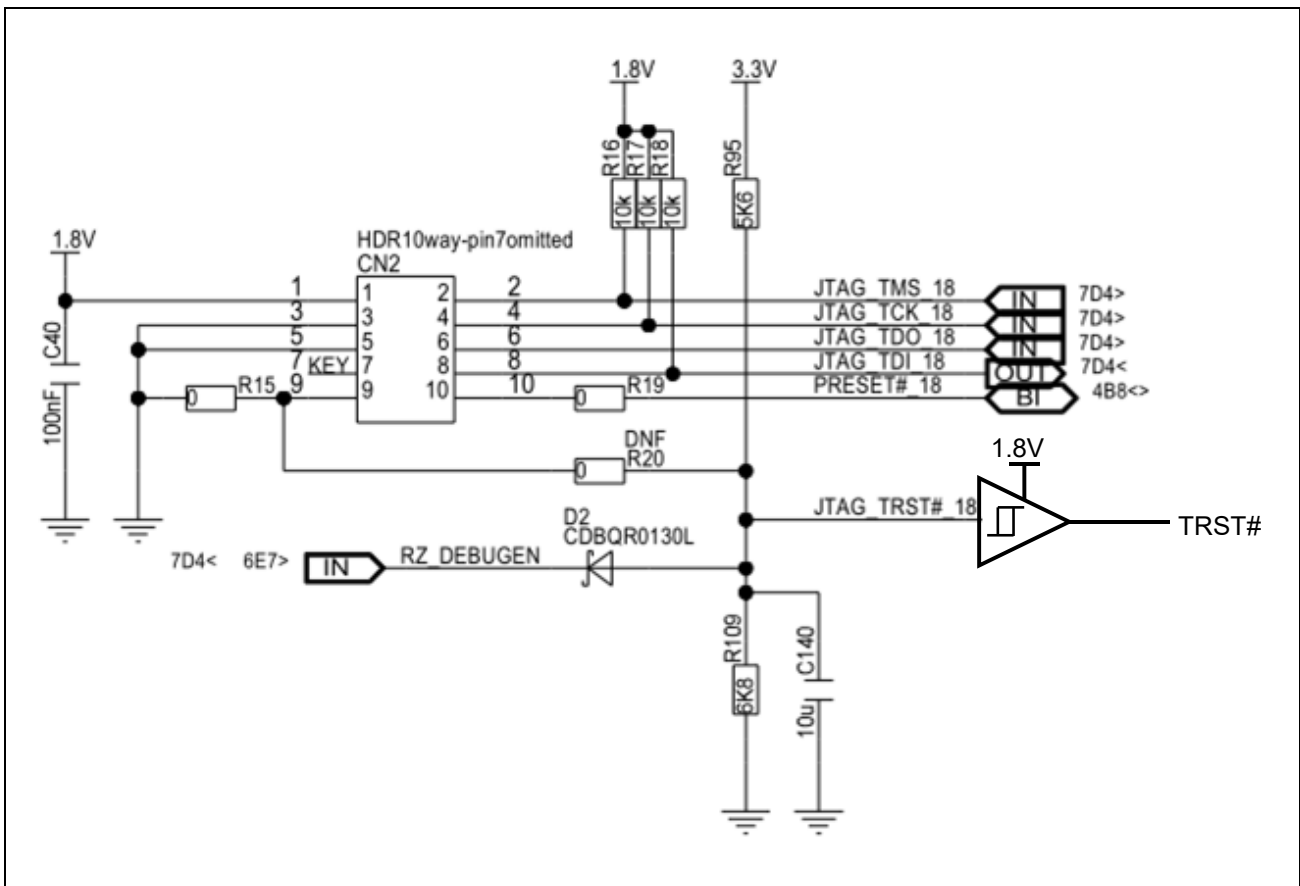


Figure 5.12 Insertion of Schmitt Trigger Buffer

5.17 I2C

5.17.1 IO Voltage and Buffer Type



Points

ALL

- Two types of buffers are available: low-driving with LVTTL buffers and open-drain buffers.

RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, RZ/A3M

- Open-drain type: This belongs to the 3.3V IO power domain and can be used with a 3.3 V I2C bus.
- LVTTL-buffer type: This belongs to the 3.3V IO power domain and can be used with a 3.3 V I2C bus.

RZ/G3S

- Open-drain type: This belongs to the 1.8V IO power domain but has 3.3 V tolerance, so can be used with a 1.8 V or 3.3 V I2C bus.
- LVTTL-buffer type: This belongs to the 3.3V IO power domain and can be used with a 3.3 V I2C bus.
- The I2C does not have 5 V tolerance. The voltage level shifting is required to use I2C with 5 V.
- When the LSI is powered off, the pull-up power of the bus also must be off.
- Select an optimal pull-up resistor for the bus in terms of the number of connected devices. For LVTTL-buffer type I2C, when the I2C function is to be used, internal pulling up of the LSI is always off regardless of the pull-up and pull-down settings.

Table 5.4 Specifications of Output Buffer of I2C of RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, RZ/G3S, RZ/G3E, and RZ/A3M

I2C	Output Buffer Type (LVTTL, OD = Open Drain)								
	RZ/G2L	RZ/G2LC	RZ/V2L	RZ/G2UL	RZ/Five	RZ/A3UL	RZ/G3S	RZ/G3E	RZ/A3M
I2C ch. 0	OD	OD	OD	OD	OD	OD	OD	LVTTL	OD
I2C ch. 1	OD	OD	OD	OD	OD	OD	OD	LVTTL	LVTTL
I2C ch. 2	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	—
I2C ch. 3	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	LVTTL	—
I2C ch. 4	—	—	—	—	—	—	—	LVTTL	—
I2C ch. 5	—	—	—	—	—	—	—	LVTTL	—
I2C ch. 6	—	—	—	—	—	—	—	LVTTL	—
I2C ch. 7	—	—	—	—	—	—	—	LVTTL	—
I2C ch. 8	—	—	—	—	—	—	—	LVTTL	—

Remarks

In short, the LVTTL output is used to achieve open-drain-like operation by turning off the output enable when the normal output buffer is driven to the high level.

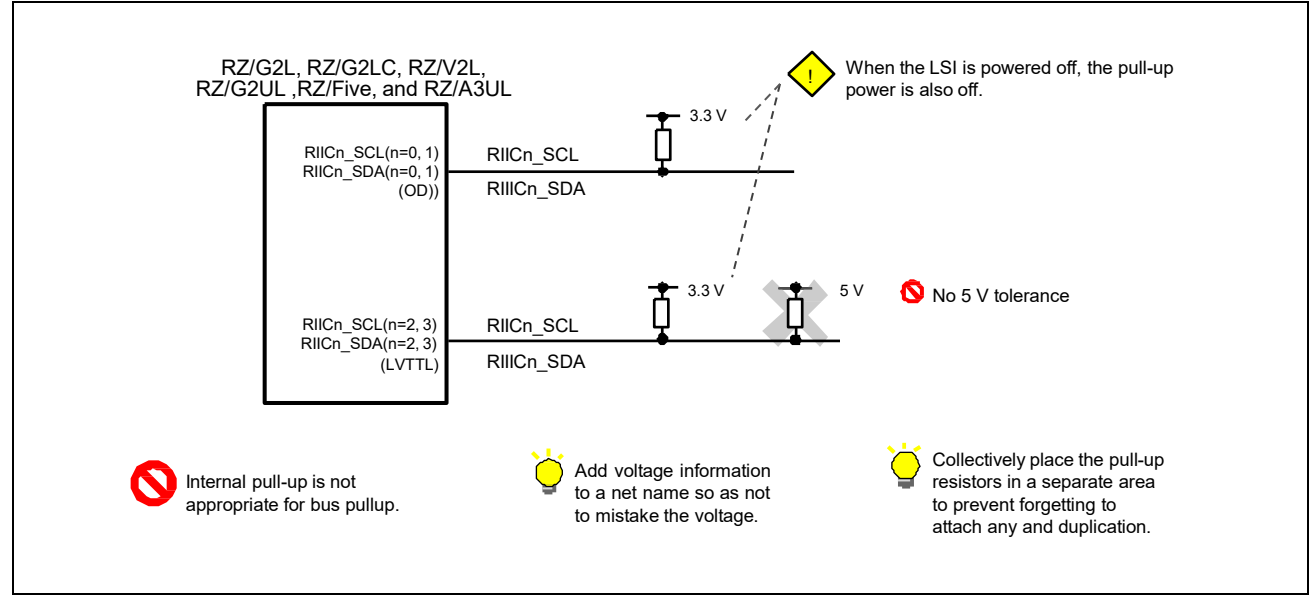


Figure 5.13(a) Example of a Circuit Configuration for I2C

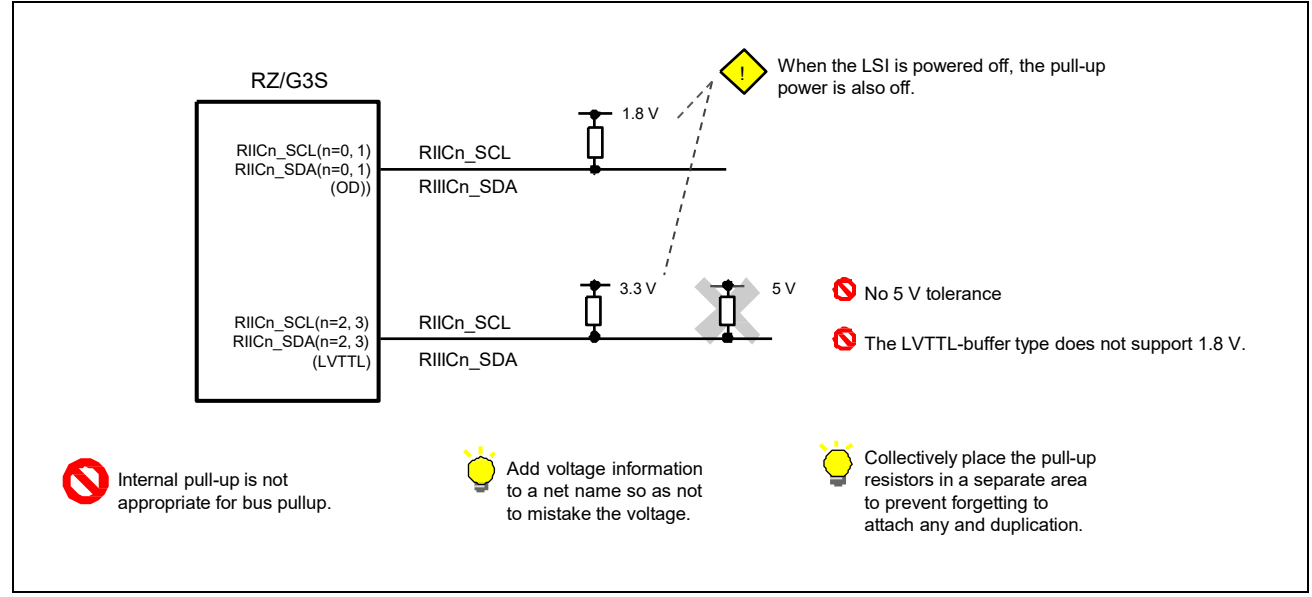


Figure 5.13(b) Example of a Circuit Configuration for I2C

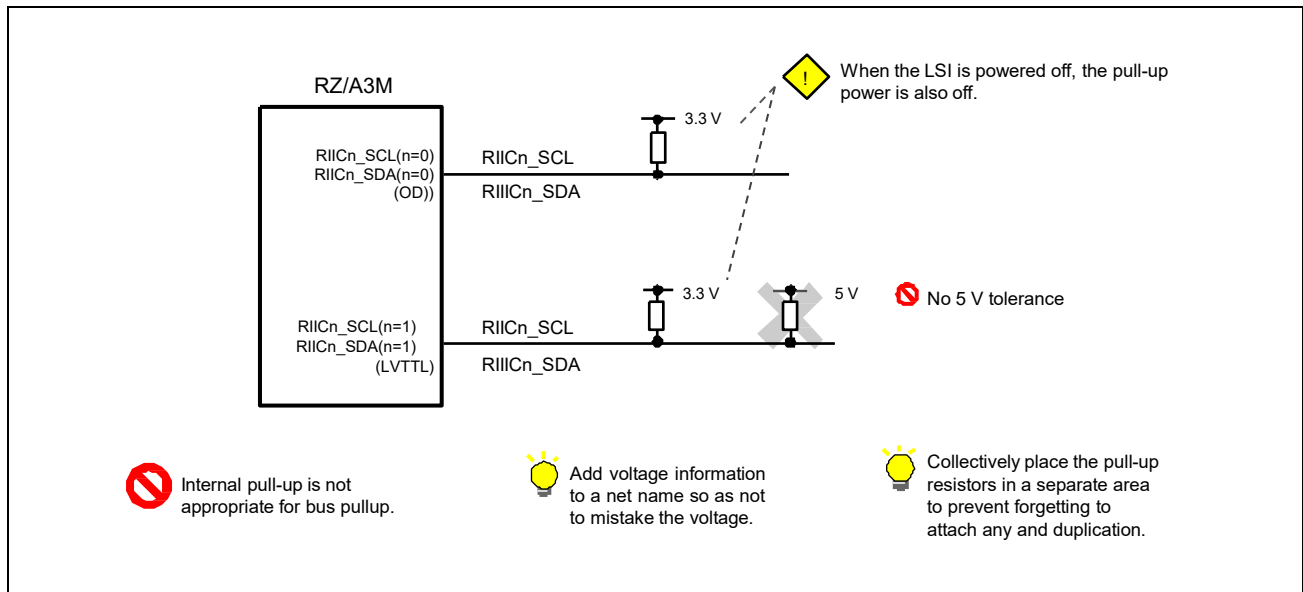


Figure 5.13(c) Example of a Circuit Configuration for I2C

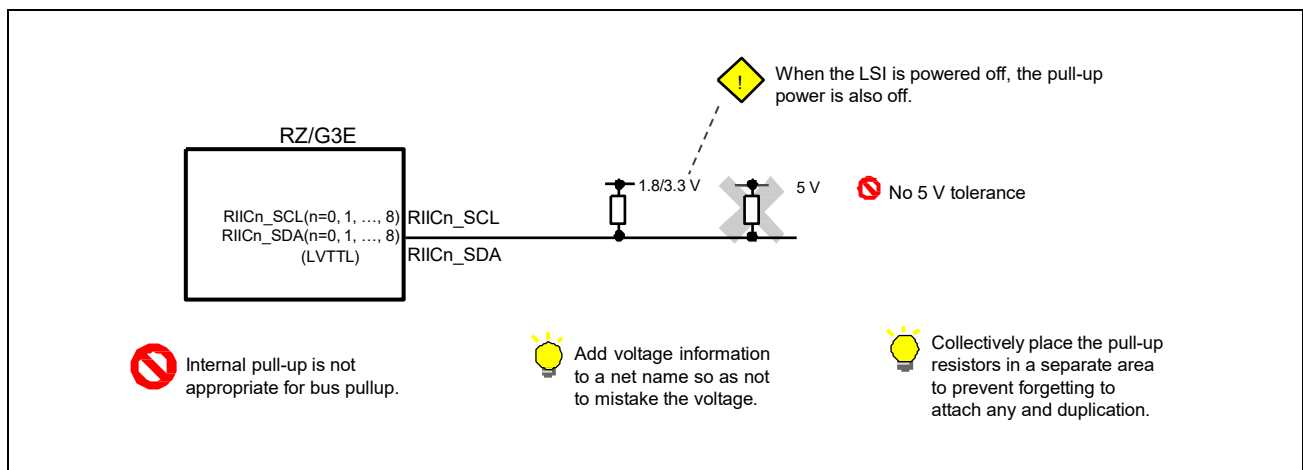


Figure 5.13(d) Example of a Circuit Configuration for I2C

Documents for Reference

- Hardware user's manuals for individual target devices
- Lists of pin functions for individual target devices
- Circuit diagrams of individual evaluation board kits
- Datasheets or technical documents for the individual peripheral devices

5.17.2 Slave Address



Points

ALL

- Check that the slave addresses are not the same.

I2C devices are identified by slave addresses. When connecting multiple I2C devices to the same I2C bus, be careful not to set the same slave address. If there is an I2C device with the same slave address in the same I2C bus, malfunction may occur. When using multiple I2C devices for which addresses cannot be set, you need to take measures such as connecting each device to a different I2C bus and using an I2C bus address translator IC.

- We recommend that you specify slave addresses and connect an I2C bus on the schematic to allow efficiency in software development by driver engineers, in circuit reviews and in debugging by third parties.

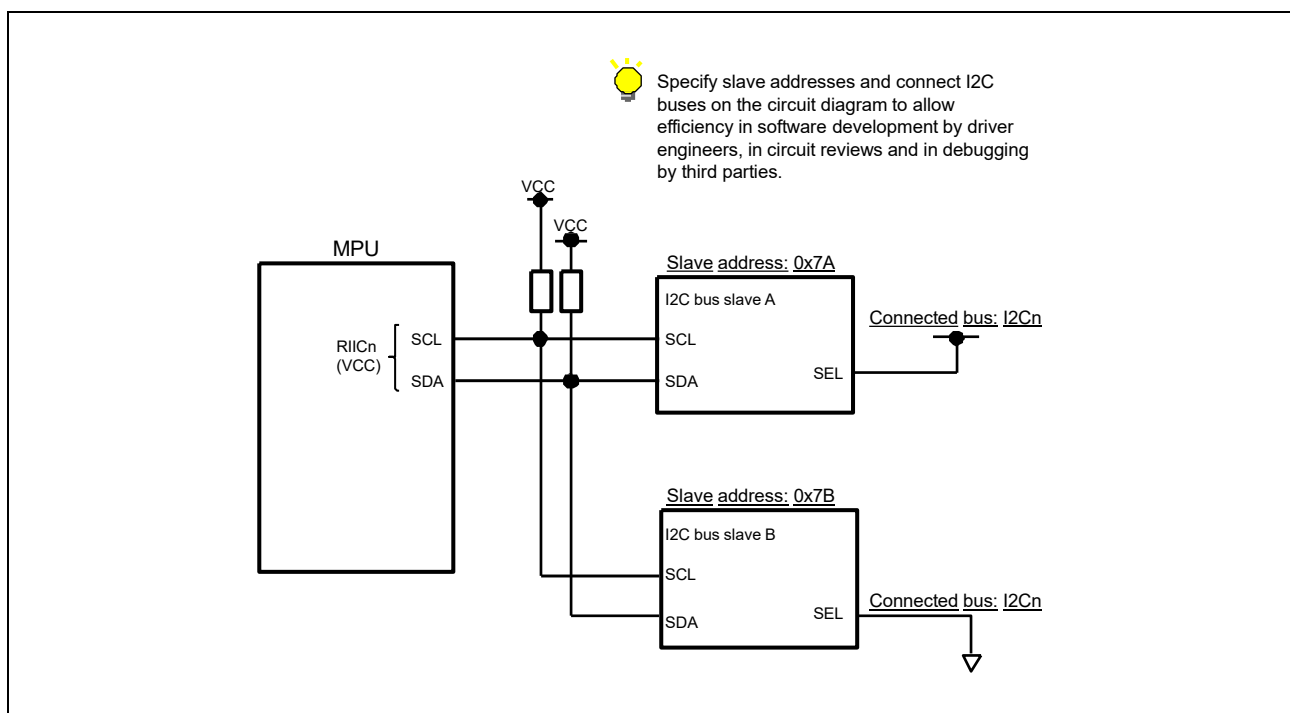
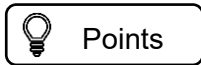


Figure 5.14 Example of a Circuit Diagram of I2C Devices

5.18 SCIF

5.18.1 External Input Clock



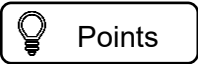
ALL

- Either external clock or internal clock can be selected as the SCIF clock source.
- If there is no possibility of changing the internal clock, and the error rate of the SCIF (UART) bit rate generated from the internal clock is within an allowable range, it is not always necessary to use an external clock.

Documents for Reference

- Circuit diagrams of individual evaluation board kits
- Datasheets or technical documents for the individual peripheral devices

5.18.2 SCIF0 for Debug



G2L	G2LC	V2L
G2UL	Five	G3S
		A3M

- SCIF0_RXD/TXD must be assigned so that it can be used as a SCIF download.
- It is recommended that SCIF0_RXD/TXD be ready to be connected to a console for debugging.
- The following circuit configuration is recommended to output to a console when power is turned on.

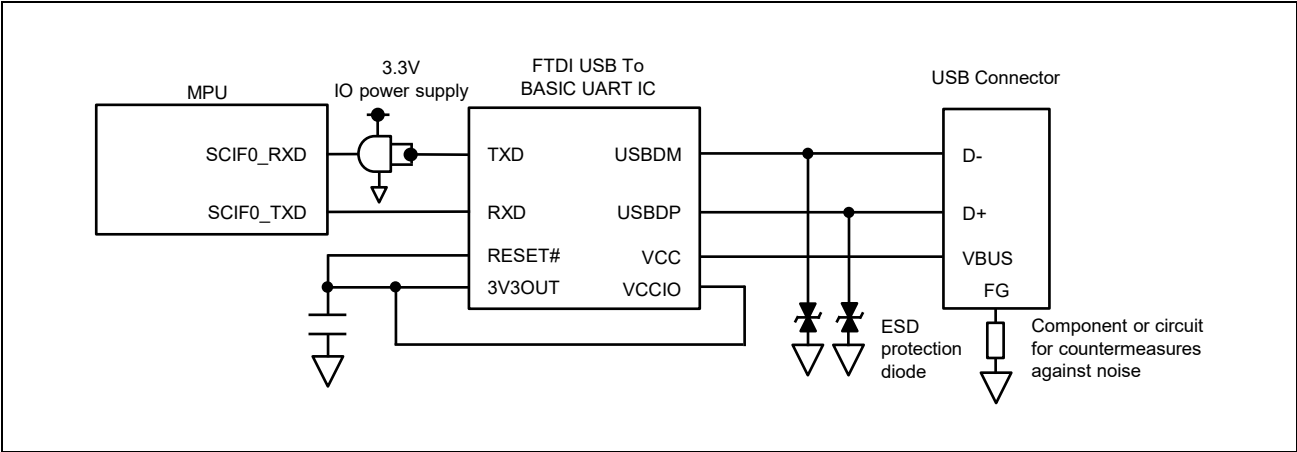
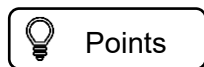


Figure 5.15 Example of a Circuit Configuration for SCIF0 Signal

5.19 Audio

5.19.1 Coupling Capacitors for Audio Output Circuits



ALL

- Pay attention to the polarity if you are using aluminum electrolytic capacitors as coupling capacitors for the audio circuits.
- Please refer to the datasheet of the peripheral devices to be used.

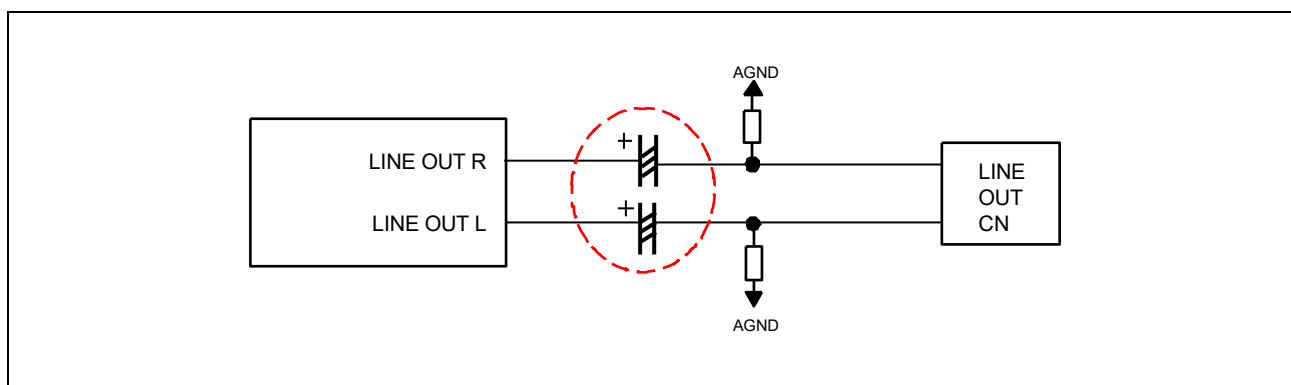


Figure 5.16 Polarity of Electrolytic Capacitors for Audio Output Circuits

Documents for Reference

- Circuit diagrams of individual evaluation board kits

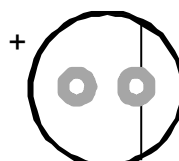
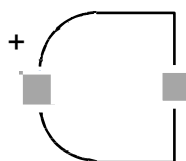
5.20 Polarity of Electrolytic Capacitors



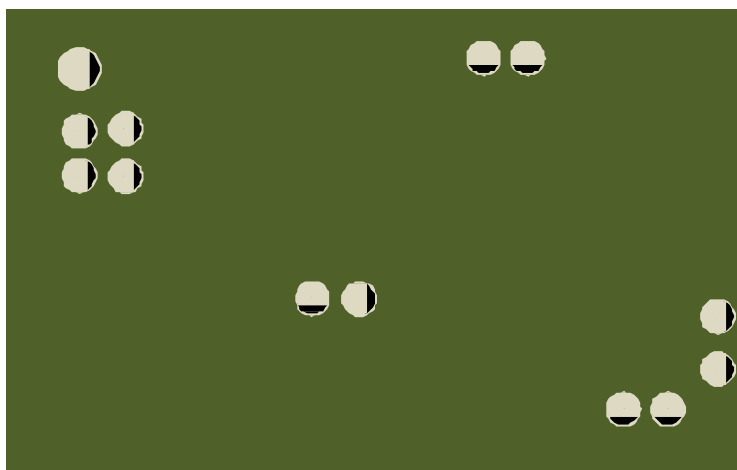
Points

ALL

- Incorrect polarity of the power supply capacitor may cause a serious accident such as generation of toxic gas.
- To make it easy to detect errors in implementation when designing a circuit in addition to paying attention to correct polarity of the power supply capacitor, observe the following.
 - Silk-screen markings to highlight the point
 - Devising the layout and component arrangement for uniform orientation



Prevent errors by silk-screen printing of shapes.



Devise the layout and component placement such that orientation is uniform both vertically and horizontally to reduce the possibility of errors in implementation.

Figure 5.17 Silk-Screen Printing and Orientation of Electrolytic Capacitors

5.21 Programming On-Board EEPROM



Points

ALL

- A system configuration in which on-board EEPROM is installed for the writing and reading information such as configurations of the system power supply (PMIC), an FPGA or CPLD, MAC address, and board ID via target devices or a separate on-board controller might be useful in terms of evaluation and debugging.
- Accessing the internal SPI or EEPROM on the I2C bus when the target devices are not powered on violates the absolute maximum rating. In such a situation, the circuit must be configured so that the target devices are isolated and protected.
- In particular, you need to pay attention to devices that are not powered on, including the MPU, when programming an FPGA/CPLD that includes the system power supply (PMIC) and power control circuit.

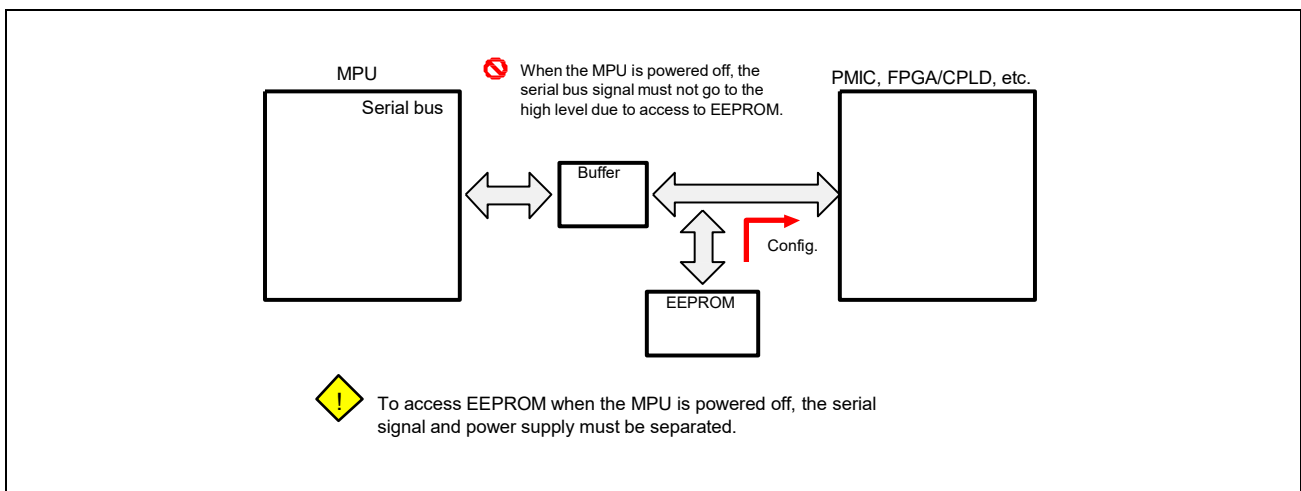


Figure 5.18 Example of a Circuit to Program the On-Board EEPROM

Document for Reference

- Circuit diagrams of individual evaluation board kits

5.22 Board to Board Connector



ALL

Note the following points when installing board-to-board connectors for peripheral devices and the expansion of memory.

- Is there any consistency in the connector pin arrangement between the main board and the expansion board?
- Is the connector pin arrangement designed so that noise such as crosstalk is likely to be applied?
- Is there no problem with the allowable current per connector pin when power is supplied through the connector?
- Do the connectors have a sufficient number of GND pins in terms of the allowable current and reducing noise?
- Is the power supply on the main board designed to use expansion boards?
- Are the values of capacitors on the connector's boundary plane sufficient?
- When power to the target devices and peripheral devices on the main board is off, will the expansion board circuit not produce a high-level output?
- Are measures such as against the reverse insertion of connectors taken?
- Are the heights of the connectors sufficient for those of the components on the main board and expansion boards?
- Are safeguards against the connection of extension boards that might render the board inoperable sufficient?

Documents for Reference

- Circuit diagrams of individual evaluation board kits
- Datasheets or technical documents for the individual connectors and connected devices

5.23 Confirm Part Number of MPU



ALL

- Make sure that the MD pin settings suit the revision of the device.
 - For optional products such as for security, the MD pins (details are not disclosed) may need to be set to the side designated as “prohibited”.
- Please confirm the Part Number of the MPU.

5.24 Reconfirm Operations of Re-used Circuits



Points

ALL

- Although using circuits designed and evaluated for past hardware as design assets is common practice, assuming that a circuit is proven may delay the detection of defects and problems with the circuit.
- Confirming that points of change such as the conditions applicable to peripheral circuits and changes to the specifications of the ICs used do not raise problems is important, even for a circuit with a proven track record.
 - Have new restrictions not been added?
 - Has the revision number of the device to be used not changed?
 - Are the adapted circuits appropriate compared to application circuits described in the technical documentation?
 - Is the power connection and signal connection inconsistent due to careless copy and paste?

5.25 Watchdog Timer (WDT)



G3S

G3E

- Be careful when using the WDT terminal of RZ/G3S and RZ/G3E. When the PRST# signal level is low, the pin condition of the WDT terminal is Hi-Z, not the high level. Therefore, an external pull-up resistor is required.

6. PCB Layout Design

6.1 Power Supply

6.1.1 Target Impedance

 Points

ALL

- Design power supplies to meet target impedance.

Target impedance is shown for some power supplies. The target value is only a desirable value in the pattern design of the power supply and does not guarantee that it will not fail. However, designs that greatly exceed the target values can cause failures. Therefore, it is recommended to design patterns within the target values.

Table 6.1 Guidelines Describing Target Impedance

Power Supply	Related Guideline
Logic power supplies (VDD)	PCB verification guide for Core
DRAM I/O power supplies (DDR_VDDQ)	PCB verification guide for DDR
USB	PCB design guidelines for High-Speed Signal Interfaces
MIPI-CSI	
MIPI-DSI	
PCIe	

6.1.2 Trace Width



Points

ALL

Current of several amperes may be drawn through power supply pins. For such power supplies, take care with the widths of wiring patterns between the power supplies and the LSI.

- The recommended width of power supply patterns is generally 2 mm per A to take the DC resistance of copper and the generation of heat into account. Even if a pattern width alone cannot satisfy the above recommendation, ensure no more than 2 A per mm as a minimum requirement. In cases where sufficient pattern width cannot be ensured, consider countermeasures such as sharing the pattern for the same power supply between 2 layers.
- When the wiring patterns for power supplies are such that wiring runs are drawn from a power supply IC to multiple layers through via holes, take the maximum current into account in ensuring a sufficient number of via holes.
- On the target devices, logic power supply pins which draw relatively large amounts of current are arranged around the center of the package. Take care that the wiring patterns for the power supplies are not narrowed or divided into parts due to clearance for via holes to be used in bringing signal lines out from the pins on the periphery of the package. Examine the widths of power supply patterns in terms of the clearance for via holes being removed from the conductor widths.
- Narrow wiring patterns for power supplies lead to the generation of heat on the board itself. The combination of the generation of heat by the MPU itself and narrow patterns leads to further lowering of the power supply voltage due to the DC resistance vs. temperature characteristic of copper. This also makes countermeasures for heat more expensive.
- When a power supply IC has a remote-sensing pin, placing the sensing pin closest to the MPU (the source of the power consumption) is advantageous from the viewpoint of cancelling the voltage-dropping effect of the power supply pattern.

Pattern width:

The per-square resistance of copper foil with a thickness t of 35 μm at 20°C is approx. 0.5m Ω . When such a wiring pattern for a power supply is 20-mm long, the DC resistance of the pattern is approx. 10m Ω . In this case, if a 5-A current is drawn, the voltage drops by approx. 50 mV.

The resistance of copper has a positive temperature coefficient. The temperature of the wiring pattern for a power supply changing from 20°C to 100°C will increase the resistance by approx. 1.35 times.

When $t = 35 \mu\text{m}$, rough estimates of the allowable currents for limiting the rise in temperature to 10°C and 20°C are 1 A and 3 A, respectively, per mm of width.

Via hole:

The thickness of the plating metal of a standard via hole is from 10 μm to 20 μm . A via hole must be suitable for the current that flows through it according to the same considerations as described for pattern width above. A rough estimate of the allowable current is 0.5 A for a via hole 0.5 mm in diameter and 0.3 A for a via hole 0.3 mm in diameter.

When the width of a power supply pattern is reduced to bring signal lines out as shown in the figure at right, examine the width of the power supply pattern with the parts occupied by the via holes and the clearance between them removed.

Ensure sufficiently wide paths for the flow of current from each power supply through countermeasures such as taking the placement of via holes into account, as in the example at right. If doing so is impossible, consider other measures such as using two layers of wiring for the power supply or exchanging the PCB design for a build-up board that has no via holes.

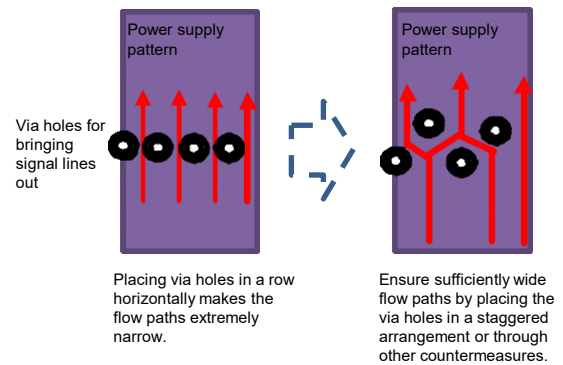


Figure 6.1 Width of Wiring Patterns and Via Holes for Power Supplies

6.2 Exposed Pad



Points

ALL

- Some ICs such as power supply ICs have exposed pads to improve heat dissipation.
- The exposed pad may not be defined as an LSI pin in some cases. To avoid forgetting the need for connection to the specified destination such as the ground or a power supply, apply countermeasures such as adding pin names for exposed pads to the circuit diagram.
- The majority of exposed pads are intended for the dissipation of heat. So that the generated heat is propagated to the inner layer along paths with low thermal resistances, apply countermeasures such as using more via holes leading to grounds in the inner layer than would be usual.
- If a recommended wiring pattern for the LSI chip covers the wiring pattern around an exposed pad, follow the recommendation.

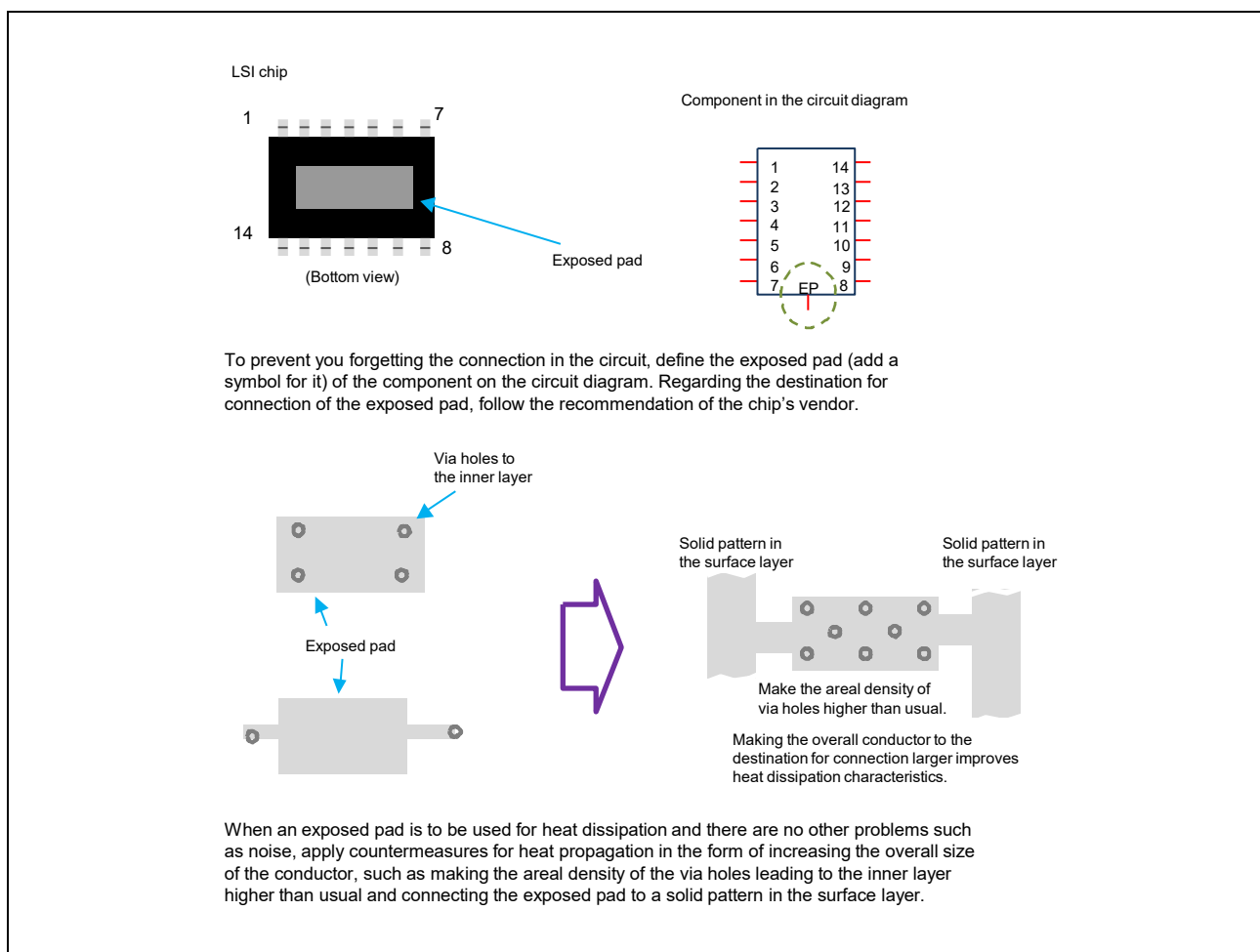


Figure 6.2 Handling Exposed Pads

6.3 Digital and Analog Ground



Points

ALL

- Analog grounds are sensitive to noise, so take particular care to avoid the application of noise from digital or signal grounds, which are relatively noisy. This is why separating analog grounds from digital and signal grounds and only connecting them at a single point are recommended in most cases. Avoid the analog ground not being connected or being connected to multiple points in the layout of patterns on a PCB by stating the one-point connection as a note on the circuit diagram.
- As the ground around a switching power supply IC draws a large amount of current in many cases, the ground is usually separated as a power ground. Most power supply IC makers provide a recommended layout of patterns on PCBs. Clearly state that the recommended layout is present on the circuit diagram.
- When connecting a frame ground for USB memory or an SD card, etc. with a digital or signal ground, take appropriate measures such as a one-point connection through noise-suppressing components. If a connector vendor provides a recommended layout of patterns on PCBs, follow the vendor's recommendation.
- When connecting a chassis ground and a PCB, take the application of external noise such as electro-static discharge (ESD) into account in the pattern design. Though the way of connecting a chassis ground and digital or signal ground differs from case to case, including non-connection, ensure the following points: noise must run through paths with relatively low impedance and be earthed; and the above paths do not include digital or signal grounds for the LSI chip that is the main component.

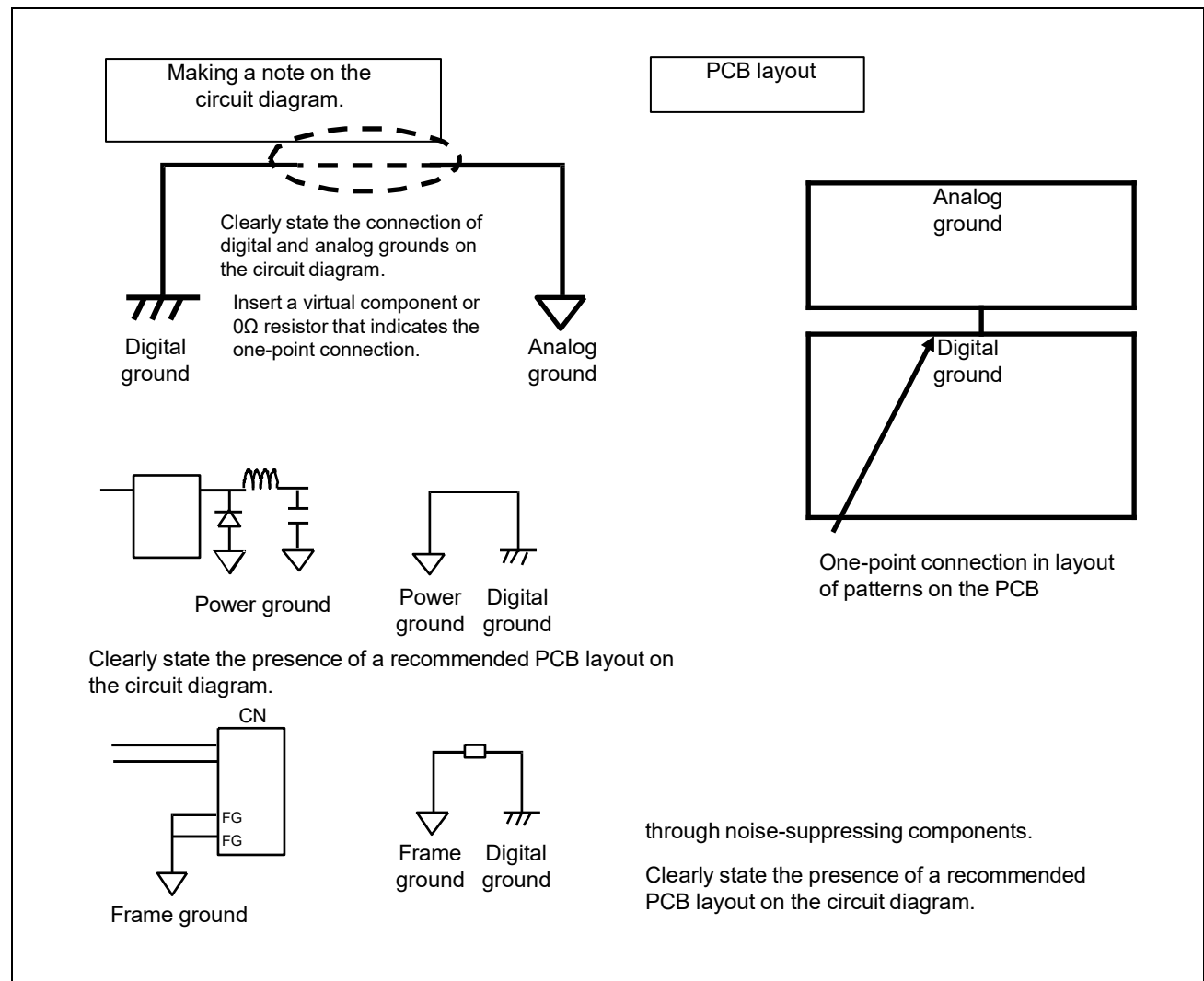


Figure 6.3 Connecting Digital Grounds to Other Grounds

6.4 Ground Shields/Guards



Points

ALL

- Applying ground shields to clock, reset, or faint analog signals may be desirable or necessary in many cases.
- Ground shields are only effective if the wiring is appropriate. Inappropriate wiring may lead to the ground shields having the opposite effect to that which was intended.
 - Be sure to connect both sides of a ground shield to the ground plane in the inner layer to prevent their being left open-circuit.
 - When the ground shield wiring runs are long, as well as a single via hole leading to the ground layer from both sides, place a via hole every 5 to 10 mm.
 - The width of the ground shield lines must be at least the same as that of the signal line, and ideally at least as wide as the diameter of the via holes leading to the ground plane.
- Care is also required in the placement of solid patterns of ground in unused areas of the PCB.
 - If this prevents the preparation of via holes leading to the inner ground, do not proceed with the application of a solid pattern of ground.
 - For a large solid pattern of ground, place one via hole leading to the ground layer roughly every 10 mm.
- Especially in the case of applying ground shields to high-speed signals, take care with regard to the uniformity of the shields.
 - When applying a ground shield to a high-speed signal, take care on the following points: do not change the spacing between the signal and ground shield along their paths; do not divide the ground shield into parts due to via holes; and as far as possible, do not allow variation in the wiring widths of a ground shield.
- When applying ground shields to differential wiring, take care with regard to the point that the ground shields being too close to the differential wiring is likely to have a strong effect on the differential combination.
 - In the wiring of a ground shield, its clearance must be at least twice the spacing of the wiring for the differential signals.

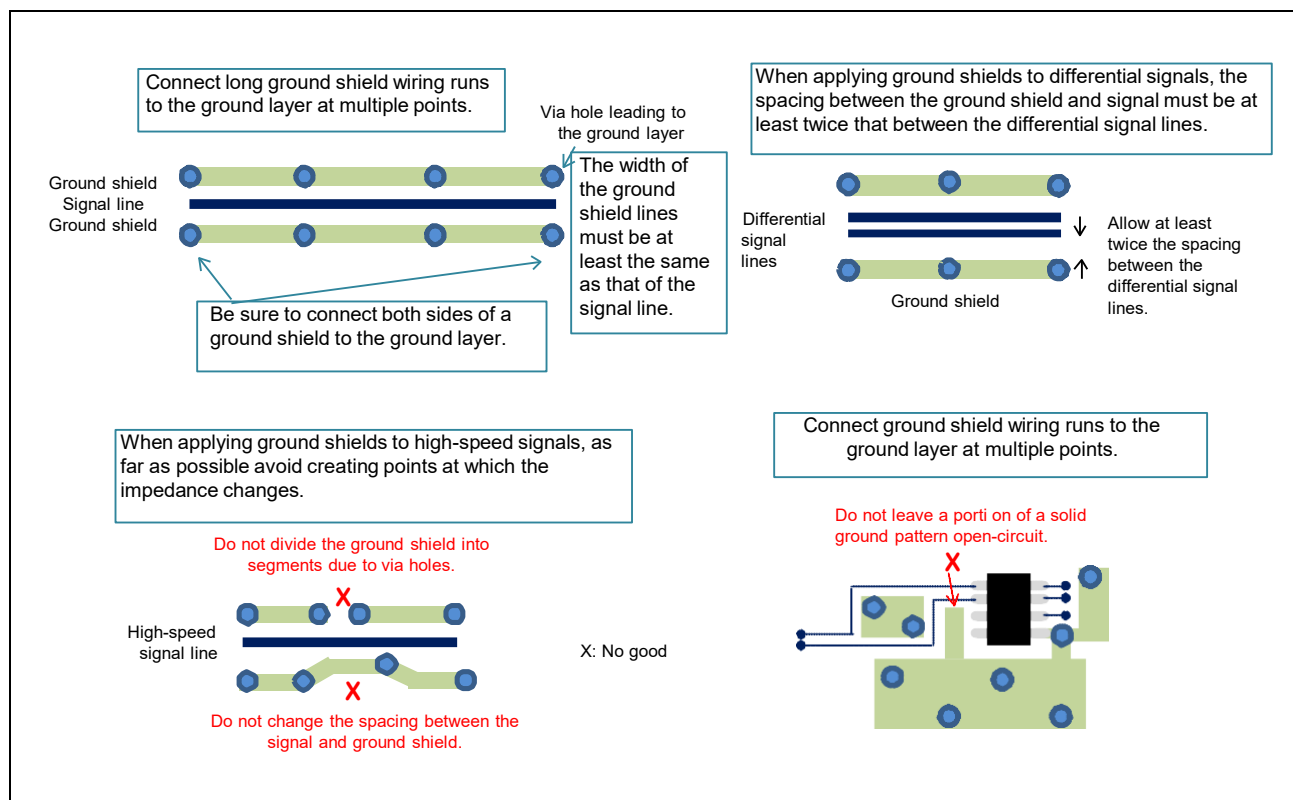


Figure 6.4 Ground Shields/Guards

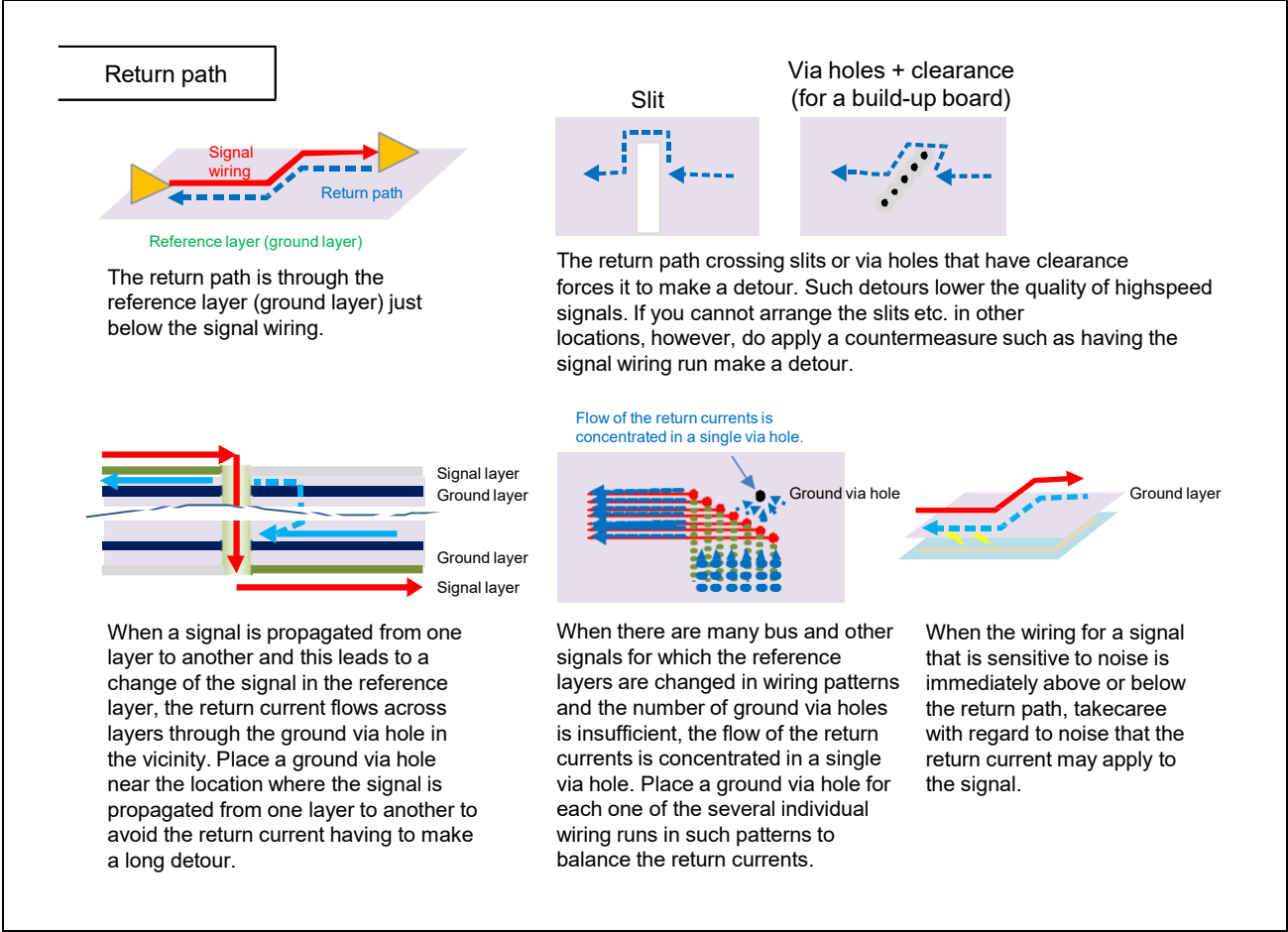
6.5 Return Path



Points

ALL

- A single-ended signal is propagated from a driver to a receiver through signal wiring, and a return current flows from the receiver to the driver at the same time. In such cases, the path along which the return current flows is referred to as a return path. The ground or power supply layer placed closest to the signal wiring serves as the return path in most cases. To retain signal quality and prevent problems before they arise, take the return paths into account in pattern design.
 - In most cases, return paths are just below the signal wiring.
 - The higher the speed of a signal, the more important taking return paths into account in pattern design to retain the signal quality becomes.
 - Take care that arranging via holes to change bus signal wiring runs from one layer to another does not create slits along the return paths.
 - Take care slits in the ground layer or clearance for use with via holes arranged horizontally do not divide the return paths into parts.
 - When a reference layer (ground layer) for use as a return path is changed, place a ground via hole in an appropriate location to avoid a detour from the original return path.
 - If insufficient via holes leading to the reference layer (ground layer) are present near locations where LSI signals are brought out or bus signals are propagated from one layer to another, etc., the flow of the return currents will be concentrated in a particular via hole, leading to the generation of noise such as crosstalk from the return paths. To avoid this, place a ground via hole in every one of several signal wiring runs near locations where signals are propagated from one layer to another.
 - For wiring patterns for circuits that are sensitive to noise such as crystal oscillation circuits, pay attention to the return paths of signals as well as the wiring patterns in the circuit diagram, such as in terms of parallel runs of signal wiring.



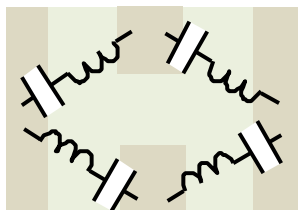
6.6 3-Terminal Capacitor with “Non-feedthrough” Connection



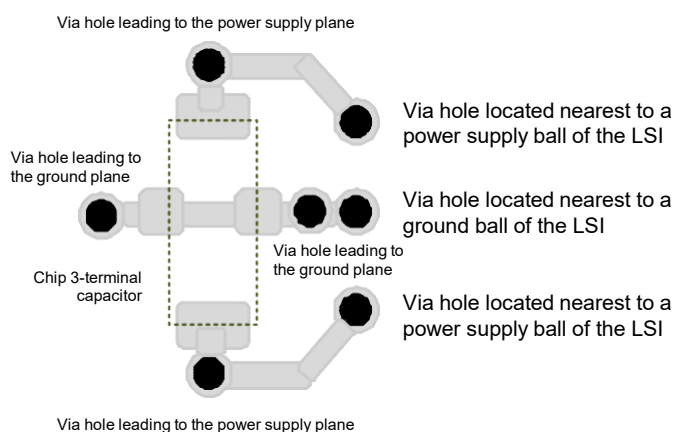
Points

ALL

- When a chip 3-terminal capacitor that does not have a feedthrough connection is used for its structural advantages, consideration of pattern design is important in bringing out its performance.
- For details, refer to the Web page of Murata Manufacturing Co., Ltd. and TDK Corporation.



Equivalent structure of a chip 3-terminal capacitor



When using a chip 3-terminal capacitor that does not have a feedthrough connection, use a pair of ground via holes for both ground pins in the center to make more effective use of the four capacitors that are equivalently generated as bypass capacitors in terms of the internal structure.

Figure 6.6 Designing Wiring Patterns when Using a Chip 3-Terminal Capacitor with a “Non-feedthrough” Connection

6.7 High-Speed Interfaces

 Points

ALL

- Please refer to the guidelines in the following table for high-speed signal interfaces.

Guidelines for board development regarding the DDR4/DDR3L, USB 2.0, CSI, and DSI are separately available and listed in the following table. Each guideline covers constraints, instructions, and guidance on the design of the related patterns on a PCB. Refer to these guidelines in pattern design. The guidelines also state reference documents from vendors other than Renesas and recommend referring to them. As these documents may also cover constraints, instructions, and guidance, refer to them together with the guidelines from Renesas.

Table 6.2 Guidelines for High-Speed Signal Interfaces

Interface	Guideline
DDR4, DDR3L	PCB design guideline for DDR4/DDR3L
	PCB verification guide for DDR4/DDR3L
LPDDR4, DDR4	PCB design guideline for LPDDR4/DDR4
	PCB verification guide for LPDDR4/DDR4
USB	PCB design guidelines for High-Speed Signal Interfaces
MIPI-CSI and DSI	
PCIe	

6.7.1 Differential Signals



Points

ALL

- The target devices have several high-speed differential signal interfaces such as the USB modules.
 - In differential interfaces in general, positive and negative signals are paired. This allows reduction of the signal amplitude and increases the immunity to common mode noise, thus allowing for higher-speed transfer.
 - Wiring patterns for pairs of differential signals are required to make the best use of differential transfer.
 - To avoid any problems arising later, consider modelling interface components such as components to be inserted and connectors in advance, and confirming the signal quality such as in terms of the deterioration of open eye patterns through simulation.
1. Wiring of differential pairs
 - Design the wiring patterns for pairs of differential signals while basically maintaining the required isometry and parallelism without changes in the width and spacing of the wiring.
 - As far as possible, that is, unless this presents a difficulty in terms of bringing the signal lines out or inserting any components for use as countermeasures for noise, place the wiring pairs for differential signals in the same layer.
 - When the locations where the signal lines are brought out lead to differences in electrical length, as far as possible adjust the lengths by a measure before the location. Methods of adjustment include changing the direction in which the signals are brought out. Do not use meandering wiring.
 - When a bend in a signal wiring run leads to a difference in electrical length, adjust the lengths to remove the difference by a measure as close as possible to the location where the difference was produced.
 - Place components such as those for use as countermeasures for noise, via holes for use in interlayer routing, and ground shields as close to symmetrically as possible relative to the wiring runs of differential pairs.
 - When you cannot avoid using meandering wiring to adjust the timing relative to that of other signals, ensure enough spacing of the meandering wiring relative to that of the other wiring for the differential pair.
 2. Differential impedance
 - Adjust the differential impedance to be roughly estimated as $\pm 10\%$ relative to the characteristic impedance specific to the given interface unless otherwise specified in the guideline or other documents for the given interface.
 - Remove the ground layer immediately under the wiring for differential pairs as required to adjust the impedance. Take care that the wiring runs of differential pairs do not cross slits in the ground plane for use as the reference layer.
 - When running the wiring for a differential pair from one layer to another, place a ground via hole near the via hole for the differential pair to suppress the generation of uneven impedances.
 3. Taking peripheral wiring patterns into account
 - When ground shields are not to be applied, the wiring for a differential pair and another signal must be separated from each other by at least five times the width of the signal wiring.
 - When ground shields are to be applied, the wiring for a differential pair and for the ground shield must be separated from each other by at least twice the width of the signal wiring.

- When bending signal wiring runs, do not bend them through right angles but by no more than 45° (or at least 135°).
- When you cannot avoid using wiring patterns that lead to deterioration of the signal integrity (SI) of differential signals such as for test points, use as few as is possible.

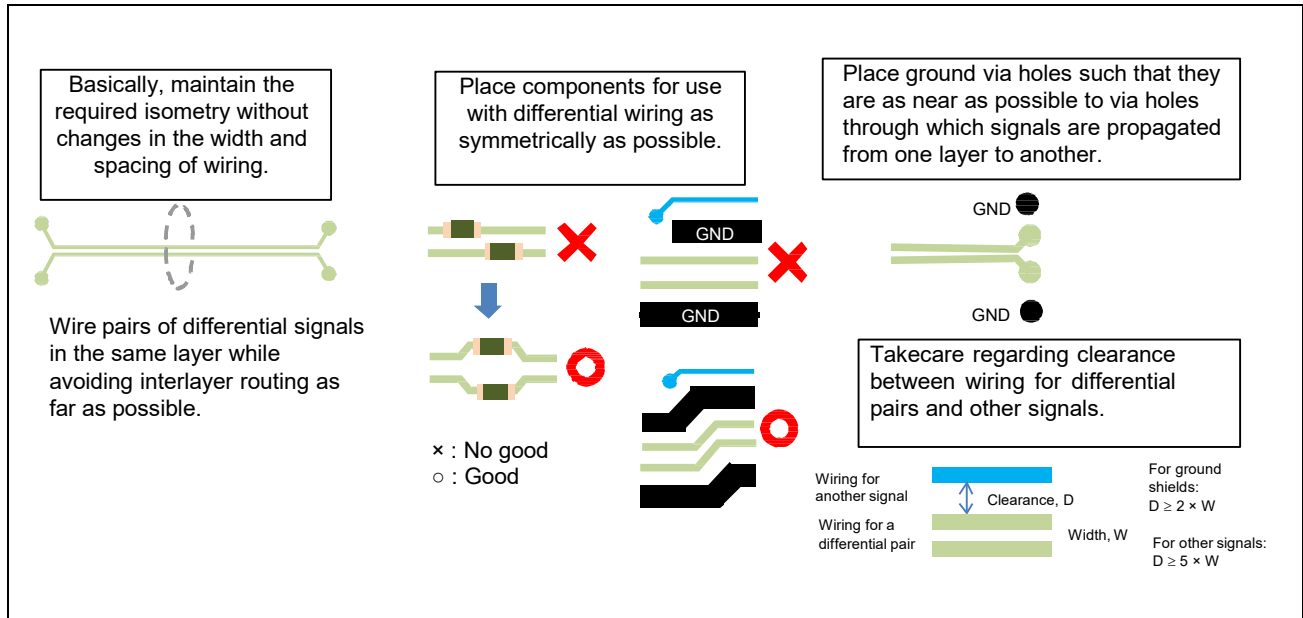


Figure 6.7 Designing Wiring Patterns for Differential Signals

6.7.2 Crosstalk

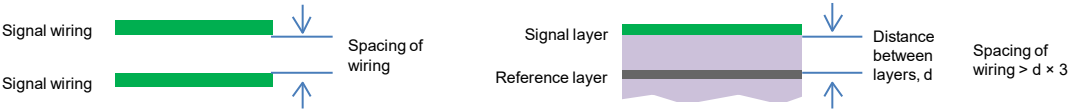


Points

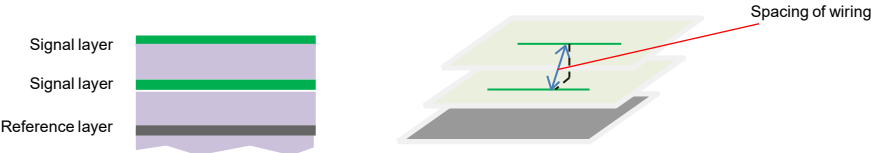
ALL

Especially in the case of wiring patterns for high-speed signals, deterioration of signal quality due to crosstalk affects timing design, and may also strongly affect signals that are sensitive to noise such as analog signals. Typical countermeasures for crosstalk are given below.

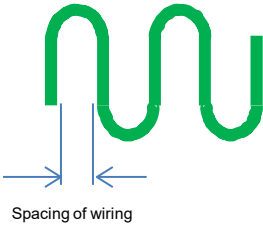
- For wiring patterns for single-ended signals, make the spacing between wiring runs as wide as possible, and take care not to arrange multiple wiring runs in parallel over long stretches.
- When multiple signal wiring runs are arranged in parallel over a long stretch in the case of the routing of buses or otherwise, apply countermeasures for crosstalk such as inserting ground signal wiring once every few wiring runs.
- Also, take care not to arrange wiring runs in parallel over long stretches in layers just above or below the wiring for high-speed signals.
- When using meandering wiring to adjust timing, take care that the meandering wiring itself is arranged correctly in terms of, e.g., the spacing.
- In pattern design where major adjustments of timing are required, verify how crosstalk affects the timing with the resulting wiring patterns through simulation to confirm that the patterns do not create a problem.
- When guidelines define constraints regarding wiring patterns such as spacing, follow the guidelines.
- When adjacent wiring is for signals that are sensitive to noise, ensure sufficient spacing, including for the respective return paths. Moreover, apply countermeasures such as the use of ground guards.



The reference spacing of signal wiring is set according to the distance from the solid ground layer or other layer that is just below the signal layer and serves as the reference layer and to the frequencies of the signals. For wiring patterns for high-speed signals, the standard spacing is at least three times the distance from the reference plane in most cases.



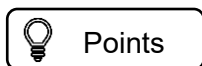
The reference spacing of signal wiring is set according to the distance from the solid ground layer or other layer that is just below the signal layer and serves as the reference layer and to the frequencies of the signals. For wiring patterns for high-speed signals, the standard spacing is at least three times the distance from the reference plane in most cases.



The concept mentioned above also applies to wiring patterns using meandering wiring for timing adjustment. Ensure that spacing between adjacent wiring runs is sufficient.

Figure 6.8 Taking Suppression of Crosstalk into Account in the Design of Wiring Patterns

6.7.3 Pads for Monitoring Signals



ALL

When placing pads for monitoring high-speed signals, take care on the following points.

- Place the signal pad on the signal line so that the stub lengths are as short as possible.
- Place a ground pad near the monitoring point if this is possible. When placing a ground pad in a ground shield, take care that slits in the shield and so on do not change the impedance.
- When the target for monitoring is a pair of differential signals, place the components including ground pads for use in monitoring symmetrically relative to the wiring runs of the differential pair.
- For monitoring a high-speed signal, select a monitoring point that suits the aims of the monitoring, such as close to the receiving terminal.
- When you proceed with simulation to check signal integrity (SI), do so with the inclusion of a pad for use in monitoring. Note that the signals monitored from the pad and at the receiving terminal will not perfectly match. The simulation of monitoring waveforms on the pad may be used to extrapolate those at the receiving terminal in later evaluation of the waveforms.

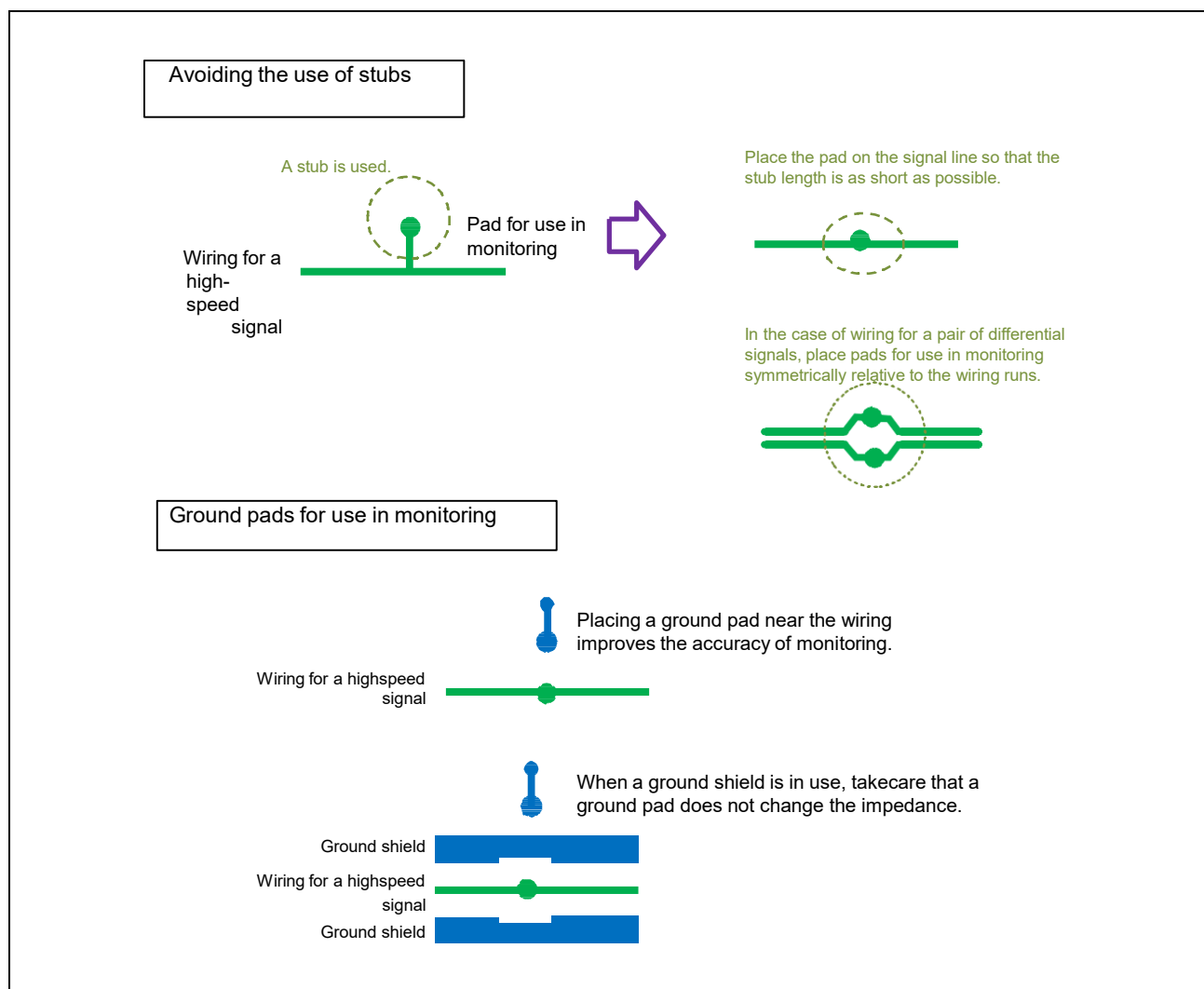


Figure 6.9 Wiring Patterns for Use in Monitoring High-Speed Signals

6.8 General Notes



Points

ALL

- General notes on designing wiring patterns for signals are given below.

When the wiring patterns for a circuit can be predicted to have a relatively strong effect on the signal quality, we recommend stating this as a note on the circuit diagram to aid in avoiding wiring patterns that are not as intended.

- For wiring patterns for relatively high-speed signals, avoid the use of stubs or branching of the wiring and make the wiring lengths as short as possible.
- For wiring patterns for clock signals, take care that elements such as reflections due to stubs or branches of the wiring and waveform rounding on rising or falling edges due to long wiring runs do not lead to excessive deterioration in the quality of the clock signals.
- When stubs are used in wiring of circuits for mode settings, external pulling up or pulling down, and filtering, make the stubs as short as possible.
- When bending wiring runs is not avoidable, do not bend them through a right angle but through 45° to avoid sudden changes in the impedance of the wiring. Especially for wiring patterns for high-speed signals, apply countermeasures such as rounding the wiring runs at the corners or using curved wiring to retain the signal quality.
- As far as possible, bring signal lines out near an LSI chip to take reflections of the signals at via holes into account. Moreover, keep the main wiring in the same layer.
- For wiring patterns for parallel synchronous signals such as in routing for a bus, use the same layer and employ isometric wiring.
- When using different layers for wiring patterns for parallel synchronous signals such as in routing for a bus is not avoidable, especially when an inner layer and the surface layer are used, simulate signal propagation and confirm that the delay times are the same on the bus as a whole. Adjust the wiring if this is not the case.
- For a circuit that has a record of unsuccessful operation, we recommend applying countermeasures for improving the monitoring performance in confirming its operation such as mainly using the surface layer for wiring patterns or the setting of test points.
- For wiring patterns for a crystal oscillation circuit, take care on the following points in general:
place the wiring patterns such that they are as near as possible to the LSI chip;
place the wiring patterns such that they are not too close to other patterns, including the digital ground, in the layer where the wiring patterns are placed and those above and below it;
as far as possible, remove the ground layer just below wiring patterns;
place the wiring patterns such that they are not too near to wiring for input or output; and apply load capacitance with the connection to the same ground.
- For wiring patterns for a crystal oscillation circuit, if the LSI vendor provides a recommended layout of patterns on a PCB, follow the recommendation.

6.9 Countermeasures for Noise



Points

ALL

- The inappropriate placement of components that serve as countermeasures for noise may prevent them being sufficiently effective and may even lead to their having the opposite effect to that which was intended.
- Even if the connection information such as for parallel circuits is the same as that in the net list, take care in terms of the order of connection and the method of connection to other circuits with grounds or power supplies possibly being important.
- State constraints and conditions on pattern design as notes on the circuit diagram as far as possible to avoid wiring patterns that are not as intended.
- Reference documents such as datasheets or design guidelines for the given LSI chip cover the recommended layout of patterns and constraints on the methods of connection. Follow the recommendations and apply the constraints.

Examples

- Place a common mode noise filter or component that serves as a countermeasure for electro-static discharge (ESD) nearest to its potential entry point, that is, the connector for use in connecting an external device.
- Place a damping resistor such that the resistor is as near as possible to the sending terminal, while placing a parallel terminating resistor such that the resistor is as near as possible to the receiving terminal.
- Connect a parallel or differential terminator after a wiring run passes through an input point to the IC to avoid the use of stubs as far as possible.
- Place a current reference resistor adjacent to the LSI chip to avoid lengthening the wiring run.
- Place bypass capacitors with a smaller capacitance nearer the given LSI power supply.
- Connect wiring runs for the reference voltage and remote sensing for a switched-mode power supply through a smoothing capacitor to a location where the ripple generated in the power supply line will be sufficiently small.
- For wiring patterns for filter circuits such as resistor–capacitor (RC) filters, connect the components in the order that provides the greatest effectiveness. Specifically, in a case where an RC filter is used to reduce noise in an IC input, connect the wiring run to the IC input pin through a resistor and capacitor, in that order.
- Connect a filter circuit to ground at one point if doing so makes it more effective.

7. Check List

Table 7.1 Check List

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
1	Reset	Check the IO voltage of the PRST#.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.1	
2	Reset	Do not set PRST# high when the MPU is powered off.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.1	
3	Reset	Make sure that the connection to TRST# is OK.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.1	
4	Reset	Make sure the PRST# signal is pulled up. We recommend the pull-up resistor no greater than 10kΩ. Determine the pull-up resistor to account for stray capacitance.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.1 1.2	
5	Reset	Also check the reset signals of peripheral devices. Peripherals with a reset terminal with Schmitt trigger IO are recommended.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.1 1.2	
6	Reset	Take care of the noise. Ex. Ground shield etc.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.2	
7	Reset	Note the pull-up/pulldown resistors scattered throughout the schematic.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.2	
8	Reset	Make sure the constraints are met for the reset timing.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.3	
9	Reset	Make sure that the oscillator stabilization time and reset release time are met.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.4	
10	Reset for peripherals	When PRST#, QSPI_RESET#, DDR_RESET# or SD0_RST# are used to reset peripheral devices, is the target peripheral device turned on?	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.5	
11	Reset for peripherals	Are the voltage and active sense of reset input for the target peripheral device correct?	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.5	
12	Reset for peripherals	Is the reset input for the target peripheral device set in consideration of the possible presence of an internal pull-up or pull-down resistor?	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.5	
13	Reset for peripherals	Is the driving ability of the reset signal sufficient?	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.5	
14	Reset for peripherals	Is PRST# connected to specific peripheral devices for which targeted devices have dedicated reset pins (such as QSPI_RESET#, DDR_RESET#, and SD0_RST#)?	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.5	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
15	Reset	When using GPIO as a reset for peripheral devices, make sure that the initial state of GPIO is Hi-Z.	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.5	
16	Reset	Make sure that the reset sequence is not a problem by comparing the power up/down timing diagram.	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.3	
17	MD pin setting	Did you check whether the connected device has an internal pull-up or pull-down resistor to maintain correct operation when the MD pin signal returns to its primary function?	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.6	
18	MD pin setting	Are the external pull-up and pull-down resistance values for setting the MD pin selected in consideration of the internal pull-up and pull-down resistors of targeted devices and peripheral devices?	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.6	
19	MD pin setting	Does the peripheral device malfunction due to external pull-up or pull-down for setting the MD pin?	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.6	
20	MD pin setting	Is the MD pin setting confirmed to keep the level for 100 ns or less after PRST # = H change?	Y	Y	Y	Y	Y	Y	Y	Y	Y	1	1.6	
21	XIN/EXCLK	Check the frequency. Only 24 MHz is supported.	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.1	
22	AUDIO_CLK	Is the voltage of the clock input appropriate?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.1	
23	EXCLK	Do not input an external clock exceeding the IO voltage level to the EXCLK pin during the power ON/OFF sequence.	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.4	
24	EXCLK	When using an external clock with the EXCLK pin, are the XOUT pin open and the XIN pin pull-down?	Y	Y	Y	Y	Y	Y	—	Y	Y	2	2.4	
25	Clock input	Check the requirement of the accuracy and deviation of the clock input.	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.2	
26	Clock for High-speed Interface	Is the clock input signal for the high-speed serial interface from a non-SSC type oscillator?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.4	
27	X'tal circuit	Do you include patterns for a damping resistor or feedback resistor that might be necessary for evaluating the oscillation of a crystal resonator?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.3	
28	X'tal circuit	Do the circuit constants for the crystal resonator match the constants of the crystal resonator in use?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.3	
29	X'tal circuit	Have you considered the notes in the circuit design guideline for the crystal resonator in use?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.3	
30	X'tal circuit	Is the crystal resonator free of oscillation in the unwanted overtone mode?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.3	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
31	X'tal circuit	Have you confirmed that the selected crystal resonator manufacturer supports the evaluation of oscillation?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.3	
32	Others related to clock	MD_OSCDRV should be connected to the GND.	Y	Y	Y	Y	Y	Y	—	—	Y	2	2.5	
33	Others related to clock	Did you pay equal attention to the clock input to peripheral devices and targeted devices?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.6	
34	Others related to clock	Did you pay equal attention to the connection of crystal resonators to peripheral devices and targeted devices?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.6	
35	Others related to clock	Did you follow the general notes in the guidelines for the connection of clocks to targeted devices and peripheral devices?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.7	
36	Others related to clock	Did you include instructions on ground shielding, such as in the wiring layers for PCB pattern design, in the circuit diagram for clock connections and clock wiring?	Y	Y	Y	Y	Y	Y	Y	Y	Y	2	2.7	
37	Power supply	Have you checked the power requirements for each power supply and that the power circuits have sufficient supply capacity? We recommend drawing a power tree.	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.1	
38	Power supply	In the development stage, it is recommended that the power supply capacity be designed with a margin to allow for the possibility that current consumption may be higher than expected.	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.1 3.2	
39	Power supply	In particular, use power supply ICs with sufficient margin for logic power supplies.	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.1 3.2	
40	Power supply	When lowering the estimated current for the logic power supply according to a use case, have you confirmed that the use case is reasonable?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.1 3.2	
41	Power supply	Have you placed a sufficient number of 0.1 to 10 μ F capacitors in the power supply circuit to handle sudden surges in the logic power supply?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.2	
42	Power supply	If you are using a switched-mode power supply for the logic power supply, have you confirmed that the switching frequency can follow the variations in load?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.8	
43	Power supply	Does the circuit configuration conform to the power-on and -off sequences?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.3	
44	Power supply	Did you create a time chart of the power-on and -off sequences for the entire power tree, and confirm that there were no problems?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.3	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
45	Power supply	Did you create a time chart of special conditions, such as the time of the first power-on, for the power-on and -off sequences of the entire power tree, and confirm that there were no problems?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.3	
46	Power supply	Is there any circuit that may cause damage when the power of targeted devices is being switched on or off, such as pulling up at the power supplies of peripheral devices?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.3	
47	Power supply	Are there enough discharge circuits for power-off to conform to the power supply sequence?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.3	
48	Power line filter	Have you selected and installed filters as recommended in the guidelines for power supply filter circuits to take account of the noise-sensitivity of dedicated power supplies?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.4	
49	Power line filter	Is the noise filter for the CPG PLL power supply one provided in the guidelines?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.4	
50	Power line filter	Have the noise filters for individual power supplies not been merged?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.4	
51	Power line filter	As well as targeted devices, have you selected and installed filter circuits as recommended in the datasheet or technical documentation for peripheral devices?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.4	
52	Power circuit	Did you analyze the impedances of the VDD power supplies by applying the method stated in the guidelines and confirm that there were no problems?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.5	
53	Power circuit	Did you analyze the impedance of the DRAM IO power supply by applying the method stated in the guidelines and confirm that there were no problems?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.5	
54	Power circuit	Have multiple DRAM IO power supply systems not been merged to act as a single power supply?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.5	
55	Power circuit	Did you analyze the inductance of the dedicated power supply for high-speed serial interfaces and IO power supply by applying the method stated in the guidelines and confirm that there were no problems?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.5	
56	Power circuit	As well as targeted devices, did you analyze the power supply impedances of peripheral devices that came with recommendations on this point, and confirm that there were no problems?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.5	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
57	Bypass capacitor	Did you install the appropriate number and capacity of bypass capacitors for the IO power supply?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.6	
58	Bypass capacitor	Did you install bypass capacitors in consideration of simultaneous-switching output noise SSO, such as placing capacitors with large capacitances of about 10 μ F at the end of the IO power supply pattern?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.6	
59	Bypass capacitor	Did you include instructions regarding the PCB pattern in the circuit diagram, such as the placement of capacitors with small capacitances near the device?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.6	
60	Bypass capacitor	Did you consider bypass capacitors for peripheral devices as well as for targeted devices?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.6	
61	Bypass capacitor	Do the bypass capacitors have sufficient capacity in consideration of the decrease in the effective capacitance due to variations in DC bias and temperature?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.7	
62	Bypass capacitor	Is the value of the bypass capacitor for the power supply circuit of the high-speed serial interface as recommended in the guide?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.7	
63	Bypass capacitor	If aluminum electrolytic capacitors are to be used as bypass capacitors, have you taken measures in the silk-screened markings or pattern design to prevent insertion with reverse polarity?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.19.1 5.20	
64	Power-IC circuit	Does the design conform to the recommended circuit provided in the datasheet or technical documentation of the power supply IC in use?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.8	
65	Power-IC circuit	Do the components for the selected power supply circuit, such as coils, FETs, and diodes, correspond to the power supply specifications?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.8	
66	Power-IC circuit	Did you include typical characteristics regarding the selection of peripheral components for the power supply IC in the circuit diagram?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.8	
67	Power-IC circuit	Does the design take the allowable losses and heat dissipation into account?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.8	
68	Power-IC circuit	Have you confirmed that the phase margin and gain margin of the power supply sufficient?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.8	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
69	Power-IC circuit	Did you place the remote sensing pin of the power supply IC in the vicinity of the load? Additionally, did you include instructions on PCB pattern design in the circuit diagram to avoid degradation of the power quality due to noise?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.9	
70	Power pin on CN	Do the numbers of power pins and FGND pins allow margins for the maximum current when power is being supplied via a connector?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.22	
71	Power pin on CN	Is a capacitor with a relatively large capacitance installed near the connector when power is being supplied via a connector?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.22	
72	SDHI power circuit	Did you take care to prevent the SD card power supply adversely affecting other power supplies when it is turned on or off?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.11	
73	SDHI power circuit	When the SD card power supply is controlled by the pin of targeted devices, does the configuration take into account the fact that the pin becomes Hi-Z when the power pin on the targeted devices side is initially turned on?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.11	
74	SDHI power circuit	Does the bypass capacitor for the SD card interface have a proven capacitance?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.11	
75	SDHI power circuit	Did you check that the SD card power supply being turned on while the power of targeted devices is off and IO pins are being pulled up does not violate the ratings?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.11	
76	SDHI power circuit	Is a discharge circuit prepared for the SD card power supply?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.11	
77	SDHI power circuit	Have you confirmed that no excessive voltage occurs when the voltage is changed in the SDHI IO power supply switching circuit?	Y	Y	Y	Y	Y	Y	Y	Y	Y	3	3.11.2	
78	USB	Is a load switch or similar component placed between the VBUS and the USB20_VUBUSIN so that 5 V is supplied from the VBUS to the USB20_VUBUSIN after the USB power supplies such as the USB2_VDD33 and the USB20_VDD18 are turned on?	—	—	—	—	—	—	—	Y	—	3	3.12	
79	LPDDR4/DDR4/DDR3L SDRAM	Is the connected DRAM supported by targeted devices?	Y	Y	Y	Y	Y	Y	Y	Y	—	4	4.2.1	
80	LPDDR4/DDR4/DDR3L SDRAM	Did you perform SI verification, timing verification, and PI verification for the connection between targeted devices and DRAM according to the guidelines?	Y	Y	Y	Y	Y	Y	Y	Y	—	4	4.2.2	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
81	LPDDR4/DDR4/DDR3L SDRAM	Is the DRAM to be used a product type (model) for which SI verification, timing verification, and PI verification have been completed?	Y	Y	Y	Y	Y	Y	Y	Y	—	4	4.2.3	
82	LPDDR4/DDR4/DDR3L SDRAM	Do the circuits for signal termination and ZQ pin handling follow the recommendations in the guidelines?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.2.5	
83	LPDDR4/DDR4/DDR3L SDRAM	Have you confirmed the selection of an appropriate DRAM connection topology?	Y	Y	Y	Y	Y	Y	Y	Y	—	4	4.2.4	
84	DDR4/DDR3L SDRAM	Is the configuration of the VREF circuit for DDR4 or DDR3L SDRAM appropriate?	Y	Y	Y	Y	Y	Y	Y	—	Y	4	4.2.6 4.2.7	
85	DDR4/DDR3L SDRAM	In designing the resistive division circuit to obtain VREF for DDR4 or DDR3L SDRAM, was the input current of the IC taken into consideration when selecting the resistor values?	Y	Y	Y	Y	Y	Y	Y	—	Y	4	4.2.6 4.2.7	
86	DDR4/DDR3L SDRAM	In designing the resistive division circuit to obtain VREF for DDR4 or DDR3L SDRAM, is VREF generated independently for each VREF pin?	Y	Y	Y	Y	Y	Y	Y	—	Y	4	4.2.6 4.2.7	
87	DDR4/DDR3L SDRAM	Is there any error in the tolerance of the resistor connected to the ZQ pin of the RZ/G2L and DRAM, and in the destination for connection (power supply or GND)?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.2.8	
88	DDR3L SDRAM	Have the restrictions described in this guideline been applied to pin swapping of the CA and DQ pins when targeted devices are connected to DDR3L SDRAM?	Y	Y	Y	Y	Y	Y	—	—	—	4	4.2.9	
89	DDR4 SDRAM	Have the restrictions described in this guideline been applied to pin swapping of the CA and DQ pins when targeted devices are connected to DDR4 SDRAM?	Y	Y	Y	Y	Y	Y	Y	Y	—	4	4.2.10	
90	LPDDR4 SDRAM	Have the restrictions described in this guideline been applied to pin swapping of the CA and DQ pins when targeted devices are connected to LPDDR4 SDRAM?	—	—	—	—	—	—	Y	—	—	4	4.2.11 4.2.12	
91	LPDDR4/DDR4/DDR3L SDRAM	Has the power supply sequence of the DRAM been applied when the MPU is connected to the DRAM?	Y	Y	Y	Y	Y	Y	Y	Y	—	4	4.2.13 4.2.14 4.2.15 4.2.16	
92	High-speed serial IF	Does the design of the high-speed serial interface follow the restrictions and recommendations described in the guidelines?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.1	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
93	High-speed serial IF	Did you check the accuracy and the temperature coefficients of the components for connection to the high-speed serial interface?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.1	
94	High-speed serial IF	Is a coupling capacitor inserted for the transmission-side signal line of the high-speed serial interface?	—	—	—	—	—	—	Y	—	—	4	4.5.1	
95	High-speed serial IF	Did you include the restrictions and recommendations for the high-speed serial interface signal described in the guidelines in the circuit diagram?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.3	
96	High-speed serial IF	If you add pads to the signal traces to observe signals, is the circuit designed so that it does not degrade the signal quality?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.7	
97	High-speed serial IF	If the signal observation points are different from the end of the trace, have you run simulations to verify the signal quality and see the difference?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.7	
98	High-speed serial IF	Did you take appropriate measures against signal ESD and noise? Additionally, did you include instructions for the placement of these countermeasure components on the PCB in the circuit diagram?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.8	
99	USB	Is the overcurrent input level-shifted appropriate level?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.9.1	
100	USB	Is the resistor divider inserted in the VBUS input?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.9.1	
101	USB	Is the VBUS enable for the USB power circuit active high?	Y	Y	Y	Y	Y	Y	Y	Y	Y	4	4.9.2	
102	eMMC	Did you check the speed grade of the eMMC to be connected?	Y	Y	Y	Y	Y	Y	Y	Y	—	5	5.11	
103	eMMC	Did you confirm that the external pulling up and down of the eMMC signal lines does not violate the eMMC standard?	Y	Y	Y	Y	Y	Y	Y	Y	—	5	5.11.2	
104	eMMC	If the eMMC is set as the boot device, did you confirm that resetting of the eMMC was released before the start of booting up the targeted devices?	Y	Y	Y	Y	Y	Y	Y	Y	—	5	5.11.2	
105	SPI Multi I/O I/F	Did you confirm that the connection of the QSPI flash memory and HyperFlash memory (Target: RZ/G2L, RZ/G2LC, and RZ/V2L) is correct?	Y	Y	Y	Y	Y	Y	—	—	Y	5	5.13.1	
106	SPI Multi I/O I/F	Is the QSPIdx_SSx signal being pulled up to the 1.8 or 3.3-V supply?	Y	Y	Y	Y	Y	Y	—	—	Y	5	5.13.1	
107	SPI Multi I/O I/F	Are the CS#, INT#, and RESET# signals of HyperFlash memory being pulled up to the 1.8-V supply?	Y	Y	Y	—	—	—	—	—	—	5	5.13.1	
108	xSPI	Did you confirm that the connection of the QSPI flash memory and OctaRAM is correct?	—	—	—	—	—	—	Y	Y	—	5	5.13.2	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
109	xSPI	Is the QSPI CS# signal being pulled up to the 1.8 or 3.3-V supply?	—	—	—	—	—	—	Y	Y	—	5	5.13.2	
110	SDHI IF	Did you confirm that the destination for pulling up the CD and WP signals of the SD card interface is the system power supply (3.3 V)?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.13.3	
111	SDHI IF	Did you confirm that the destination for pulling up the signals (other than CD and WP) of the SD card interface is the SDHI IO power supply?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.14.2	
112	JTAG	Did you confirm the pull-up/pull-down processing of each signal?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.16	
113	RGMII, MII	Is the connection to the Ethernet PHY properly performed with reference to the contents of the application notes?	Y	Y	Y	Y	Y	Y	Y	Y	—	5	5.15	
114	I2C	Is the internal pull-up of the LSI being used to pull the I2C signal lines up?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.17	
115	I2C	Did you confirm that the I2C with an LVTTL-type buffer being pulled up when 5.0-V is applied?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.17	
116	I2C	Is the I2C of an open-drain type buffer being pulled up with 3.3-V?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.17	
117	I2C	When the IO power for targeted devices is not turned on, has the power supply for the destination for pulling the I2C signal lines up being turned on been avoided?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.17	
118	I2C	Has any slave address conflict between the I2C device been avoided? Did you include the slave addresses in the circuit diagram as a supplement for software design and so on?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.17.2	
119	SPI/RSPI	Is the signal connection between targeted devices and SPI device correct?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.18	
120	SCIF	Have you decided whether to use an external or internal SCIF clock? If you chose to use an external SCIF clock, is the clock at an appropriate frequency input?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.18.1	
121	AUDIO AOUT	If you are using aluminum electrolytic capacitors as coupling capacitors for audio analog output, is the polarity correct?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.19.1	
122	Others	Is the handling of unused pins of targeted devices in accord with the statements on the handling of unused pins in the hardware manual?	Y	Y	Y	—	—	—	—	—	—	5	5.1	
123	Others	As well as targeted devices, is the handling of unused pins of peripheral devices in accord with the statements on the handling of unused pins in the hardware manual?	Y	Y	Y	—	—	—	—	—	—	5	5.1	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
124	Others	Did you provide circuits, such as damping and parallel termination, as countermeasures on circuits for interfaces where signals may undershoot or overshoot?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.3	
125	Others	Did you consider the risk of interfaces where signals may undershoot or overshoot by checking the component specifications and simulating transmission?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.3	
126	Others	Did you confirm that there is no problem with the voltage of all the signals connected to targeted devices?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.4	
127	Others	Did you confirm sufficient AC and DC margins for the connections between targeted devices and peripheral devices?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.5	
128	Others	Did you provide circuits as countermeasures on connections between targeted devices and peripheral devices for which AC and DC margins may be insufficient?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.5	
129	Others	Did you check all internal pull-up and pull-down resistors of targeted devices and peripheral devices, and apply measures in the form of external circuits to prevent the generation of intermediate potentials due to contention between pulling up and down?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.6	
130	Others	For relatively high-speed parallel IO interfaces such as QSPI and VIN/VOUT, did you include instructions on pattern design in the circuit diagram, such as instructions regarding equal lengths and delays, and stating the wiring layers?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.8	
131	Others	For relatively high-speed parallel IO interfaces such as QSPI and VIN/VOUT, did you confirm that there is no problem with the signal quality by simulating transmission?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.8	
132	Others	When connecting a relatively high-speed parallel IO interfaces such as QSPI and VIN/VOUT through a connector, did you prepare a sufficient number of ground pins to secure the return path?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.8	
133	Others	When targeted devices and peripheral devices are connected, did you confirm that Hi-Z input does not occur even in specific situations such as resets, and that there will be no problems even if Hi-Z input does occur?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.9	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
134	Others	When targeted devices and peripheral devices are connected, did you confirm that output signals are not directly connected even in specific situations such as resets?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.9	
135	Others	Is the polarity of the aluminum electrolytic capacitors used in the power supply circuits and peripheral circuits correct?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.20	
136	Others	In a circuit configuration where power is partially turned on to operate the board, such as EEPROM programming, has application of the high level to devices that are not turned on, such as targeted devices, been avoided?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.21	
137	Others	Are the connectors correctly arranged in terms of male and female matching?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.22	
138	Others	Are the pin 1 positions of the connectors correct?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.22	
139	Others	Did you include a pattern diagram in the circuit diagram to specify the positions and arrangements of pin 1 of each of the connectors?	Y	Y	Y	Y	Y	Y	Y	Y	Y	6	5.22	
140	Others	When the RZ/G2L is turned off, have you ensured that an expansion board device connected through a connector does not output a high-level signal, and that pull-up resistors are not connected?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.22	
141	Others	Did you provide fail safes to prevent the reverse insertion of connectors?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.22	
142	Others	Does the circuit that has been created match the revision of targeted devices to be installed?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.23	
143	Others	If the circuit is an adaptation of a previous design, did you review the circuit configuration and the revision of the installed device, and confirm which parts of the circuit raise no problem in being used as is?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.24	
144	Others	Is the NC pin of targeted devices and peripheral devices properly handled?	—	—	—	Y	Y	—	—	—	—	5	5.2	
145	SCIF	Did you assign SCIF0_TXD and SCIF0_RXD signals to be used as SCIF download?	Y	Y	Y	Y	Y	—	Y	Y	Y	5	5.18	
146	Octa Memory Controller	Did you confirm that the connection of the OctaFlash and OctaRAM is correct?	—	—	—	—	—	Y	Y	—	—	5	5.12	

#	Item	Point to Check	Section in the Application Note for Reference									Link		Check
			G2L	G2LC	V2L	G2UL	Five	A3UL	G3S	G3E	A3M	Section	Sub section	
147	Power supply	Did you confirm that power domain "PVDD182533" is at 3.3 V when using pins belonging to power domain "PVDD182533" as GPIO?	Y	Y	Y	Y	Y	Y	Y	Y	—	5	5.6	
148	SPI Multi I/O I/F	Did you understand that using a QSPI flash memory with RESET pin was recommended?	Y	Y	Y	Y	Y	Y	Y	Y	Y	5	5.13	
149	Others	Did you understand the contents of this circuit design guideline, including restrictions and recommendations, before designing the PCB patterns?	Y	Y	Y	Y	Y	Y	Y	Y	Y	6	6.1 to 6.9	

REVISION HISTORY	RZ/G2L, RZ/G2LC, RZ/V2L, RZ/G2UL, RZ/Five, RZ/A3UL, RZ/G3S, RZ/A3M, and RZ/G3E PCB Design Checklist
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Rev.	Date	Description	
		Page	Summary
1.00	Sep. 30, 2021	—	First edition issued
1.01	Jan. 07, 2022	All	RZ/G2UL product is added. Chapter titles are updated.
		5 to 7	Figure 1.1 is updated.
		12	Figure 1.5 is modified.
		13	Figure 1.6 is modified.
		15	Figure 1.7 is modified.
		18	Table 2.2 is modified.
		39	Table 4.1 is modified.
		42	Figure 4.1 is modified.
		47	Figure 4.4 is modified.
		48	Figure 4.5 is modified.
		57	PRST_N is changed to PRST#.
		58	Figure name of Figure 5.1 is added.
		74	Table 5.6 is modified.
		75	Table 5.7 is modified.
		87	Section 5.26 is added.
		88	Section 5.27 is added.
		109 to 118	Section 7 is updated.
1.02	Feb. 25, 2022	All	RZ/Five product is added.
1.03	Apr. 26, 2022	All	For Section 4.1 through 4.7, the topologies correspond to "2Rank" for DRAM rank or "2" for the number of DRAM connections are available
		14	For Figure 1.6, the DRAM connection is modified from 1 to 2.
		39	For Table 4.1, the maximum Number of Ranks is modified from 1 to 2.
		42	For Figure 4.1, the number of address terminal is modified.
		46	For Figure 4.4, the DRAM connection is modified from 1 to 2.
		48	For Figure 4.5, the DRAM connection is modified from 1 to 2.
1.04	June 10, 2022	63	For Section 5.5, the description involved in pull-up or -down resistor values is modified.
		All	RZ/A3UL product is added.
		All	RZ/G2UL Group User's Manual: Hardware was added as a reference.
		All	RZ/A3UL Group User's Manual: Hardware was added as a reference.
		72	Figure 5.3 is modified for the connection of a SPI flash memory (data width = 8bits).
		73	Figure 5.4 is modified for the connection of a HyperFlash memory (data width = 8bits).
		91	Section 5.28 "Octa Memory Controller" is added.
1.10	Dec. 21, 2022	112 to 122	Section 7 is updated.
		5 to 7	For Figure 1.1 (a), Figure 1.1 (b) and Figure 1.1 (c), the pin name of JTAG ICE are modified from "TRST#" to "nRESET".
		57	For Section 4.16, pin handling is added for "USBn_OVRCUR (n = 0, 1)" pin when not in use. For Figure 4.7, overcurrent input of the USB is modified.
		71	For Section 5.10, pull-up connection of CLK signal is not required for eMMC interface circuit.

Rev.	Date	Description	
		Page	Summary
1.10	Dec. 21, 2022	77	For Section 5.15, pin handling is added for "DEBUGEN" pin for JTAG circuit.
		89	For Section 5.26, pin handling is removed for "IC" pin. Target products are restricted to RZ/G2UL and RZ/Five.
		92	For Section 5.28, document is added for reference.
		93	Section 5.29 "IO voltage level available for power domain "PVDD182533"" is added.
		114 to 124	Section 7 is updated.
1.11	Apr. 06, 2023	57	For Section 4.16 "Voltage for the overcurrent or VBUS Input of the USB", pin handling is updated for "USBn_OVRCUR (n = 0, 1)" pin when not in use.
		94	Section 5.30 "Selection of QSPI flash memory" is added
		115 to 125	Section 7 "Check List" is updated.
1.12	Oct. 31, 2023	16	For Section 2.1 "Voltage for Clock Input", the input voltage of the ET0/1_TXC/TX_CLK pin is changed from 1.8 V to 1.8/2.5/3.3 V for all products.
1.20	Nov. 06, 2023	All	RZ/G3S product is added.
		7	For Figure 1.1 (b) of Section 1.1 "Circuits for Generating PRST# Inputs", the part name of a PMIC is modified from "PMIC" to "RAA215300A2GNP#HA0".
		17	For Figure 1.6 of Section 1.6 "Making Reset Signals Open-Drain Output", the buffer types of the QSPI_RESET# and the SD0_RST# are modified from "3.3V output, open drain" to "3.3/1.8V output, open drain". For Figure 1.6 of Section 1.6 "Making Reset Signals Open-Drain Output", the buffer type of the DDR_RESET# is modified from "3.3V CMOS output" to "1.2/1.35V CMOS output".
		20	For Section 2.1 "Voltage for Clock Input", a crystal oscillator is added.
		22	For Table 2.2 of Section 2.3 "Accuracy and Deviation of the Input Clocks", the XIN is added for the clock input.
		35	For Section 3.4 "Noise Filter Circuits for Power Supplies", the description "Although the hardware manuals or guidelines do not include recommended circuits for the CPG PLL power supply circuit, this circuits indicate that the circuit is noise-sensitive." is removed. description and added a crystal oscillator. The description "filters are recommended in the guidelines" changed to "filters are recommended in the evaluation board kits or guidelines"
		48	For Section 4.4 "Command and Address Wiring Topologies for Connecting with DRAM", the section name is changed to "Wiring Topologies for Connecting with DRAM", The description "Command and Address wiring connection between target device and DRAM is under below." is changed to "Command and address wiring connection between a target device and DRAM is only supported point-to-point on our reference board." The description "Data wiring connection between a target device and DRAM is shown below." is added. The description "If you support wiring connection other than that of our reference board, please refer to the PCB verification guide for DRAM and perform simulation by yourself. Even if you support wiring connection of our reference board, it is strongly recommended to perform simulation because a PCB structure, material, and target DRAM are not exactly the same" is added.
		61	For Table 4.3 of Section 4.14 "PCB Design Guide for High-Speed Serial Interfaces", the guideline name is changed from "PCB design guidelines for MIPI-CSI, NIPI-DSI, and USB2.0" to "PCB design guidelines for MIPI-CSI, NIPI-DSI, USB2.0, and PCI Express Gen2".
		68	For Section 4.21 "USB VBUSEN", the description "refer to Figure 4.7 to make the connection" is removed. The description "It is shown a design example of an evaluation board manufactured by Renesas Electronics." is added.
		77	For Section 5.8 "Interrupt Signals", the description "Partially shared" is changed to "Dedicated" for Table 5.1 Specification of the NMI Signal.
		82	For Section 5.11 "SPI Multi I/O Interface", the description "serial flash, OctaFlash™" is changed to "Quad/Octal-SPI flash memory". Figure "Connection of SPI Flash Memory" is modified.
		93	For Section 5.19 "Master and Slave Settings of SPI", section name is modified.

Rev.	Date	Description	
		Page	Summary
1.20	Nov. 06, 2023	127 to 137	Section 7 "Check List" is updated.
1.21	Mar. 18, 2024	6	For Figure 1.1 (a) of Section 1.1 "Circuits for Generating PRST# Inputs", the diagram is modified.
		7	For Figure 1.1 (b) of Section 1.1 "Circuits for Generating PRST# Inputs", the diagram is modified.
		8	For Figure 1.1 (c) of Section 1.1 "Circuits for Generating PRST# Inputs", the diagram is modified.
		9	For Figure 1.1 (d) of Section 1.1 "Circuits for Generating PRST# Inputs", the diagram is modified.
		14	For Figure 1.5 (a) of Section 1.5 "Circuits for Generating TRST# from JTAG-ICE", the diagram is modified.
		102	For Section 5.28 "Notes on SCIF0 Signal Connection", it is not mandatory to be supported for RZ/A3UL product
		137	For Section 7 "Check List", the support for #150 SCIF is not mandatory for RZ/A3UL product.
2.00	July 29, 2024	All	Restructured the chapters of the document and reorganized some sentences, figures, and tables to make them easier to read. Basically, the content of the document remains unchanged.
		64	Section 5.6 is modified.
2.10	Apr. 25, 2025	All	RZ/A3M product is added.
		10	Figure 1.1(d) is modified.
		—	Section 1.6 is deleted.
		18	Section 2.2 is modified.
		39	Table 4.3 is modified.
		40	Section 4.2.4 is modified.
		41	Section 4.2.5 is modified.
		45	Figure 4.4(b) is modified.
		47	Section 4.2.10 is modified.
		50	Section "Power-on Sequence for DDR3L and DDR4" is divided into Section 4.2.12 and Section 4.2.13.
		74	Section 5.13.2 is modified.
		80	Table 5.2 is modified.
		82	Section 5.16.2 is added.
		95	Section 5.25 is added.
		115 to 125	Section 7 "Check List" is updated.
2.20	June 25, 2025	All	RZ/G3E product is added.
		19	Table 2.1 is modified.
		38, 39	Section 3.12 is added.
		41	Table 4.2 is modified.
		43	Figure 4.1 is modified.
		44	Section 4.2.5 is modified.
		53	Section 4.2.12 is added.
		54	Section 4.2.16 is added.
		63	Section 4.9.3 is added.
		78	Figure 5.7 is modified.
		119 to 130	Section 7 "Check List" is updated.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

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