Design Guide

PCB Design Guidelines for MIPI CSI-2, MIPI DSI, and USB2.0

RZ/G2L LFBGA 15.0/21.0sq
RZ/G2LC LFBGA 13.0sq
RZ/G2UL LFBGA 13.0sq
RZ/V2L LFBGA 15.0/21.0sq
RZ/Five LFBGA 13.0/11.0sq
RZ/A3UL LFBGA 13.0sq

Renesas Electronics
www.renesas.com

Rev.2.00 Feb. 2026

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Table of Contents

1. Guidelines for MIPI CSI-2 and MIPI DSI (RZ/G2L, RZ/G2LC, RZ/G2UL (MIPI DSI not supported), RZ/V2L, and RZ/A3UL (MIPI DSI not supported))

1.1 Guidelines for Signal Line Topology (Tx, Rx)

Refer to the MIPI D-PHY specification ver.2.1 regarding the transmitter and receiver specifications.

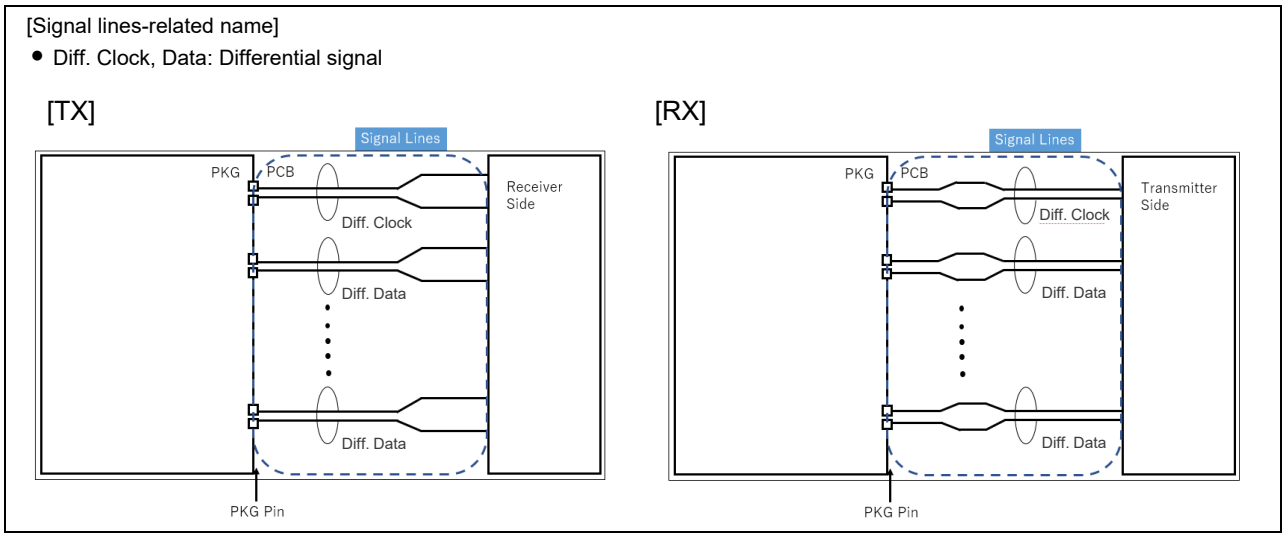

Figure 1.1 Signal Line Topology of MIPI CSI-2 and MIPI DSI

Table 1.1 Guidelines for PCB Signal Lines of MIPI CSI-2 and MIPI DSI

Items		Guidelines	Refer to	Notes
Line impedance		√: Differential 100Ω ± 20%	—	—
Line length difference	Between differential clock and differential data	√: Same length as much as possible √: Line length is as short as possible	—	—
	Between positive clock and negative clock		—	—
Line bending		Recommended: External angle 45° (Prohibited: >45°)	—	—
Line layer Number of vias	Between differential clock and differential data	Same layer Note: Recommended: Top layer without any vias	—	—
	Between positive and negative	Same via number (number is as few as possible)		
Line spacing	Between positive clock and negative clock	S (min. of PCB design criterion)	**Figure 1.2** (1)	1
	Between diffential and next diffential	≥ 3S Note: When there are no GND shields	**Figure 1.3** (6)	
	Between differential and GND shields	≥ S Note: Place GND shields on both sides of differential pair	**Figure 1.2** (2)	
	Between differential and other high speed / low speed signal	≥ 3S Note: It is unnecessary when there are GND shields	—	
	Between differential and continuous ground plane	≥ S	**Figure 1.2** (3)	
Line width		≥ S	**Figure 1.2** (4)	
Return path		√: Place a continuous ground plane under differential pair	**Figure 1.2** (5)	—
		Place GND through-hole next to signal through-hole Place GND vias symmetrically next to differential	—	—

Note 1. These sizes are for reference only. They can be changed to actual values on the designer's side.

1.2 Guidelines for PCB Signal Lines

Design with priority √ items. However, clock-data skew could be relaxed depending on the timing spec. Refer to the MIPI D-PHY specification ver.2.1 for details.

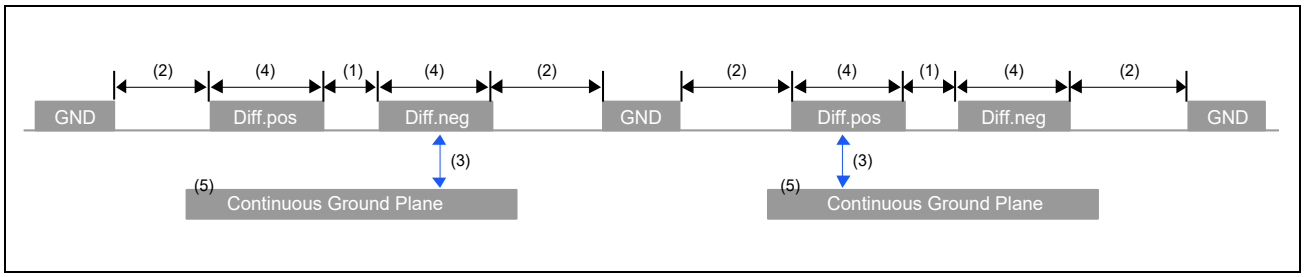

Figure 1.2 Signal Lines Example 1

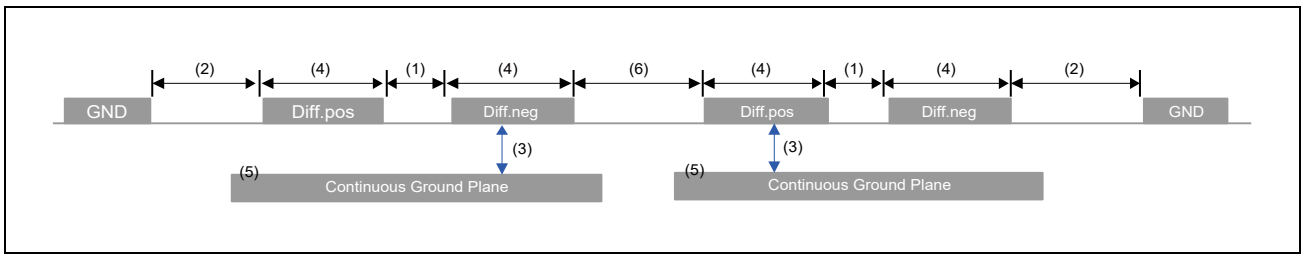

Figure 1.3 Signal Lines Example 2

1.3 Guidelines for Power Line Topology (Tx, Rx)

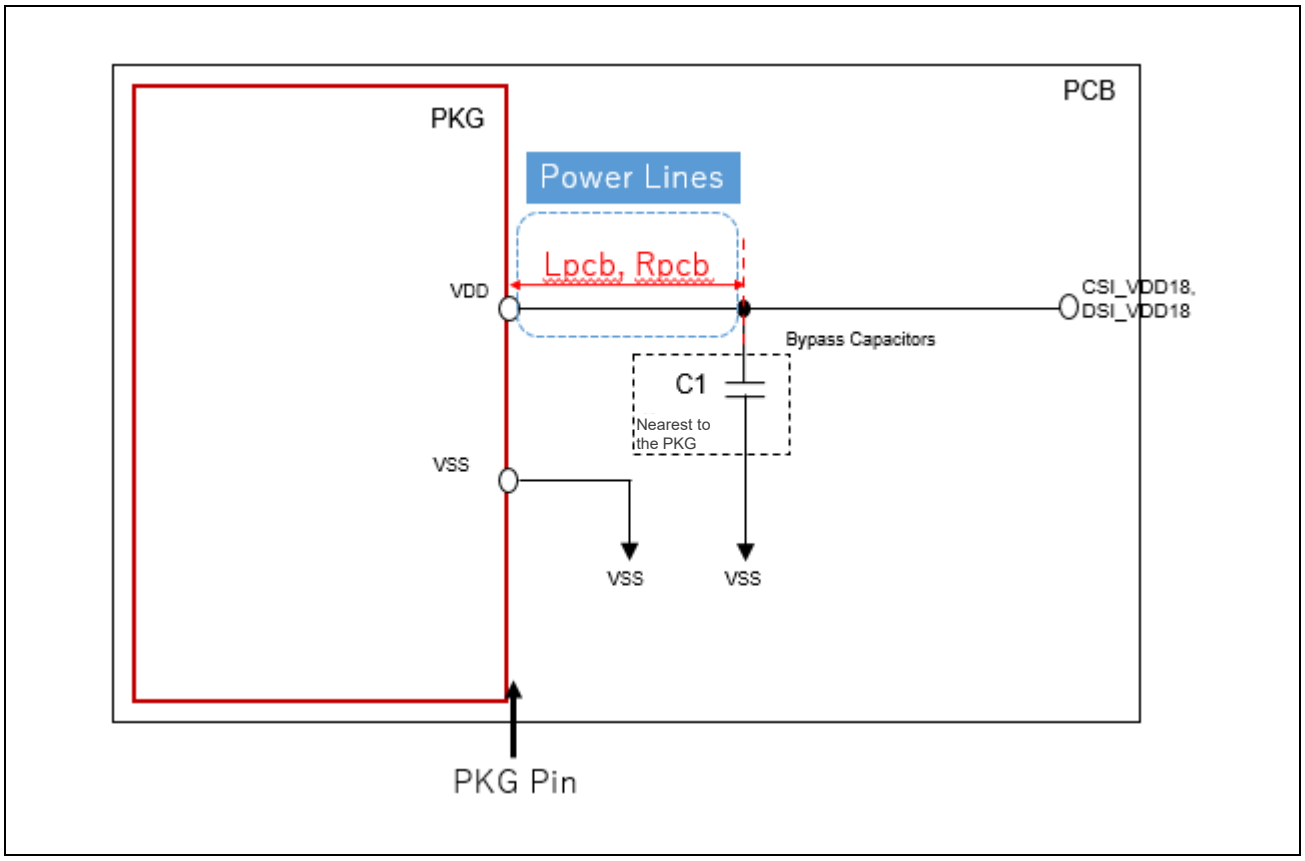

Figure 1.4 Power Line Topology of MIPI CSI-2 and MIPI DSI

1.4 Guidelines for PCB Power Lines

Supply the power from DSI_VDD18 and CSI_VDD18 with the ground as the common VSS plane of the PCB.

Table 1.2 Guidelines for PCB Power Lines of MIPI CSI-2 and MIPI DSI

Items	TX	RX	Notes
Rpcb	≤ 30mΩ	≤ 30mΩ	—
Lpcb	≤ 2.8 nH/5 ch	≤ 2.8 nH/5 ch	1, 2
C1 (nearest to the chip)	0.1 µF	0.1 µF	3

Note 1. The power line inductance from the PKG pins to C1 should be as small as possible.
Refer to **Appendix A** (**Concept of Loop Inductance**).

Note 2. The value of Lpcb does not include the component of C1.

Note 3. Place C1 closer to the PKG pins to prevent the ripple noise caused by transient current.
Place a bypass capacitor between the respective power supply planes and solder balls.

2. Guidelines for USB2.0

2.1 Guidelines for PCB Signal Lines

Table 2.1 Guidelines for PCB Signal Lines of USB2.0

Items		Guidelines	Refer to	Notes
Line impedance		√: Differential 90Ω ± 10% Single-end 45Ω ± 10%	—	—
Line length difference	Between positive data and negative data	√: Same length as much as possible	—	—
		√: Line length is as short as possible		—
Line bending		Recommended : External angle 45° (Prohibited: >45°)	—	—
Line layer Number of vias	Between positive data and negative data	Same layer	—	—
		Note: Recommended: Top layer without any vias Same via number (number is as few as possible)		—
Line width	Between positive data and negative data	√: Same width as much as possible	**Figure 1.2** (4)	1
Return path		√: Place a continuous ground plane under differential pair	**Figure 1.2** (5)	1
		Place GND through-hole next to signal through-hole Place GND vias symmetrically next to differential	—	—

Note: Do not use SSC (Spread Spectrum Clock) as the reference clock.

Note 1. Refer to **Figure 1.2** in **section 1.2**.

2.2 Guidelines for Power Lines

The SoC has two power rails for the USB 2.0 interface:

- USB_VDD33
- USB_VDD18

Figure 2.1 shows configurations of decoupling capacitors in the case of one port. The values of the capacitors and their configurations are examples of recommended values. Change the values and configurations according to the noise frequency and noise level.

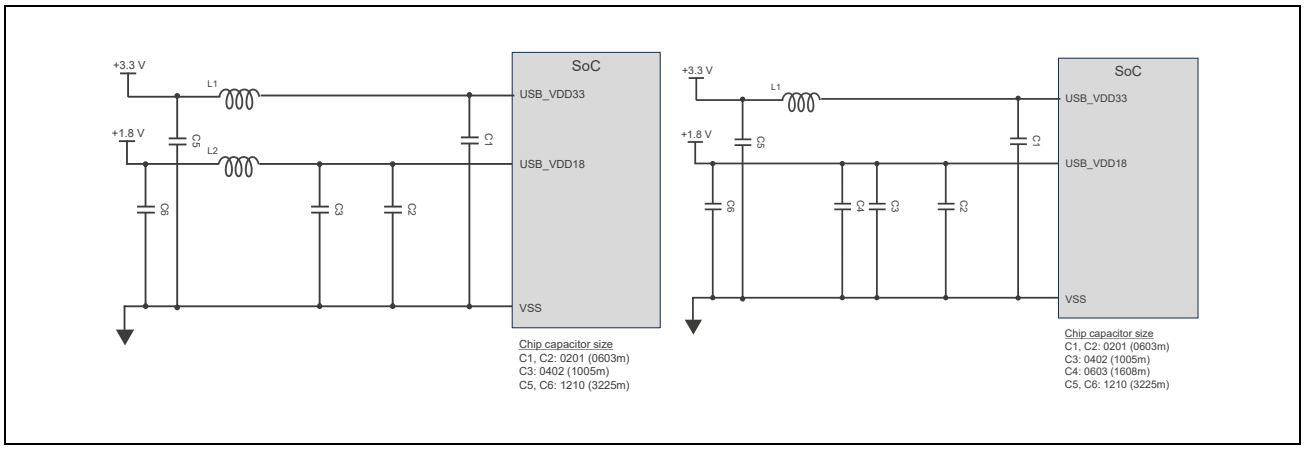

Figure 2.1 Decoupling Capacitors in the Case of One Port (Left: With Separation Inductor, Right: Without Separation Inductor)

Table 2.2 lists the capacitor and inductor values for the respective parts shown in **Figure 2.1**.

Table 2.2 External Parts for PCB Power Lines

Designator	Value	Tolerance	Voltage Rating*1	Size
C1, C2	0.1 µF	±25%	Above 8 V	0201 (0603m)
C3	2.2 µF	±25%	Above 8 V	0402 (1005m)
C4*2	10 µF	±25%	Above 8 V	0603 (1608m)
C5, C6*3	47 µF	±25%	Above 8 V	1210 (3225m)
L1*4	600Ω	±20%	—	0402 (1005m)
L2*2 *5	1 µH	±20%	—	0603 (1608m)

Note 1. It is recommended that the voltage rating be no less than three times the value of the supply voltage.

Note 2. Separate USB_VDD18 from the digital power supply by using an inductor or ferrite, or by using an additional ceramic capacitor. In addition, do NOT locate the noise source near GND.

Note 3. The electrolytic capacitor

Note 4. The ferrite bead is optional and can be placed further away from the power supply pin.

Note 5. The DC resistor is recommended to be below 150mΩ.

Critical PCB design considerations are outlined below.

Digital Power Supply

1. Populate decoupling capacitors between each power supply and GND for safe operation. In addition, populate ceramic capacitors near the SoC. The electrolytic capacitor may be placed far from the SoC.
2. USB_VDD33 should be connected to a 3.3-V digital power supply pattern.
3. The wiring impedance of the digital power supply needs to be as small as possible.

GND Wiring

1. The wiring impedance of GND needs to be as small as possible.
2. The GND plane must NOT be close to other signal wiring.

2.3 Reference Resistor

For calibration, the USB PHY requires a calibration resistor to be connected to the USB_RREF pin.

Figure 2.2 shows a configuration of this resistor.

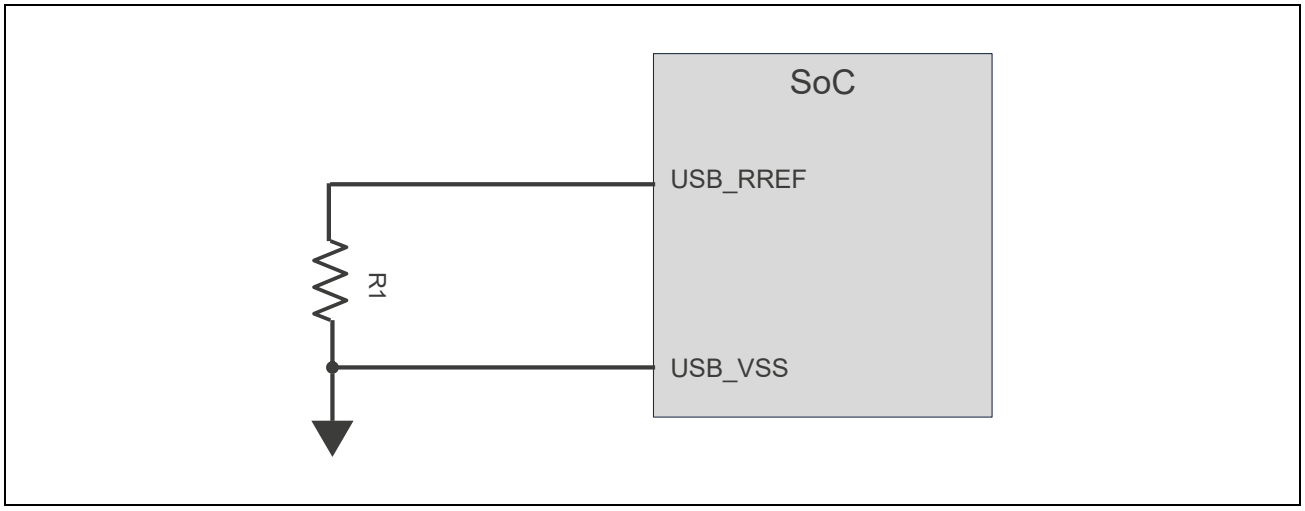

Figure 2.2 Reference Resistor

Table 2.3 lists the resistor value for the part shown in **Figure 2.2**.

Table 2.3 External Parts

Designator	Value	Tolerance	Size
R1	1.8kΩ	±1%	0201 (0603m)

Critical PCB design considerations are outlined below.

1. A 1.8-kΩ reference resistor should be located between USB_RREF and GND.
2. The reference resistor should be located close to the SoC, and the wiring should be designed with the resistance below 0.5Ω.
3. The reference resistor should NOT be located in parallel with the capacitor to avoid affecting the calibration.
4. The reference resistor and wiring must NOT be placed adjacent to or intersect with other signal wiring.
5. The layer under the reference resistor and wiring should be the GND plane to protect noise contamination.

2.4 Processing of Unused Terminals

1. DP/DM should be connected to GND through a 10-kΩ resistor.
2. USB_RREF should be left open.
3. USB_VDD18 should be connected to a 1.8-V power supply.*[1] However, it is not necessary to separate the digital power supply from the analog power supply.
4. USB_VDD33 should be connected to GND.*[2]
5. Assert the internal signal whose bit name is dirpd*[3], and power down the core VDD via this internal signal.

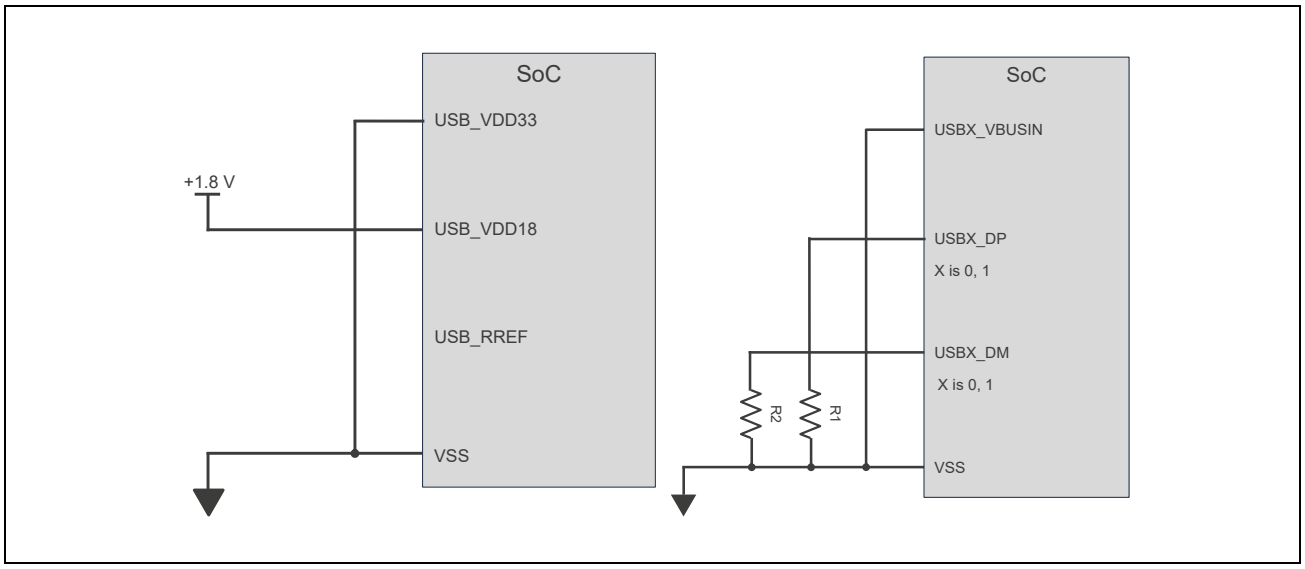

Figure 2.3 Configuration of External Parts

Note 1. Do NOT connect USB_VDD18 to GND, as this means that the internal circuit is floating and through current may occur.

Note 2. There is no problem even if the output of the external regulator that supplies voltage to USB_VDD33 is 0 V with the OFF setting. It is also possible to connect USB_VDD33 to a 3.3-V power supply. However, be careful because a current value of about 500 µA (Typ.) is generated regularly.

Note 3. Clamp VDD or GND when there is an internal input signal whose status is open except dirpd.

2.5 EMI/ESD Protection

Notes on EMI/ESD protection are described below.

- When EMI/ESD protection components such as a coil and a diode are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.
- By mounting EMI/ESD protection components, an inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. The components should be carefully evaluated and selected to ensure USB 2.0 High Speed compliance to avoid signal integrity issues.

Figure 2.4 shows an example connection when EMI/ESD protection components are used.

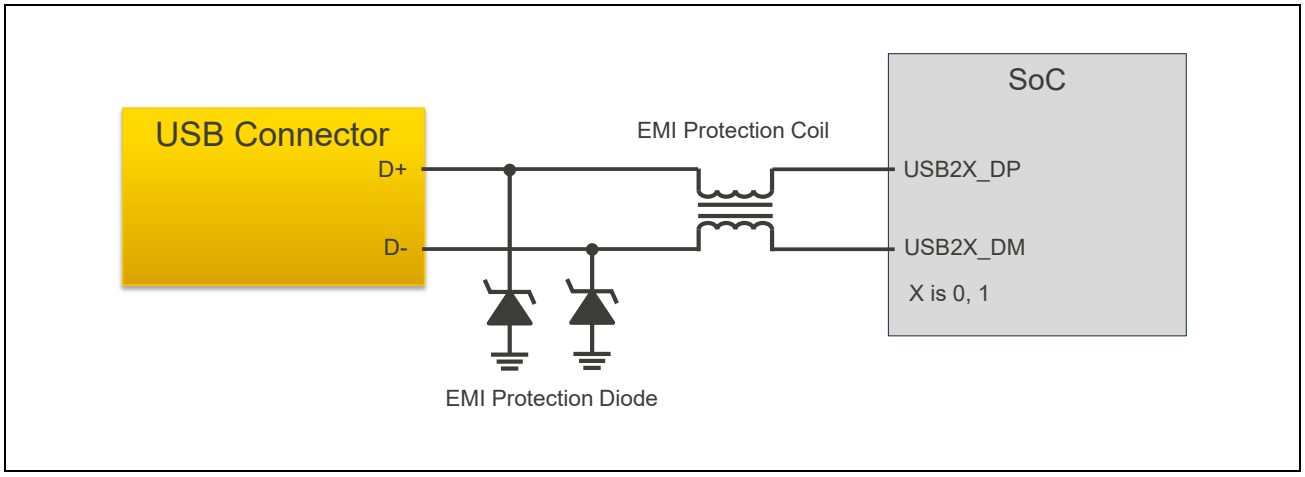

Figure 2.4 Connection Example when EMI/ESD Protection Components are Used

3. Guidelines for Modeling

Perform a simulation with a frequency range up to 10 GHz in the case of extracting S parameters.

Appendix A Concept of Loop Inductance

The target inductance can be obtained by calculating the loop inductance from the VDD balls of the package to the VSS balls of the package taken as an ideal GND as shown in the figure below. In this case, include the equivalent series inductance (ESL) component of the bypass capacitor placed close to the LSI chip.

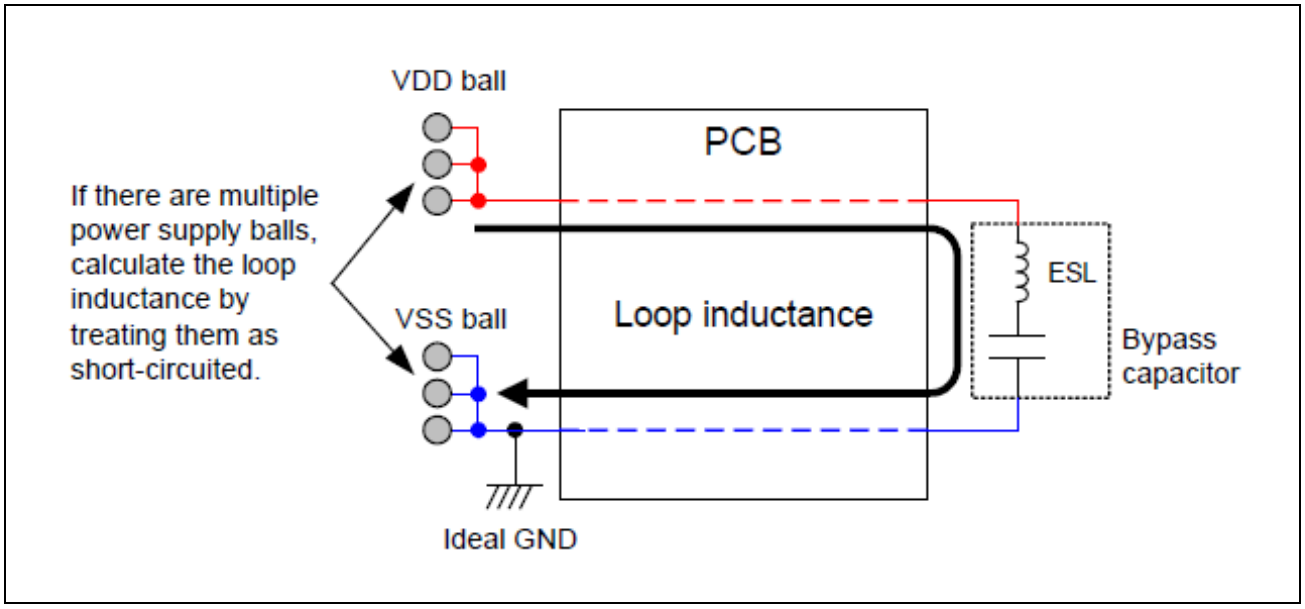

Figure A.1 Concept of Loop Inductance

REVISION HISTORY	RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL PCB Design Guidelines for MIPI CSI-2, MIPI DSI, and USB2.0

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 05, 2021	—	First edition issued
1.01	May 20, 2022	1, 10	Added RZ/Five
1.02	May 30, 2022	1, 5, 10	Added RZ/A3UL
1.10	Nov. 10, 2023	—	Added RZ/G3S
2.00	Feb. 16, 2026	All	Removed RZ/G3S and prepared the document separately. Restructured the sections of the document and reorganized some sentences, figures, and tables to make them easier to read. Basically, the content of the document remains unchanged.

RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL
PCB Design Guidelines for MIPI CSI-2, MIPI DSI, and USB2.0

Publication Date:	Rev.1.00	Oct. 05, 2021
	Rev.2.00	Feb. 16, 2026

Published by: Renesas Electronics Corporation

RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL
PCB Design Guidelines for MIPI CSI-2, MIPI DSI, and USB2.0

Renesas Electronics Corporation

R01AN5871EJ0200