

PCB Layout and Gate Drive Guidelines for Renesas Low-Voltage GaN Devices

Introduction

This application note describes the designing and implementation of Renesas' low-voltage (LV) GaN devices.

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1. GaN FET Gate Drive Control

1.1 GaN FET Gate Voltage Ratings and Threshold Voltage

The gate drive operating voltage of the GaN FETs is quite different from that of the Si-FETs. Renesas' low voltage GaN products typically have gate to source voltage ratings between **-4V** and **+6V**. Therefore, when powering on, the voltage should not exceed the V_{gs} maximum voltage 6V as shown in Figure 1 point 1. And when powering off, the voltage should not drop lower than **-4V** as shown in point 2. In addition, care must be taken to prevent GaN FETs from accidentally turning on due to ringing. The ringing can cause the voltage to exceed the threshold voltage as shown in point 3, turning the device on and causing a shoot-through.

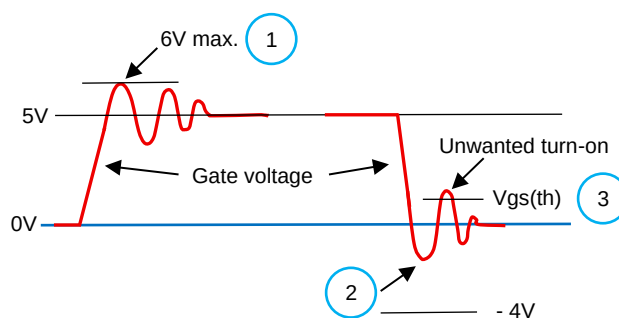


Figure 1. Gate Voltage and Threshold Voltage Ratings

1.2 Dual-Output Gate Driver

GaN FETs have very low threshold voltages, ranging from 0.8V–2V. This low voltage must be considered to ensure a good turn-off state. For optimal performance, it is recommended to use a dual-output gate driver such as the Renesas RRP68150 as shown in Figure 2. This provides one turn-on output and one turn-off output. The turn-off output is used to shut down the device through a low-impedance path.

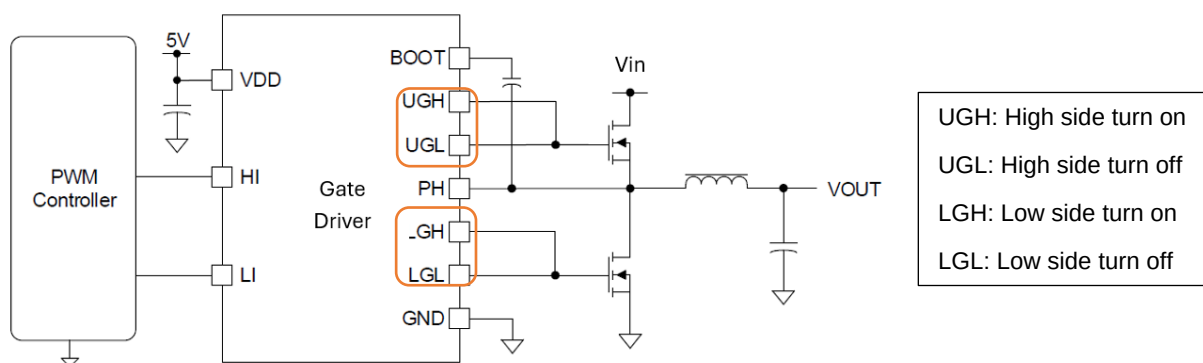


Figure 2. Dual-Output Gate Driver Turn Off/On States

1.3 Diode Avoidance in a Single Driver Output

Due to the low threshold voltages (0.8V min), we need to avoid using the circuit as shown in Figure 3. This circuit is commonly used to drive MOSFETs, but it is not suitable for GaN FETs. You'll find that the voltage drop across the diode is almost the same as the minimum threshold voltage. This means that if this circuit is used, the GaN FET may fail to turn off properly.

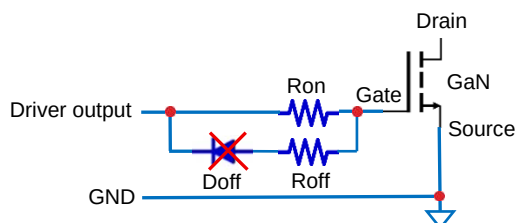


Figure 3. Circuit that Causes GaN FET Turn Off Failure

2. Parasitic Inductance Considerations

2.1 Overview

Low-voltage Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) enable high-frequency buck converters with unparalleled power density and efficiency. However, their ultra-fast switching transitions (di/dt and dv/dt) make them highly sensitive to layout induced parasitic elements. This document establishes strict layout guidelines to minimize high-frequency common source inductance, gate loop inductance and power loop inductance, ensuring safe operation, minimal voltage overshoot, and optimal thermal distribution.

2.2 Common Source Inductance

Common source inductance (L_{csi}) comes from PCB traces, package leads, vias, and bonding wires. It is a parasitic inductance that exists in the source path shared by the gate drive loop and the power current loop. In a synchronous buck converter, high side GaN switches at high current and high voltage at the same time. Common source inductance has a significant impact on it especially switching power loss. When the high side GaN Q1 is turned-on, the source current (I_s) increases, the inductor generates an induced voltage (V_s). This voltage counteracts the applied gate drive voltage (V_{drv}) and slows the rate of rise of the voltage between the gate and source (V_{gs}), and thereby, slowing the rate of rise of the source current. Finally, slower turn-on generates extra losses in the converter.

The following equation shows that the effective gate-source voltage $V_{gs(eff)}$ is reduced by the common source voltage (V_{Lcsi}) when the source current (I_s) begins to increase.

$$V_{gs(eff)} = V_g - V_{sw} - V_{Lcsi}$$

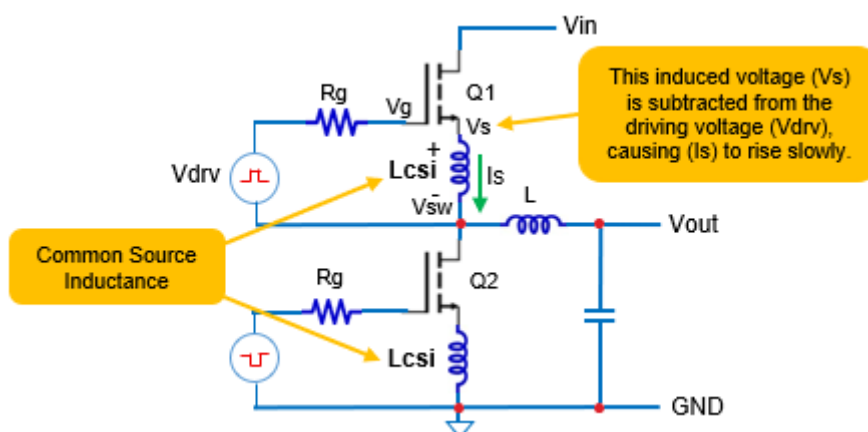


Figure 4. Common Source Inductance L_{csi} in a Buck Converter

2.3 Gate Loop Inductance

The gate loop inductance includes gate inductance (L_{gate}) and common source inductance (L_{csi}). These parasitic inductances along with the input gate capacitor (C_{gs}) can cause ringing in the gate signal, leading to gate voltage exceeding the threshold voltage and absolute maximum rating, resulting in incorrect turn-on / turn-off and potentially damaging GaN devices. Increasing the value of the gate resistor R_g can improve ringing and overshoot voltage, but it will also reduce switching speed and increase switching power loss. Therefore, to ensure low power loss and robust operation of the buck converters, the gate loop inductance must be minimized as much as possible.

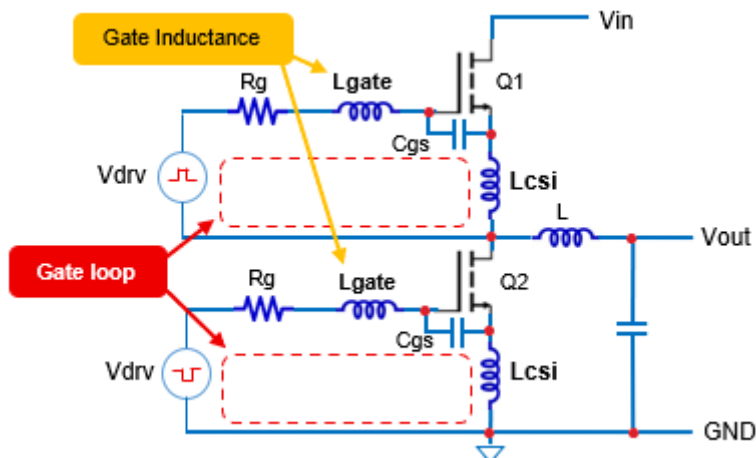


Figure 5. Gate Loop Inductance L_{gate} and L_{csi} in a Buck Converter

2.4 Power Loop Inductance

The power loop inductance consists of the GaN drain inductance (L_d), the common source inductance (L_{csi}), and parasitic inductance from input capacitors (L_{in}) and PCB traces. The impact of the power loop inductance, showing more ringing on the switch node voltage (V_{sw}) and gate signal (V_g). This ringing at the switch node increases the switching loss and deteriorates the EMI performance.

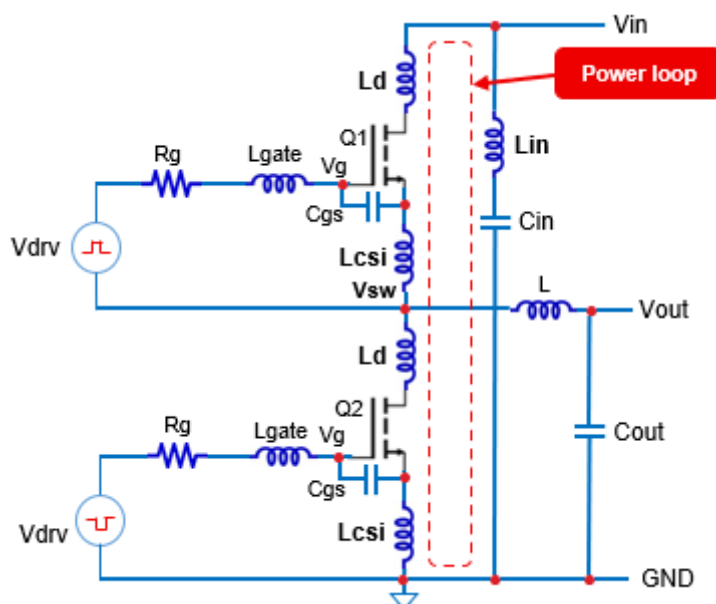


Figure 6. Power Loop Inductance L_{in} , L_d and L_{csi} in a Buck Converter

2.5 Measure Parasitic Inductance at Power Loop of PCB

There is a simple method to check for parasitic inductance in a PCB. Figure 7 (a) and (b) shows the equivalent RLC circuit of the buck converter and the switching waveform at Vsw node after high-side GaN Q1 is turned on. As there is Coss2 value and the resonant frequency fres1, use the formula in Figure 7 (c) to calculate the parasitic inductance Lloop.

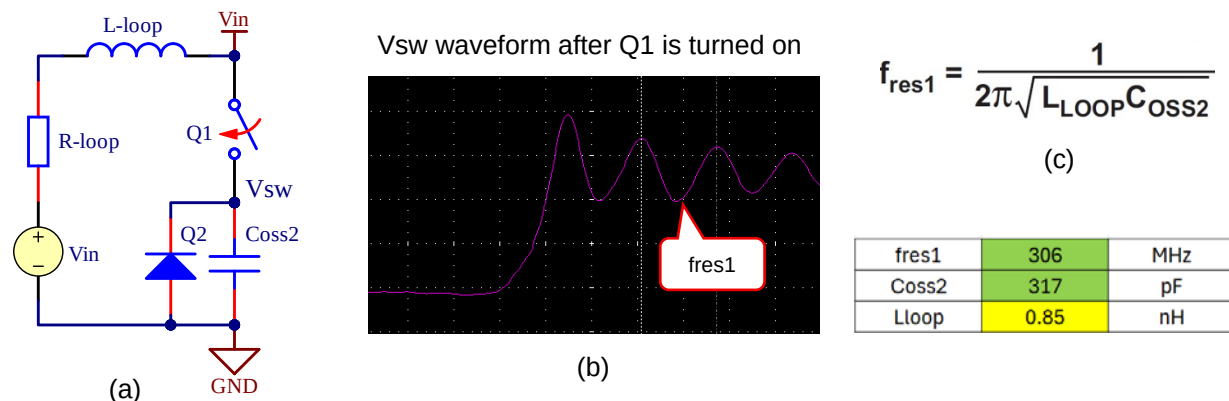


Figure 7. Measuring Parasitic Inductance at Power Loop of PCB

3. PCB Layout Optimization

Due to fast switching nature of GaN devices, minimizing parasitic inductance in the PCB layout is critical to ensure reliable operation, reduce EMI, and maximize the efficiency. Key strategies include.

3.1 Small Gate Loop

Gate driver, gate resistors and GaN devices should be placed as closed as possible to minimize the gate loop inductance and delay.

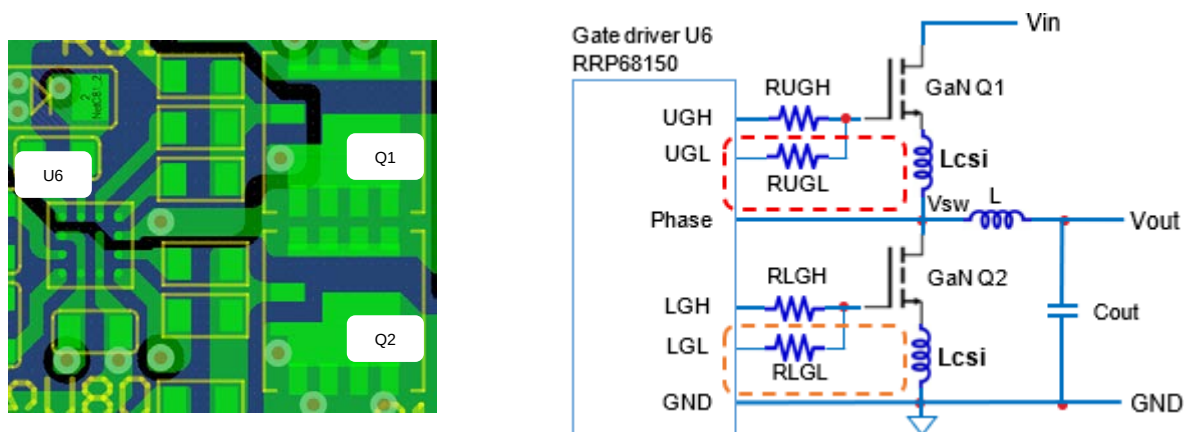


Figure 8. Minimizing the Gate Loop Inductance and Delay

3.2 Return Plane at the First Inner Layer

The copper polygons on layer 2 (first inner layer) are used as return planes. They should be located directly below the entire gate drive circuit and connected through vias to the top layer. These polygons can make the smallest gate loop inductance and help against noise interference.

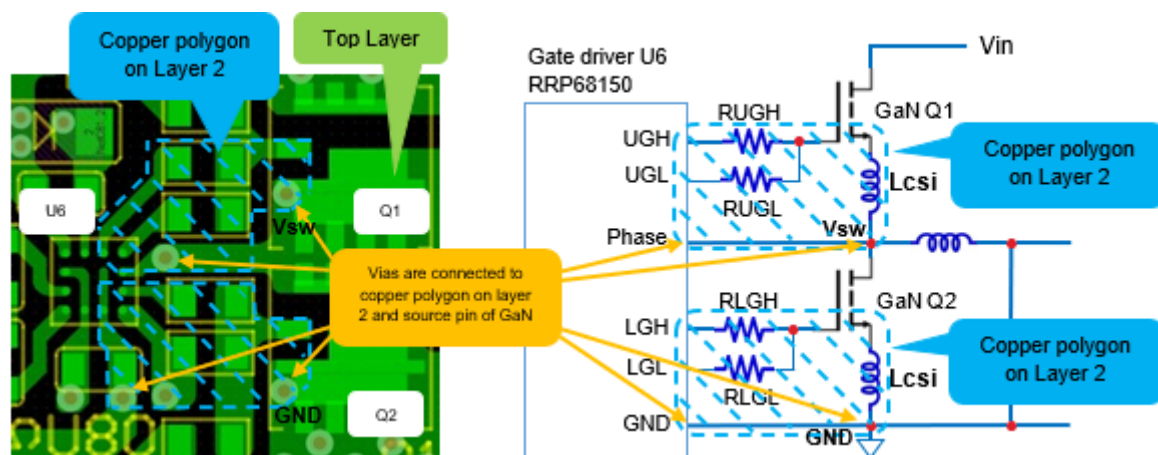


Figure 9. Copper Polygons

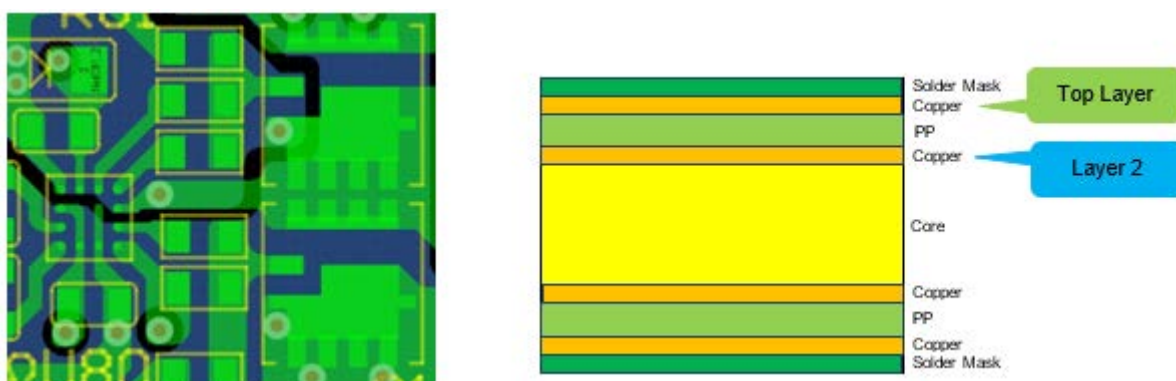


Figure 10. Layer 2 Drawing Example and PCB Structure Diagram

3.3 Parasitic Inductance and Magnetic Field Self-Cancellation

Parasitic inductance in the PCB can cause a high V_{ds} spikes in the low side GaN of the buck converter. When using a 4-layer board, it is recommended to place components on the top / bottom layer and use the first inner layer as the return path for the power ground. This achieves the shortest trace length and the **smallest loop area**, while also serving as a **magnetic field self-cancellation mechanism**, thereby reducing the parasitic inductance of the PCB. Input high frequency decoupling capacitor C_{in} (typically multi-layer ceramic capacitors) must be placed directly across the power loop and as close as possible to the half bridge to supply the high frequency switching currents.

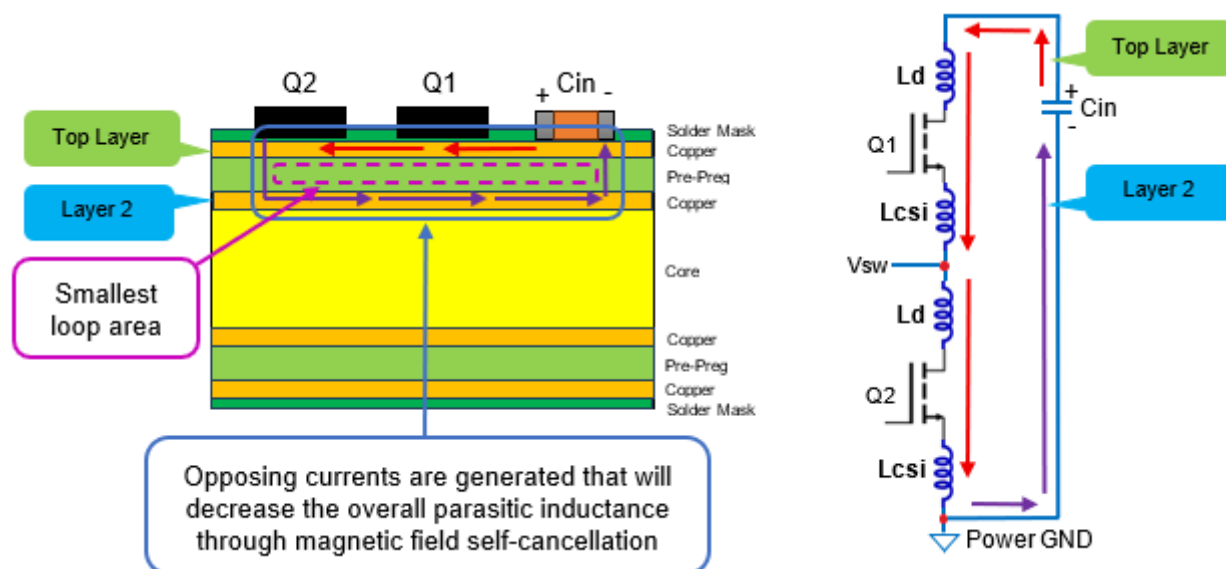


Figure 11. Magnetic Field Self-Cancellation and Current Loop

3.4 Pre-Preg Thickness

The thickness of the Pre-Preg directly affects the parasitic inductance. The larger the PP value, the larger the inductance. This is a form of an inductance formula (often used in electromagnetics), especially for a rectangular conductor or magnetic structure.

$$L = \frac{\mu_0 \cdot \text{length} \cdot \text{thickness}}{\text{width}}$$

This formula shows that as the thickness decreases, the inductance L also decreases. Therefore, it is advisable to choose circuit boards with a smaller PP value to obtain the lowest parasitic inductance.

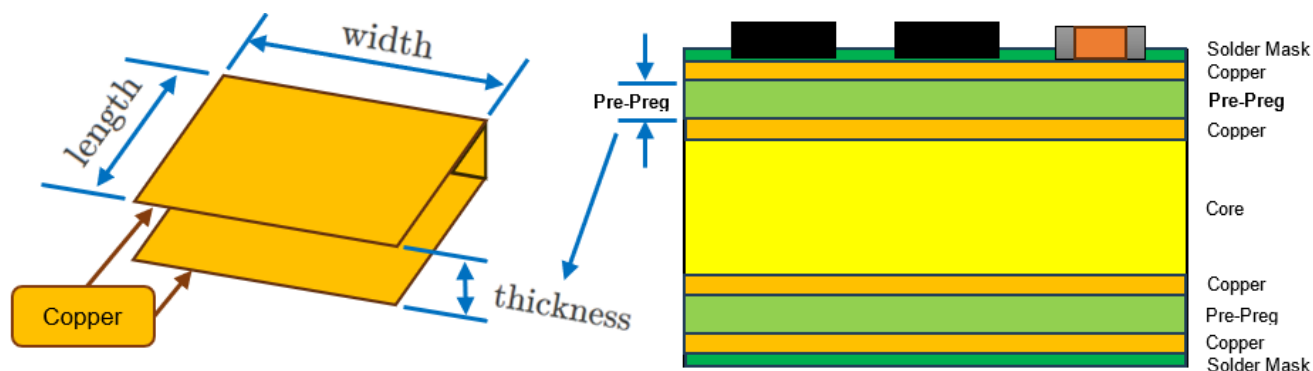


Figure 12. Pre-Preg Thickness

4. Layout Considerations for GaN Packages

4.1 FCLGA 3.3 × 3.3 mm Package

Renesas' gate driver RRP68150 and FCLGA 3.3 × 3.3 mm package LV-GaN are easy to implement in PCB layout. They can be put on the same layer, and the gate drive loop is small. Also, the power loop needs to be separated from the gate drive loop to avoid interference with each other (see Figure 13).

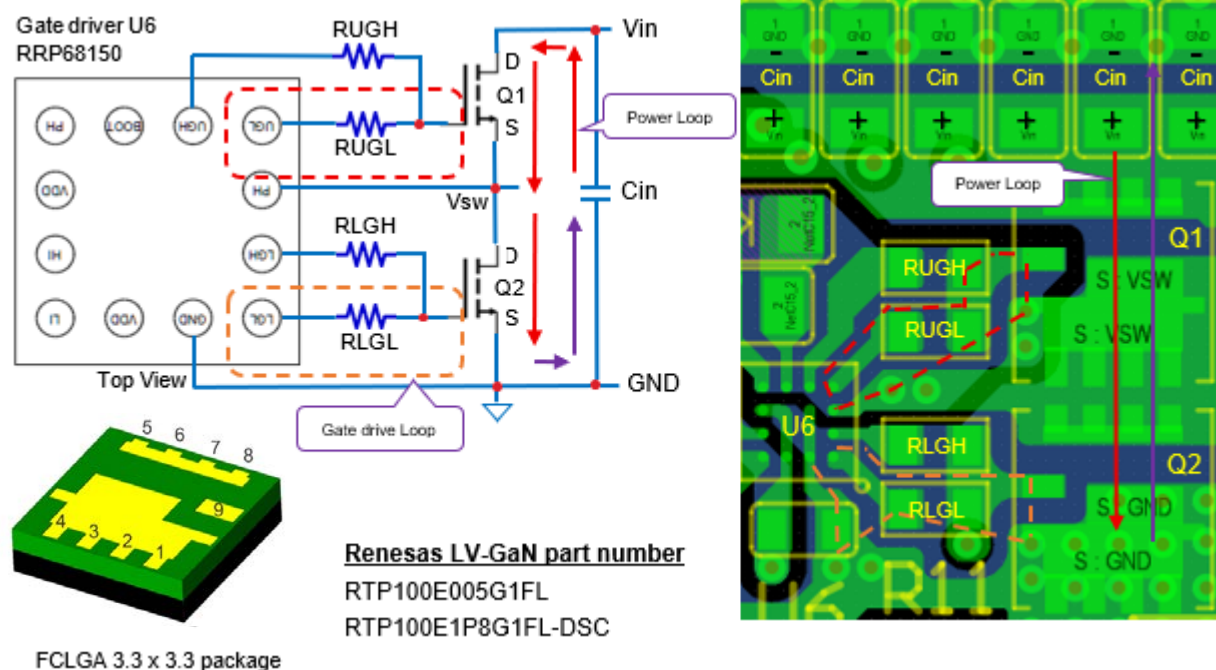


Figure 13. Reference Layout Considerations for FCLGA 3.3 × 3.3 mm Package

4.2 FCLGA 5 × 6 mm Package

The footprint of the FCLGA 3.3 × 3.3 mm and 5 × 6 mm packages is not the same. Especially the position of the gate terminal. The gate terminal of the 3.3 × 3.3 mm package is on left side, and the 5 × 6 mm package is on right side (on top view) as shown in Figure 14 (a). Because of this reason, it is recommended to place the gate driver at top side and the LV-GaN at bottom side. In this way, the gate drive loop can keep relatively small.

Figure 14 (b) shows the reference layout.

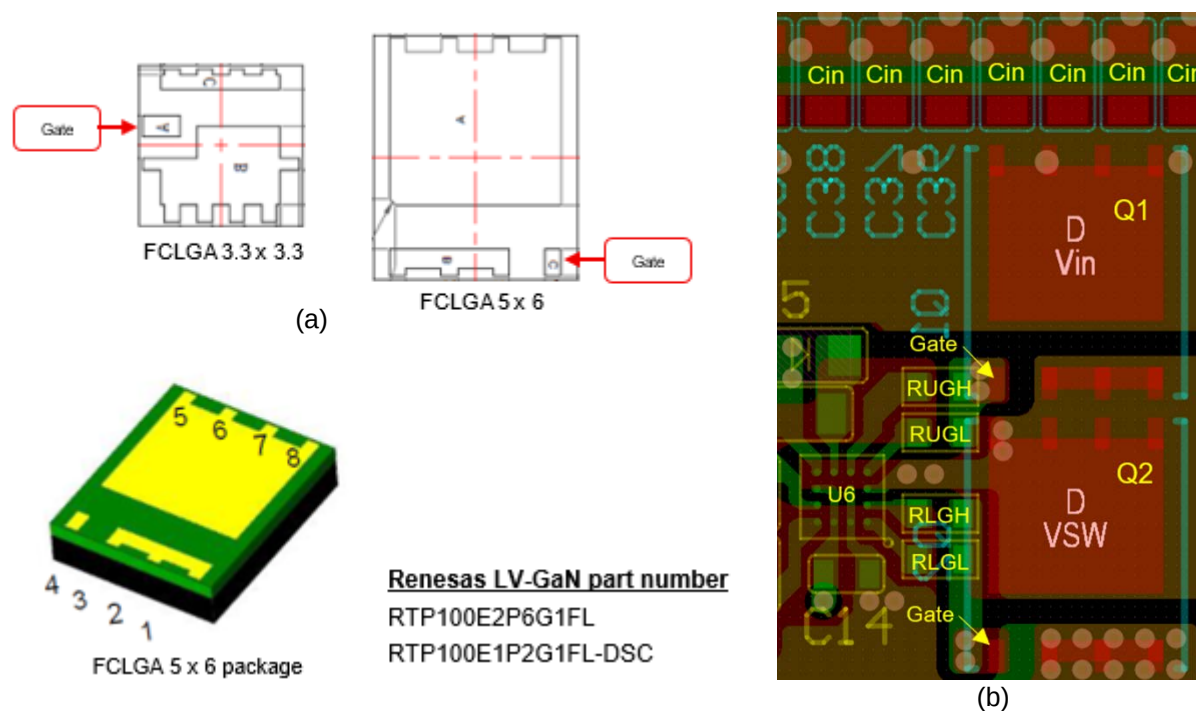


Figure 14. FCLGA 5 × 6 mm Package Footprint (a) and Reference Layout (b)

5. Measurement Techniques

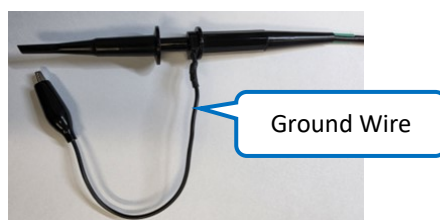
When measuring gate voltage and switching node voltage containing high-frequency content, care must be taken to provide an accurate measurement.

1. General Probe Guidelines:

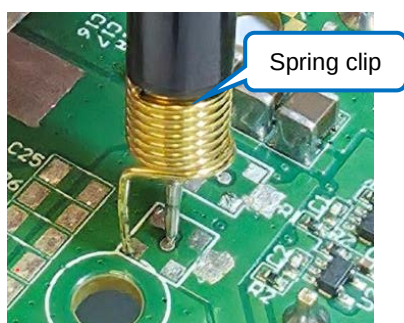
- Use highest possible bandwidth available in probe (500MHz recommended).
- Large input impedance $10\text{M}\Omega$, $< 16\text{pF}$.

2. Single Ended Probes

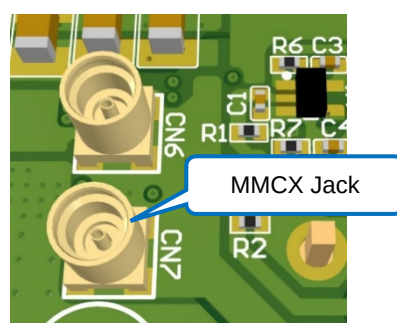
Do not use the typical long ground wire as shown below. A long wire acts as antenna that picks up radiated noise emitted by board.



3. There are two methods for measuring the high frequency switching waveform. The first method is to directly measure the traces near the components using a passive probe as shown in Figure 15 (a). A spring clip should be used to get a small ground loop to avoid noise pick-up. The second method is to measure the switching waveform using the MMCX jack as shown in Figure 15 (b).



(a)



(b)

Figure 15. Passive Probe (a) and MMCX Jack (b)

4. An isolated or differential probe is required for high-side measurements to avoid potential board damage.

6. Validation and Optimization of Design through Double Pulse Test

The Double Pulse Test (DPT) is a widely accepted method for characterizing switching behaviour under worst-case dynamic conditions. This test should be conducted on the final PCB layout to capture layout-dependent parasitic effects. Key parameters to evaluate include:

- Loop inductances voltage spikes at the drain-source and gate-source of GaN
- Rise time and fall time
- Slew rate control to balance EMI and energy efficiency
- Switching losses

Optimizing the trade-off between switching efficiency and waveform integrity, the gate resistor R_{g-on} and R_{g-off} should be empirically adjusted based on test results. This tuning directly affects the gate drive slew rate, which in turn influences switching losses, voltage stress, and EMI performance.

Figure 16 shows an example of the double pulse test result on the buck converter.

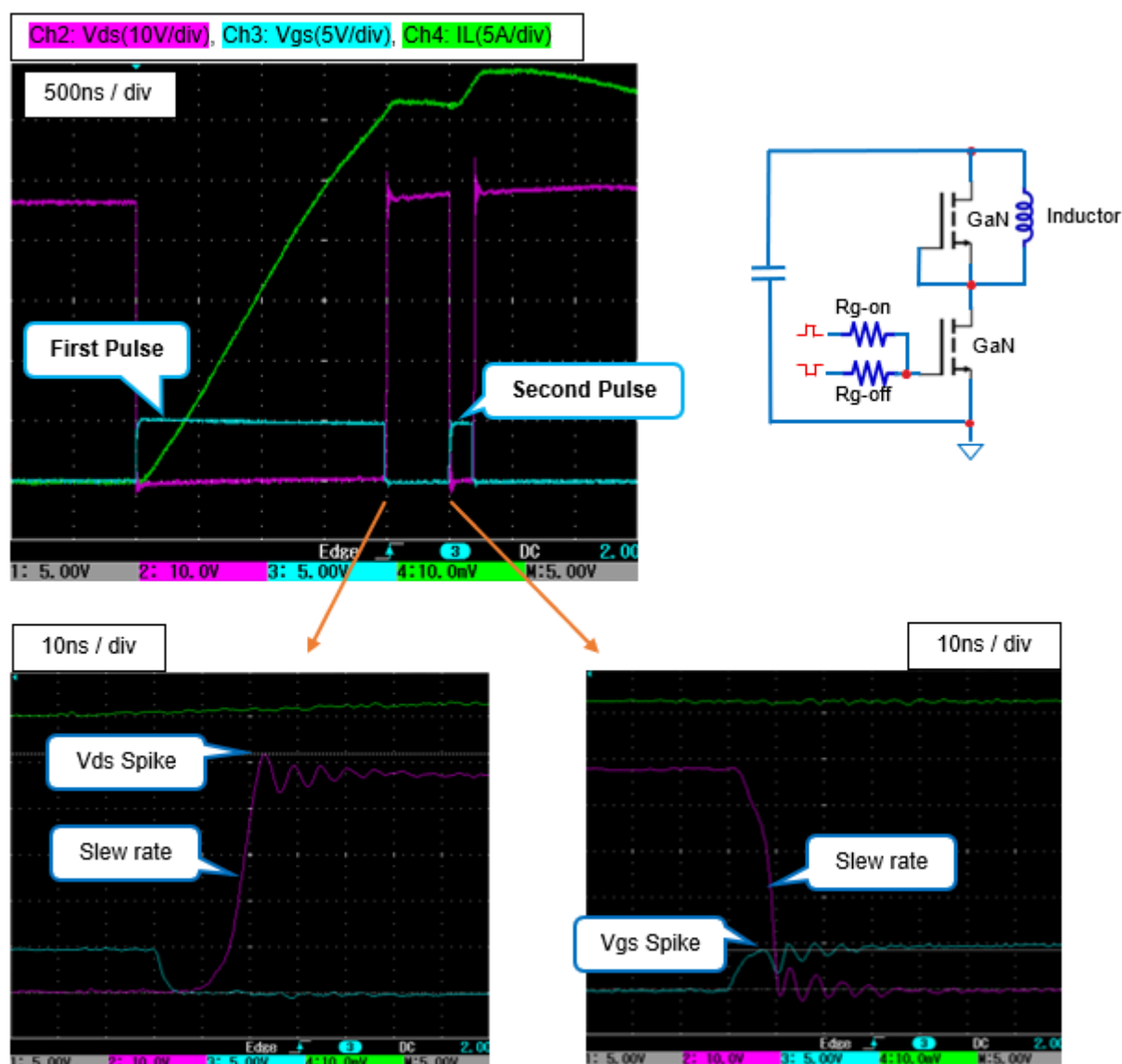


Figure 16. Buck Converter Double Pulse Test Results and DPT Circuit

7. Revision History

Revision	Date	Description
1.00	Sep 11, 2026	Initial release.

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