PCIe Buffer-Mux Layout Recommendations

The document describes the layout recommendations for the Buffer/Mux devices in the PCIe timing portfolio.

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1. PCIe Buffer/Mux Devices

The layout recommendations in this document pertain to the following PCIe Clock Buffer/Mux families:

- 9DBV/9DMV
- 9DBL/9DML
- 9ZXL/9ZML
- RC190/RC192
- RC191/RC193
- 9QXL/9Q31201D

There are two categories of pinouts: single-row and dual-row. These categories impact the signal routing and the component placement layout in the part area.

The layout specific examples provided within this document are applicable to the entire family of devices mentioned above.

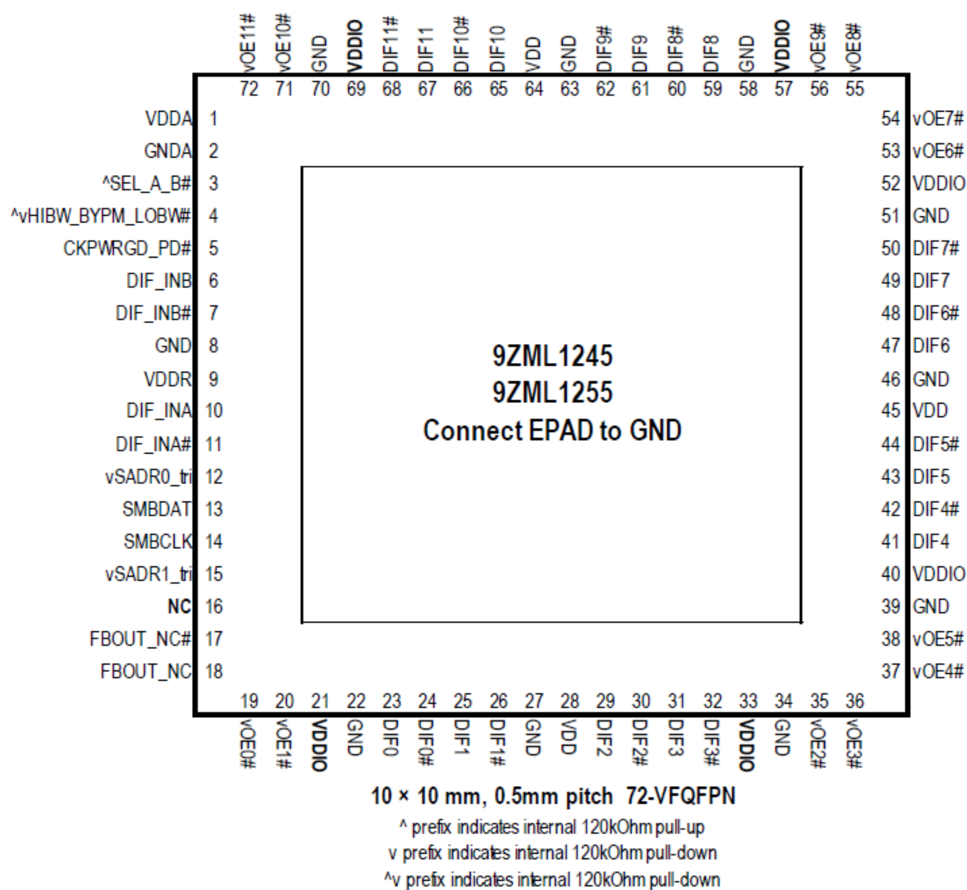


Figure 1. 9ZML124/55 VFQFPN (single-row pinout)

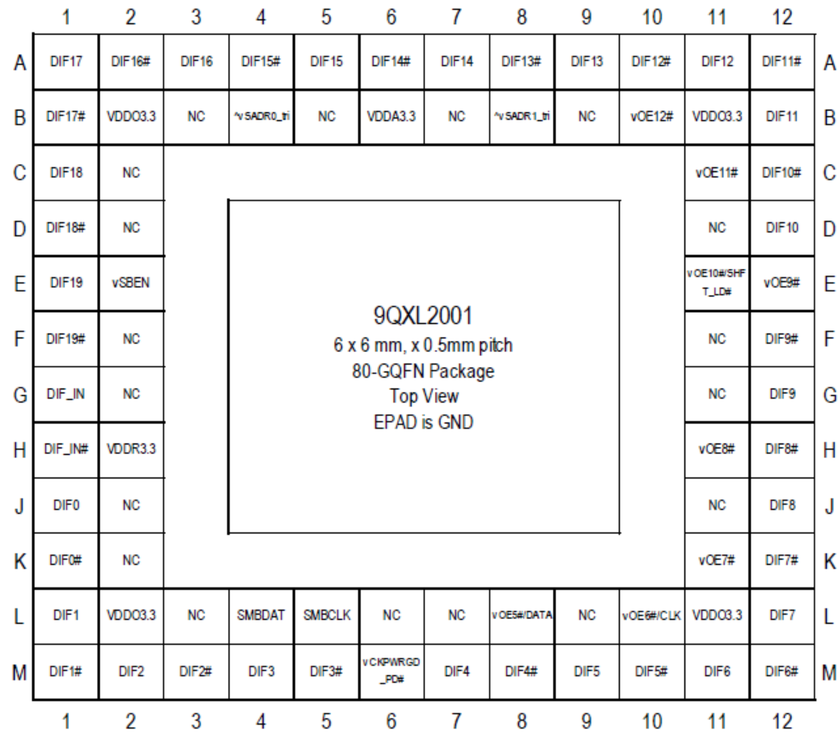


Figure 2. 9QXL2001 GQFN (dual-row pinout)

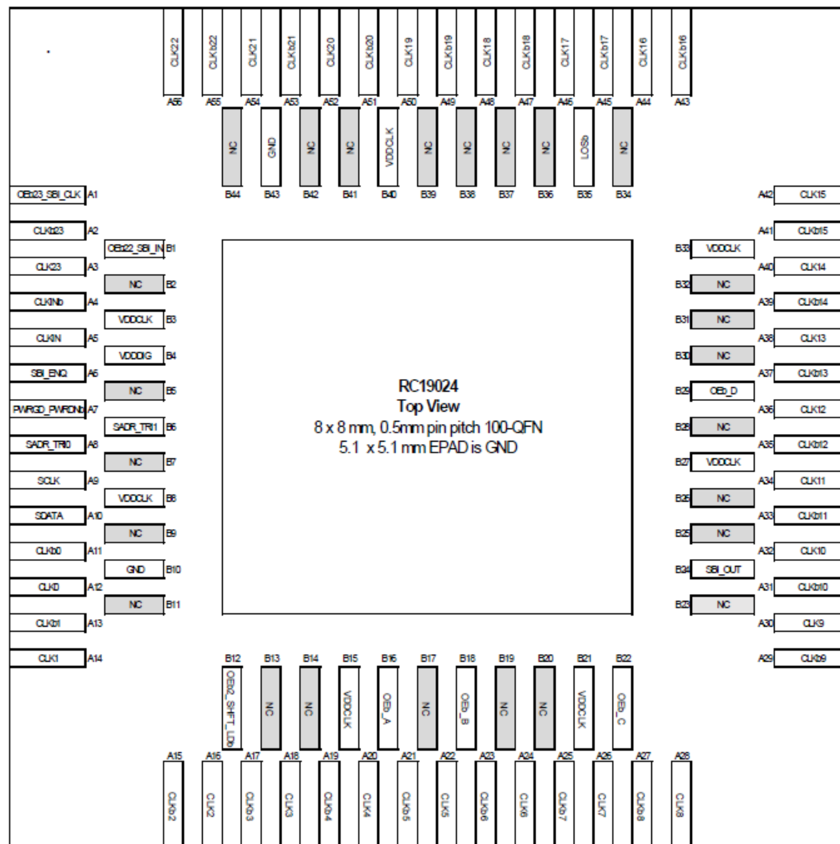


Figure 3. RC19024 QFN (dual-row pinout)

•	1	2	3	4	5	6	7	8	9	10
A	LOSb	CLKb0	CLK0	CLKb1	CLK1	CLKb2	CLK2	CLKb3	CLK3	OEb4_ SBI_CLK
B	SADR_ tri1	NC	OEb0	OEB1	VDDCLK	NC	OEb2_ SBI_OUT	OEb3	NC	CLKb4
C	SADR_ tri0	SLEW RATE_ SEL							VDDCLK	CLK4
D	SCLK	SDATA		GND	GND	GND	GND		NC	CLKb5
E	CLKIN	NC		GND	GND	GND	GND		OEb5	CLK5
F	CLKINB	VDDDIG		GND	GND	GND	GND		NC	CLKb6
G	OEb11	NC		GND	GND	GND	GND		OEb6	CLK6
H	CLK11	VDDCLK							VDDCLK	CLKb7
J	CLKb11	NC	VDDCLK	OEb10_ SHFT_ LDb	NC	OEb9	NC	OEb8	NC	CLK7
K	SBI_EN	PWRGD_ PWRDNb	NC	CLK10	CLKb10	CLK9	CLKb9	CLK8	CLKb8	OEb7_ SBI_IN

Figure 4. 9QXL1200 LGA (Land grid array)

2. PCB Layer Stack-up

A PCB has multiple layers of copper and assembled isolation materials. The stack-up is defined by the layer composition (copper and dielectric material), including the number of layers and the thickness.

A quality PCB starts with the circuit design; thus it's necessary to define a quality layout strategy that optimally interconnects each functional block of the design.

PCB design considerations:

- What is the highest frequency of the design?
- What are the electrical specifications? (voltage, type of signals, impedance, frequency, data rate…)
- Are there sensitive or high-speed signals to route? (power supply, clock, buses, high-speed interfaces, RF…)
- Create a block diagram, which helps to identify the different interconnections between the function blocks.
- Define the sizing of traces for each interconnection interface, in order to respect the requirements.

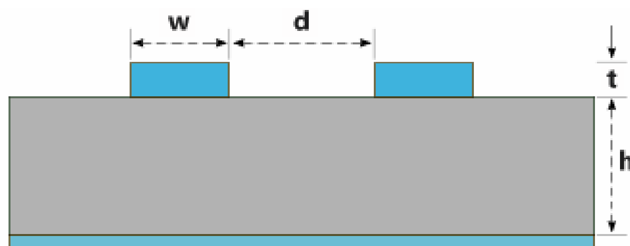
There is no fundamental information to define the number of layers, it depends on the number of traces needed to route all signals in the design.

We would recommend using the Polar instruments tool to size the stack-up and the traces.

2.1 Sizing traces

To size the clocking traces, Renesas recommends using a PCB toolkit software and targeting the impedance desired with a ±5% tolerance.

To define the sizing of a trace, there are different profiles in function of the layer configuration based on a microstrip profile.



Formula:

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)$$

$$Z_d = \frac{174}{\sqrt{\varepsilon_r + 1.41}} ln\left(\frac{5.98 \times h}{0.8 \times w + t}\right)\left(1 - 0.48exp\left(-0.96\frac{d}{h}\right)\right)$$

Figure 5. Microstrip Profile – Impedance Calculation

The microstrip impedance represents the characteristic impedance of the microstrip line, meaning the uniform impedance calculated on the dimensions of copper and materials along the microstrip.

The signals are referenced to GND.

where:

w = signal trace width

d = distance between the differential trace

h = distance between the trace and the GND plan

t = height of trace

Ɛr = dielectric constant

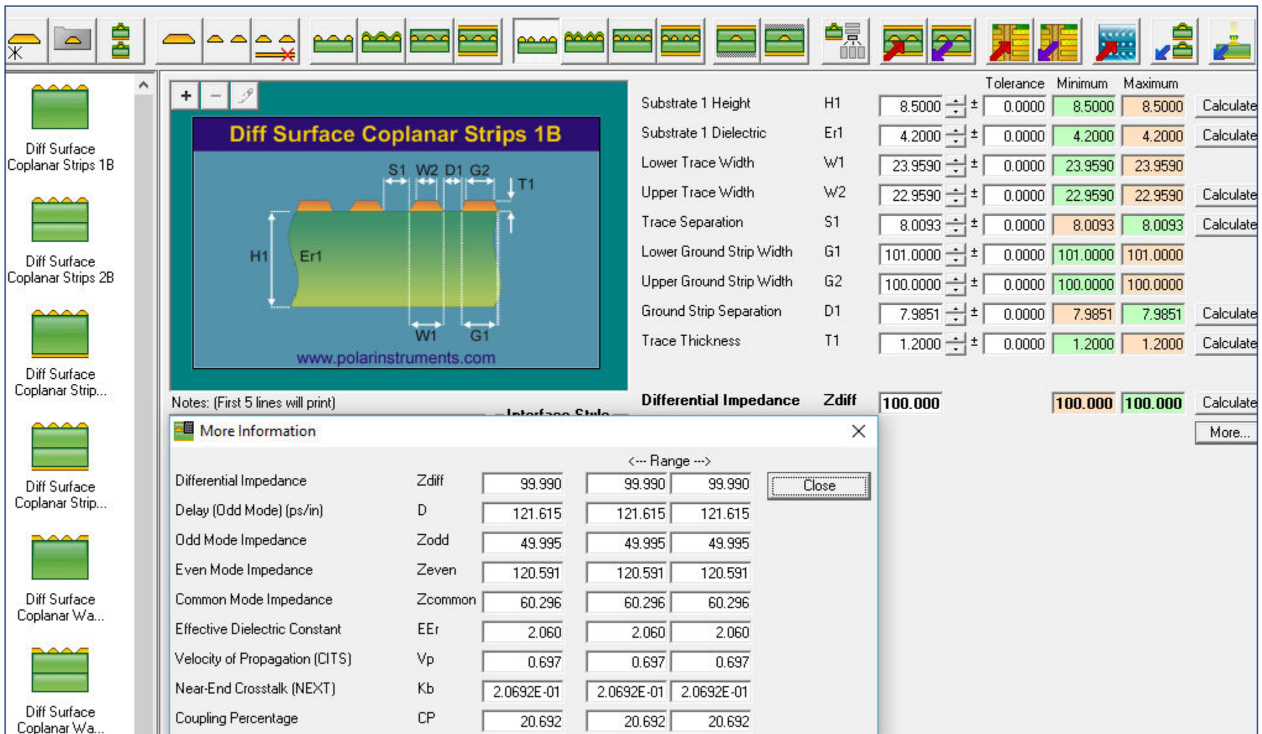


Figure 6. Polar Instruments – Impedance Calculation

After pre-defining the sizing of traces and the stack-up, it is necessary to submit them to PCB suppliers. These suppliers will provide the guidance to select the best materials for design criteria.

The Saturn PCB tool kit software is another tool for sizing the traces.

2.2 Common Layout Rules

To prevent signal routing issues, follow the common layout rules listed below.

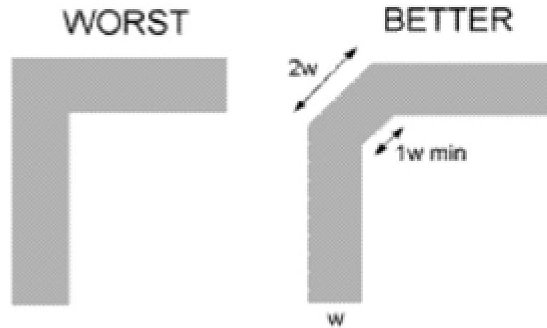


Figure 7. Signal Trace Bending

For bending signal traces, sharp-angle bending is recommended over right-angle bending.

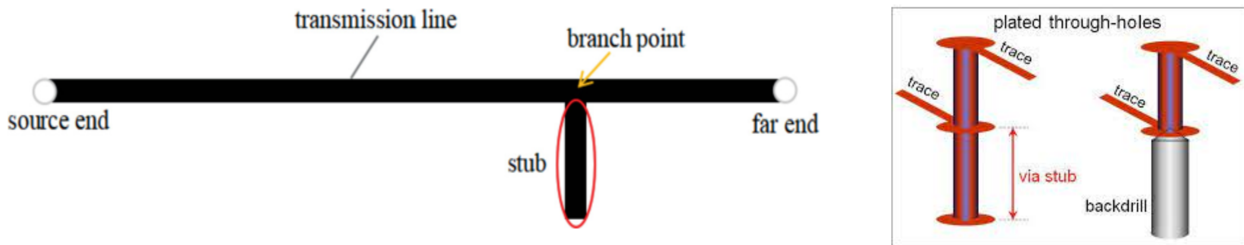


Figure 8. Stub PCB Layout

A stub is a branch off the main line of the transmission line. The mainline is the longest path from the source end (driver) to the far end (receiver or load).

The stub begins to have an impact as of ¼ wavelength. A reflection could appear on the transmission line generating a signal integrity issue (glitches on the edges, horizontal pedestal on the eye diagram) or EMC issues.

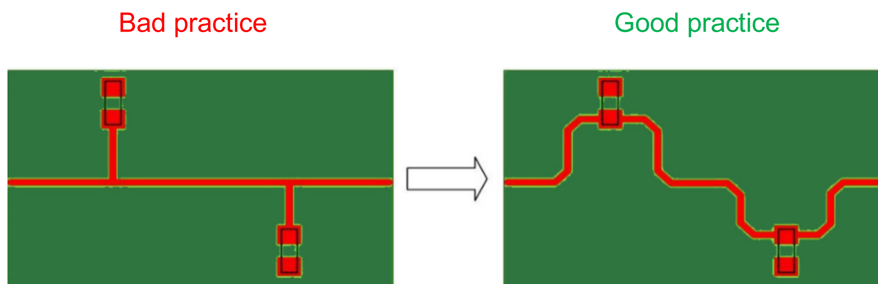


Figure 9. Stub PCB Routing Louting Practices

Figure 9 shows a way to limit the stub effect on a trace. To opt for a daisy chain layout for connecting the components.

- Renesas recommends routing the clock signals point to point on the same layer between the driver and the receiver (if possible)
- Renesas recommends trying to limit the stubs and the number of vias on the traces. Reduce them by using back-drilled via and opting for daisy chain layout
- Single-ended traces => Impedance 50 ohm
- Differential traces => Impedance differential 85 or 100 ohm ±5% tolerance (check the part characteristics)
- Renesas recommends applying signal integrity simulations and a rule checking format to verify the design

3. Layout Recommendations

3.1 Power Supply Layout

The power supply is an important part in a design layout and should be optimally implemented to avoid issues or dysfunctions.

To prevent the power supply noises from other parts, the following action items are recommended:

- Place the decoupling capacitors in the same layer of the part with a short connection to ground (see Figure 10).
- Whereas for the BGAs and specific parts (dual rows pinout, for example), place the decoupling capacitors (100nF) close as possible to pins in the opposite layer of part, along with a short connection to ground.
- Place the capacitor on the current path, between the power via and the IC

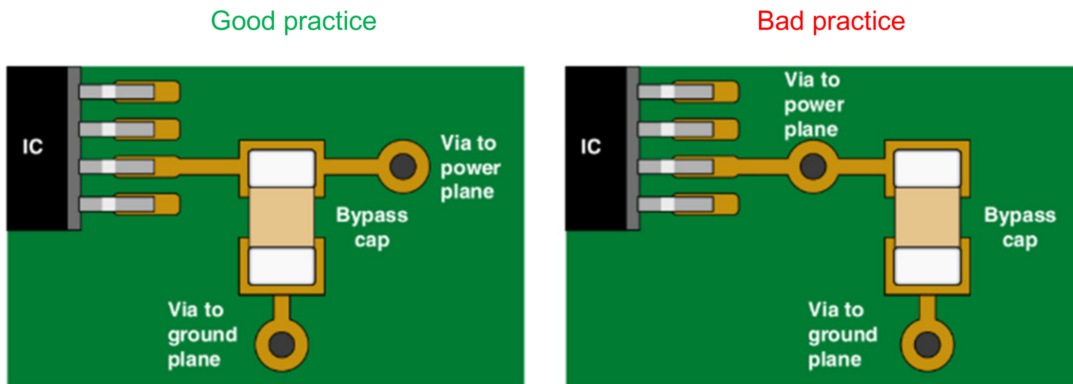


Figure 10. Decoupling Capacitor Layout Practices

Figure 11 shows the practice of implementing the placement of power filtering components in a design.

- Minimize the length of the GND connection to the capacitor, in order to reduce the coil effect.
- Place the capacitor of 100nF or the capacitor with the weaker value close as possible to the pin. It doesn't matter whether the ferrite bead placement is on top or on bottom.
- Don't share the ground via between the decoupling capacitors; each capacitor must have its own ground via.

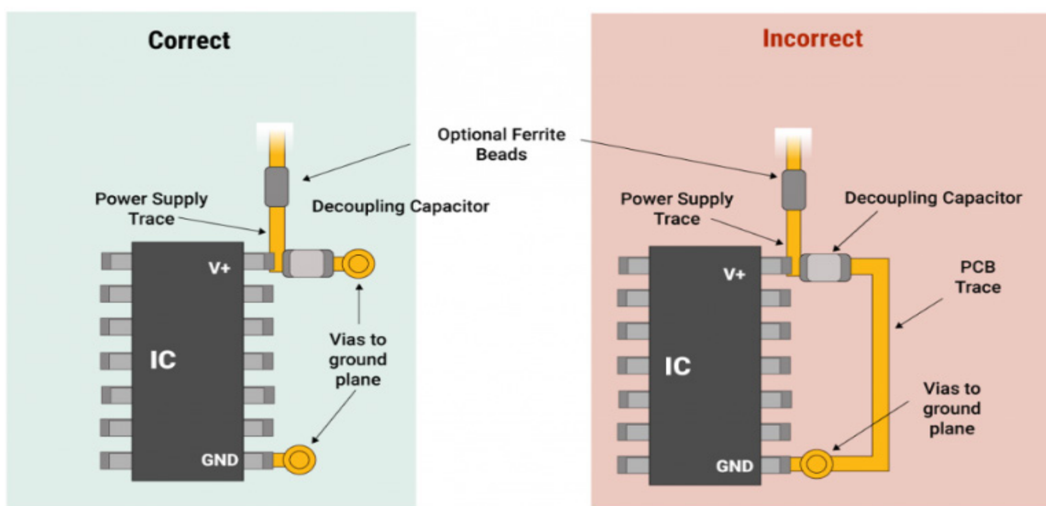


Figure 11. Power Filtering Layout Practices

Figure 12 shows how to use GND-Power planes instead of net.

A power plane allows more current to pass than the simple trace, and the GND plane, in addition to vias, improves the efficiency of the decoupling capacitors by reducing the coil effect due to the ground trace (shown in the left-side image of Figure 12).

- Size the Power-GND plane/trace correctly and the number of via in function the circulating current to avoid a PCB heating or a voltage drop.
- Implement a GND plane or allow sufficient spacing between the power planes/nets.
- Check the sizing of power planes. Renesas recommends launching power integrity simulation.
- Ensure to have complete Power-GND planes, to avoid split planes. Split planes can act as a radiating slot antenna.
- Implement a GND plane in the layer below or above in function of the part location.

  Note: In Figure 12, green represents the GND plane; yellow represents the Power plane.

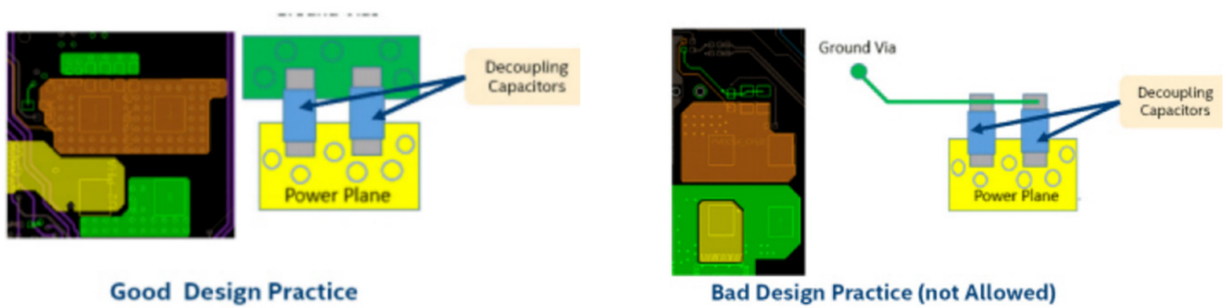


Figure 12. Power-GND Plane + Decoupling Capacitors Layout Practices

The left image of Figure 13 (9DBL0455 EVB) shows the power layout implementation for a QFPN part with a single-row pinout. All the power components are placed close to the part and on the same layer.

The right image of Figure 13 (9QXL2001 EVB) shows a different implementation due to a dual-row pinout. The power pins are located in the inner row, requiring the decoupling capacitors to be placed on the opposite layer (part on top layer, capacitors on bottom layer).

In both cases, the capacitors are placed close to the part as possible.

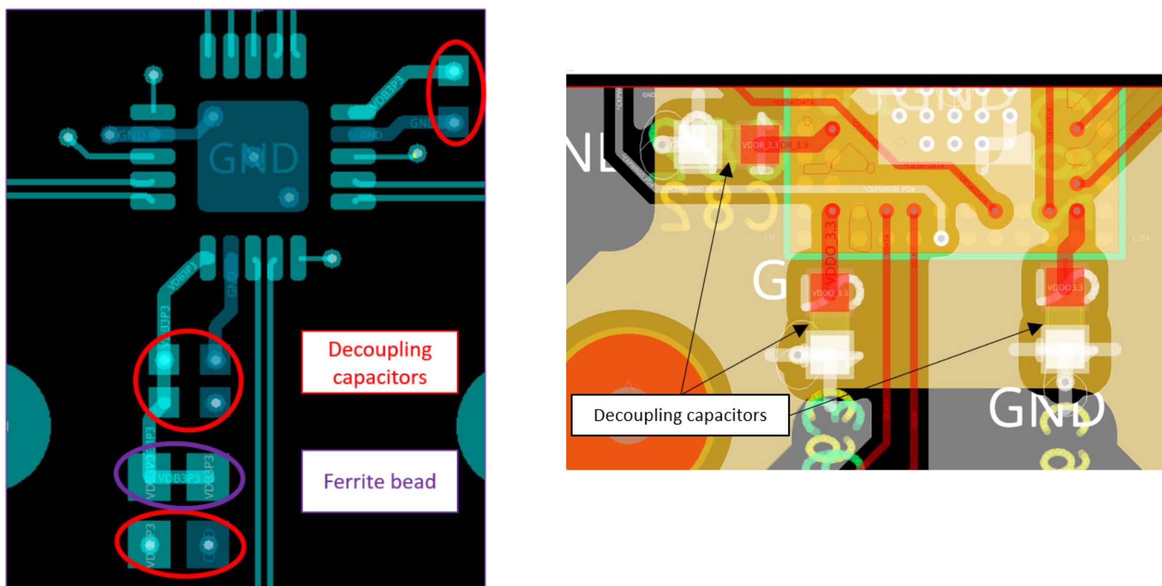


Figure 13. 9DBL0455 EVB and 9QXL2001 EVB Power Supply Layout

Usually, the power tracks are larger than the signal tracks (see Figure 14). The larger power tracks limit the amount of drop voltage.

Power planes are also a good option by providing more current and thermal dissipation.

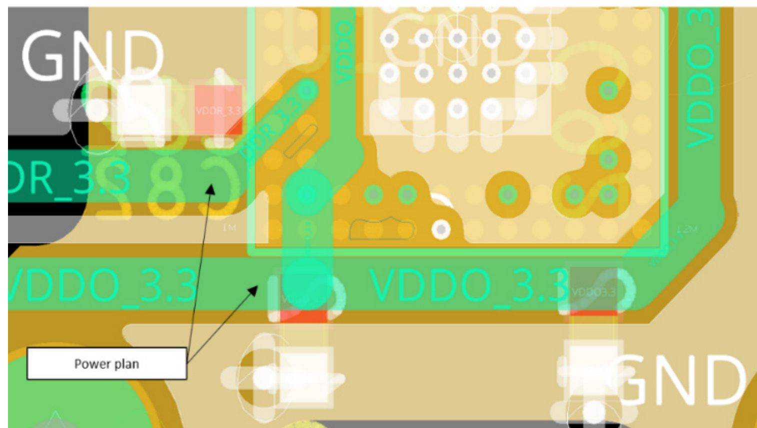


Figure 14. 9QXL2001 Power Tracks Layout

3.2 Clocking Layout

For differential traces, we would recommend the following practices:

Differential Traces Layout Practices (1) (see Figure 15)

- Do not place any component or via between the differential pair
- Place the components symmetrically and use a small size for the components (0402 or 0201 are recommended; avoid 0603)

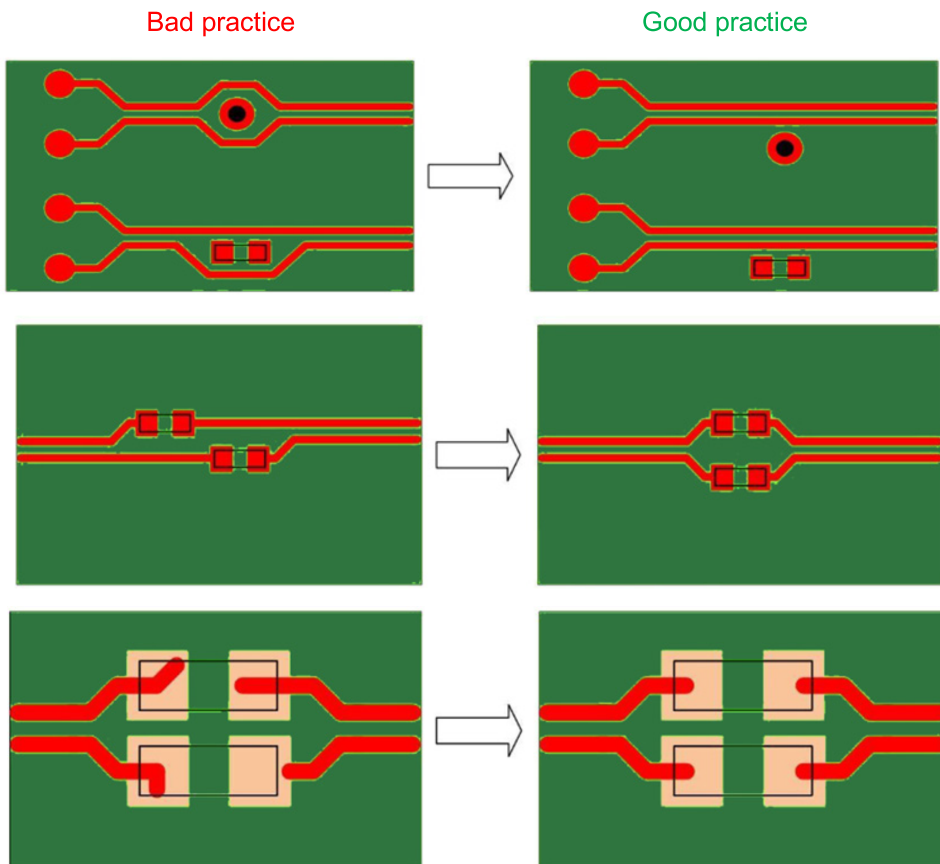


Figure 15. Differential Traces Layout Practices (1)

Differential Traces Layout Practices (2) (see Figure 16)

- Route the pair on the same layer and place the same number of vias. Place the vias symmetrically
- Renesas recommends keeping the symmetry of the differential pair on the entirety of the traces
- Renesas recommends ensuring and respecting the length matching to avoid signal integrity issues or common mode issues (propagation delay 1mm => 6ps)

  Note: In the images below, red represents layer A and blue represents layer B.

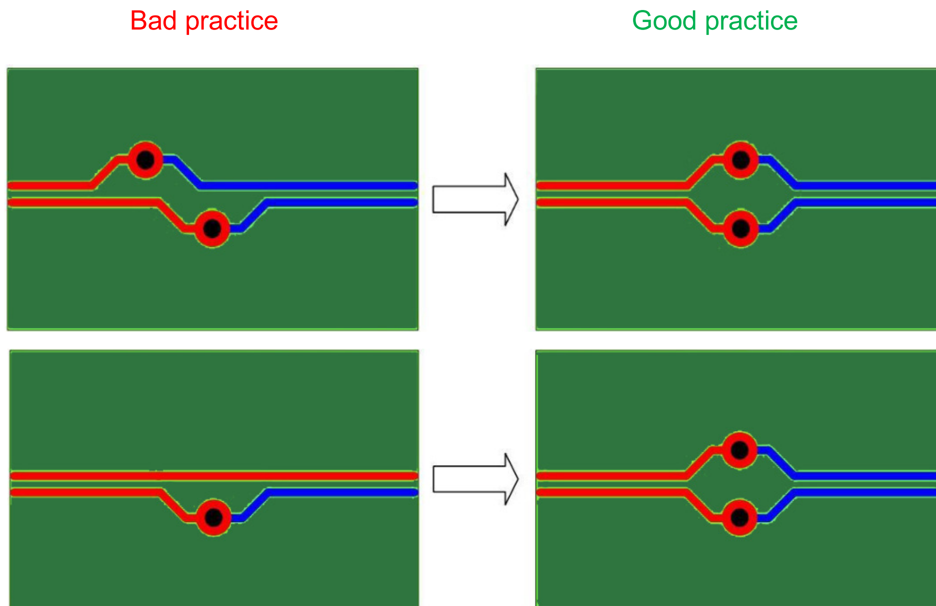


Figure 16. Differential Traces Layout Practices (2)

To compensate for the mismatched length, the following practice is recommended:

- Apply a serpentine to compensate the length between the differential traces

  Rule: S1 < 2 × S, B = D = F = H= 3 × w, 45-degree bend, where *w* is the trace width.

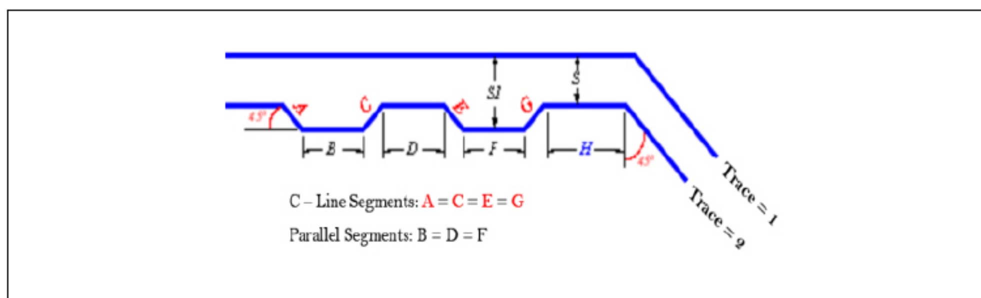


Figure 17. Serpentine Differential Mismatched Length Compensation

Differential Traces Layout Practices (3) (see Figure 18)

In cases of mismatched length, Renesas recommends compensating for it as close as possible to the source of the mismatch in order to propagate the signals in phase on the entirety of the traces

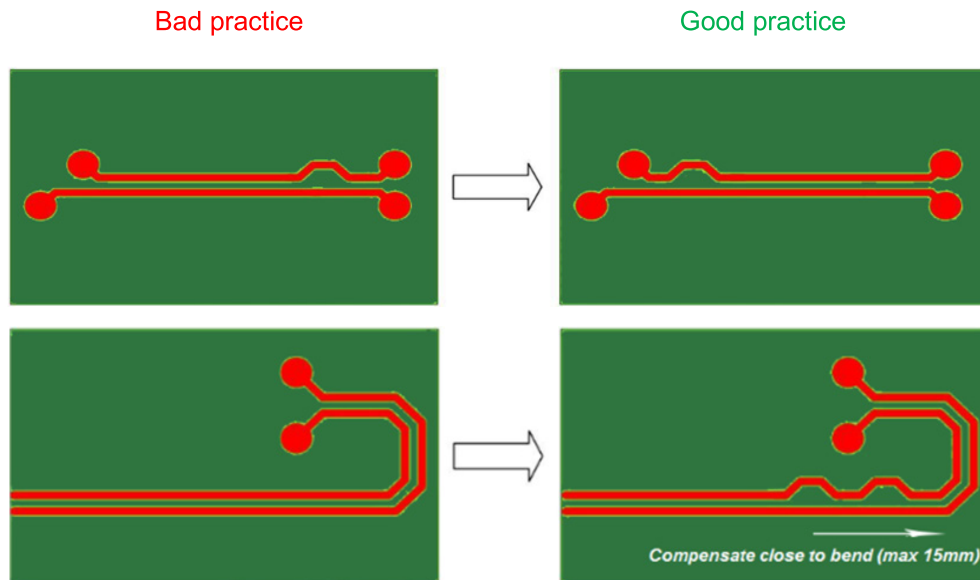


Figure 18. Differential Traces Layout Practices (3)

Figure 19 shows the differential traces implementation for a QFPN part with a single row pinout. All the clocking traces/components are symmetrically implemented.

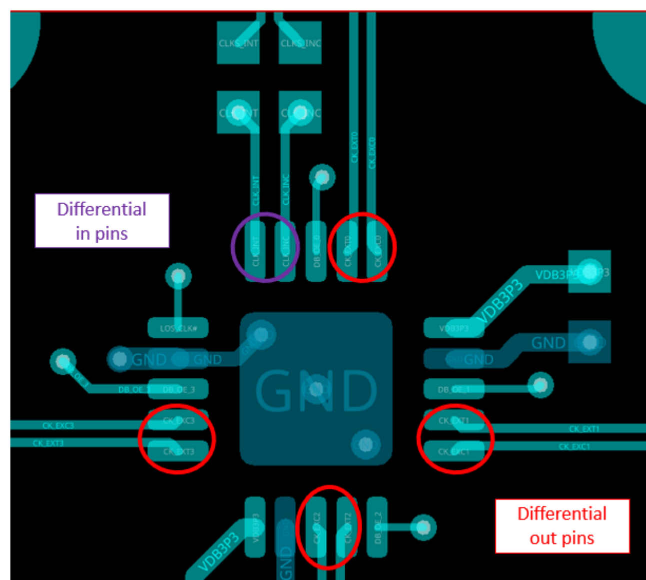


Figure 19. 9DBL0455 EVB Differential Traces Layout

Figure 20 shows the differential traces implementation for a QFPN part with a single-row pinout. All the clocking traces/components are symmetrically implemented to ensure length matches. In the SMA connector area, the differential track is routed in two single-ended tracks due to the SMA connector.

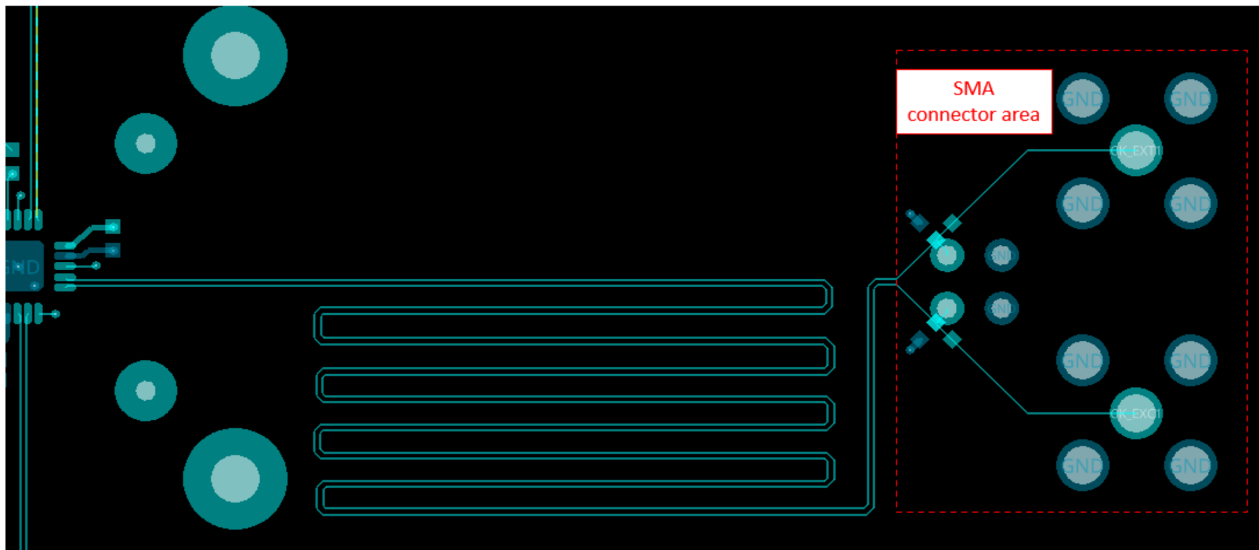


Figure 20. 9DBL0455 EVB Differential Traces Layout (2)

As shown in Figure 21, all the clocking pins are located on the external row pinout and the implementation is symmetrical.

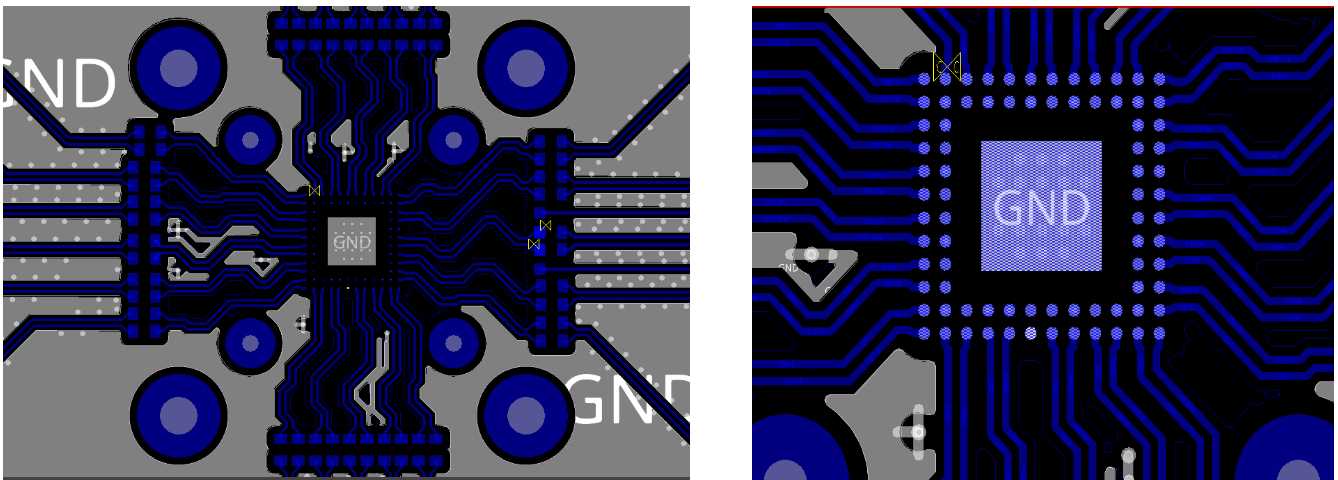


Figure 21. 9QXL2001 Differential Traces Layout (top layer)

Figure 22 shows how to route traces that are connected to the inner-row pinout. Essentially, these pins are GPIO/miscellaneous/power pins. This design uses the via-inpad method to connect them.

- All the traces are routed on the bottom layer, however, routing them on an inner layer may also be possible
- Keep a sufficient distance between the signal traces and the EPAD GND vias

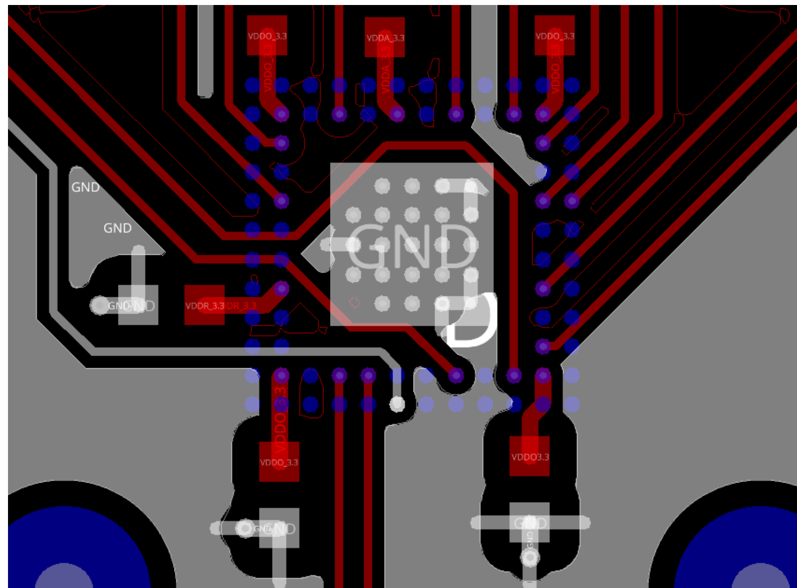


Figure 22. 9QXL2001 Differential Traces Layout (bottom layer)

3.3 EMI-EMC Layout

3.3.1. Current Return Path

The current return path is used to create a closed circuit with the signal path. It must be implemented using a short return path in order get the lowest resistance (see Figure 23).

- Renesas recommends implementing the current return path for the clocking signals and the high-speed signals to avoid any EMI-EMC issues
- Implement a GND plan above or below the signal plan to minimize the return path
- Ensure that the current return path closely follows as much of the signal path as possible. Reference the clock signals to GND.

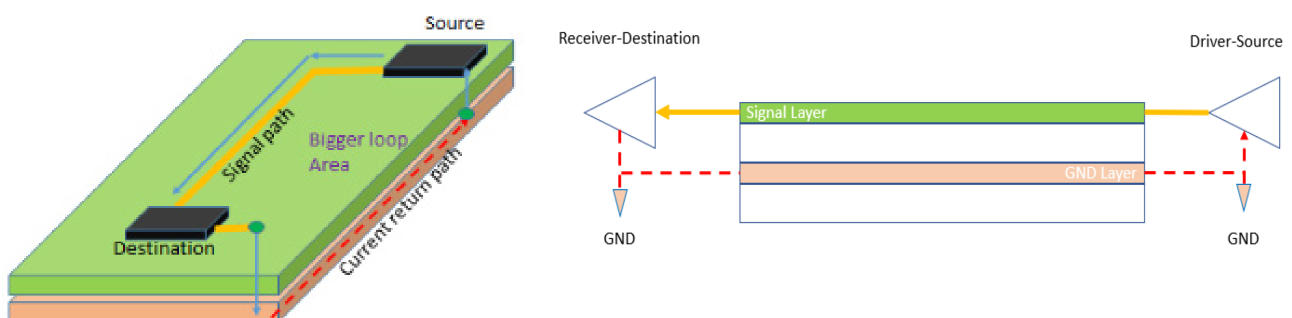


Figure 23. Current Return Path

Figure 24 shows how to implement a routing through different planes.

- Renesas recommends routing a signal across different planes. If this is not possible, implement a stitching capacitor next to the trace to maintain a short return path (see Figure 25).

  Note: In the images below, dark green represents the reference GND plane; light green represents the Obstruct plane.

Bad practice

Good practice

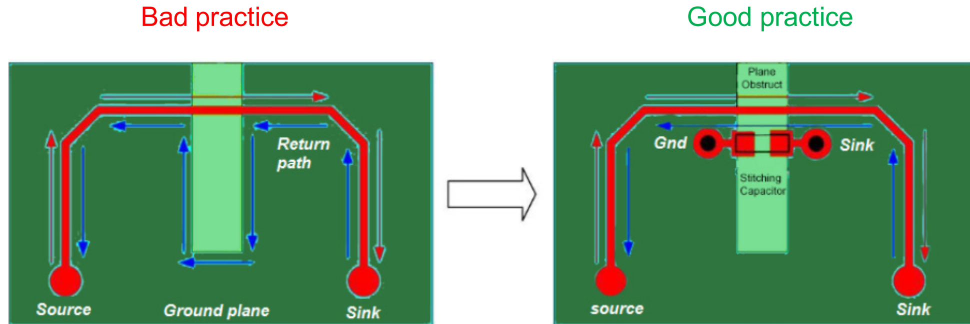


Figure 24. Current Return Path Layout Practices

- Use a GND via next to the signal via so that when the signal changes a layer, it ensures the integrity of the return current. Keep a sufficient distance between the GND via and the signal via so that the signal impedance is not affected.

  Note: The stitching capacitor isn't mandatory.

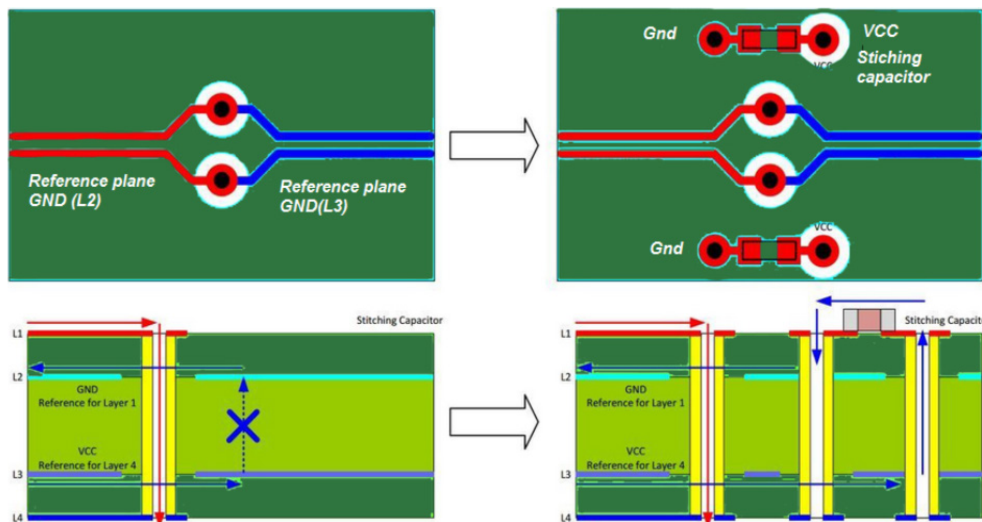


Figure 25. Stitching Via Layout Practices

3.3.2. Crosstalk and Spacing

A spacing of at least 3x width (5x width, optimal recommendation) is recommended between the clock signals and the other signals. Otherwise, the victim signal could receive noise from the aggressor signal.

If two signals with two different frequencies are in close proximity, the intermodulation products phenomenon could appear (see Figure 26).

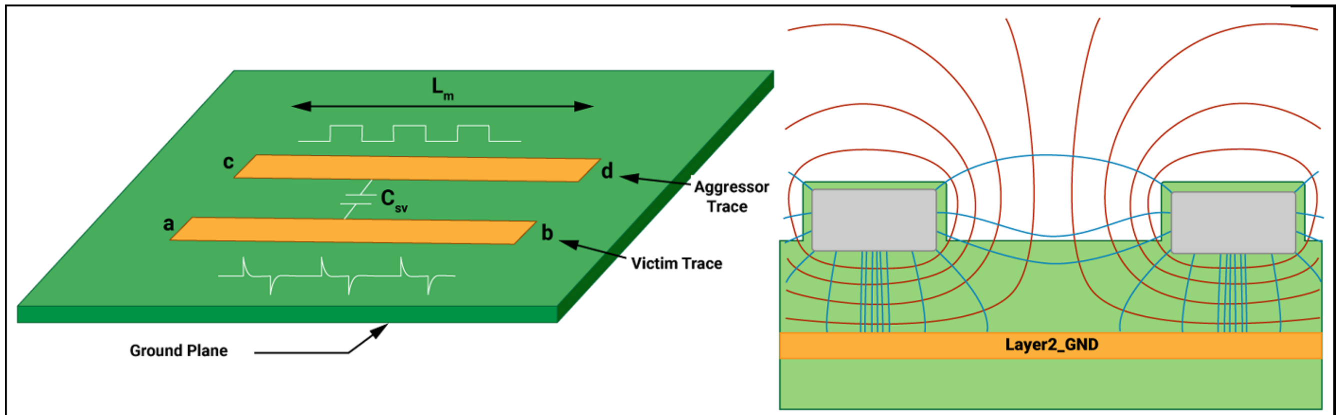


Figure 26. Crosstalk Layout Practices

Another way to isolate the traces is by adding a GND plane/trace beside the signal, as well as through all, or some, parts of the signal path. Adding stitching vias also helps to improve the efficiency of shielding (see Figure 27).

Note: The XTAL signals are not considered as a differential pair.

Important: This punctilious method must be applied correctly, otherwise the GND plane/net could receive noise from the signal and behave as antenna.

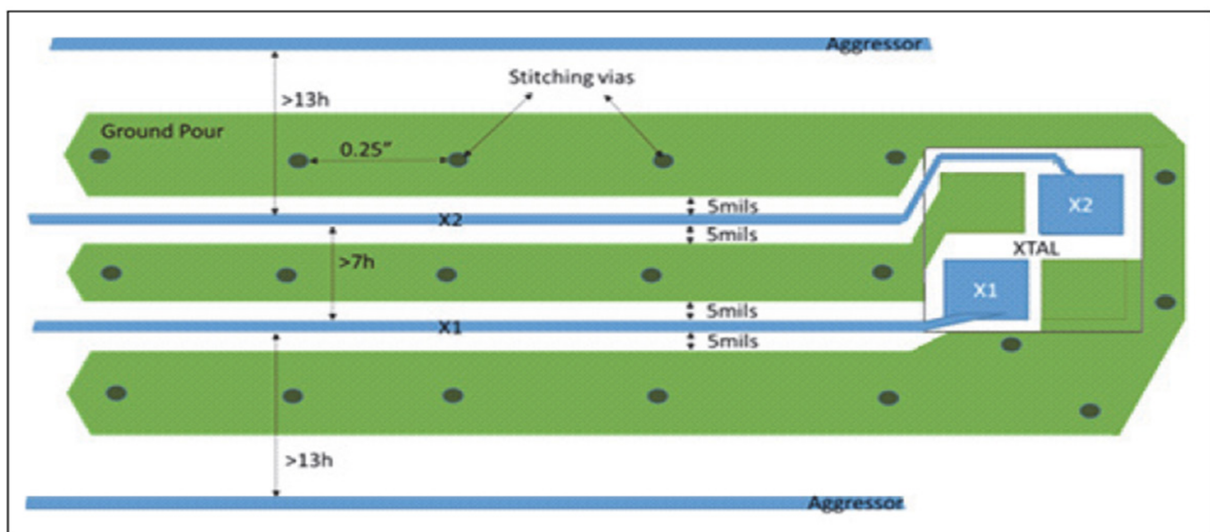


Figure 27. GND Shielding Layout Practices – XTAL Example

3.4 EPAD Thermal Layout

- Place a sufficient amount of thermal/GND vias for the EPAD to connect and dissipate the part correctly
- Refer to AN-842 Thermal Considerations in Package Design and Selection (renesas.com)
- Refer to the device's package outline drawing document

Figure 28 shows the evaluation board (EVB) EPAD layout for the 9DBL0455 EVB (left image) and the 9QXL2001 EVB (right image).

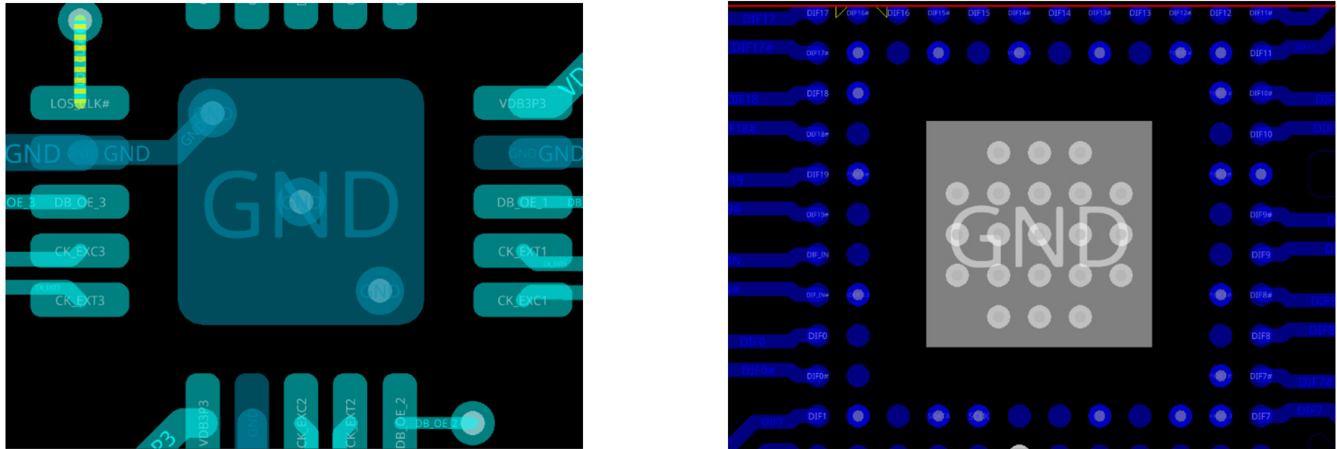
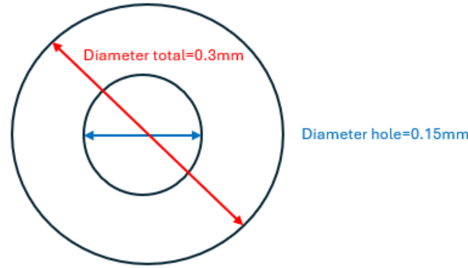


Figure 28. 9DBL0455 EVB and 9QXL2001 EVB EPAD Layout

The recommended minimum number of EPAD thermal vias for the RC190/RC191/RC192/RC193 parts are shown the table below.

Package	Part Number	Thermal Via Array
8 × 8 mm 100-VFQFPN (5.1 × 5.1 mm ePad)	RC19024A	7 × 7
6 × 6 mm 48-VFQFPN (4.2 × 4.2 mm Epad)	RC19208A / RC19308A	6 × 6
6 × 6 mm 80-VFQFPN (2.8 × 2.8 mm ePad)	RC19020A / 9QXL2001 / RC19016A / 9Q31201D	4 × 4
10 × 10 mm 72-VFQFPN (5.95 × 5.95 mm ePad)	RC19020A072	7 × 7
9 × 9 mm 64-VFQFPN (5.2 × 5.2 mm ePad)	RC19016A	7 × 7
7 × 7 mm 56-VFQFPN (5.3 × 5.3 mm ePad)	RC19013A	7 × 7
5 × 5 mm 40-VFQFPN (3.5 × 3.5 mm ePad)	RC19008A / RC19108A	4 × 4
4 × 4 mm 28-VFQFPN (2.6 × 2.6 mm ePad)	RC19004A / RC19104A / RC19204A / RC19304A	3 × 3
3 × 3 mm 20-VFQFPN (1.65 × 1.65 mm Epad)	RC19002A / RC19102A / RC19202A / RC19302A	3 × 3

Note 1: These recommendations are based on via dimensions of 0.3mm diameter total and 0.15mm diameter hole.



Note 2: If the EPAD dimensions are the same for other Clock Buffer-Mux families parts mentioned in this document, then the thermal EPAD via recommendation is also valid.

3.5 LGA Package

Note: Previous recommendations for LGA packages remain valid.

The LGA (Land Grid Array) package requires a grid of contacts on the PCB for the connection. This grid is composed of flat shaped contact pads to create a mounting surface, as opposed to a BGA (Ball Grid Array) package which is characterized by an array of solder balls.

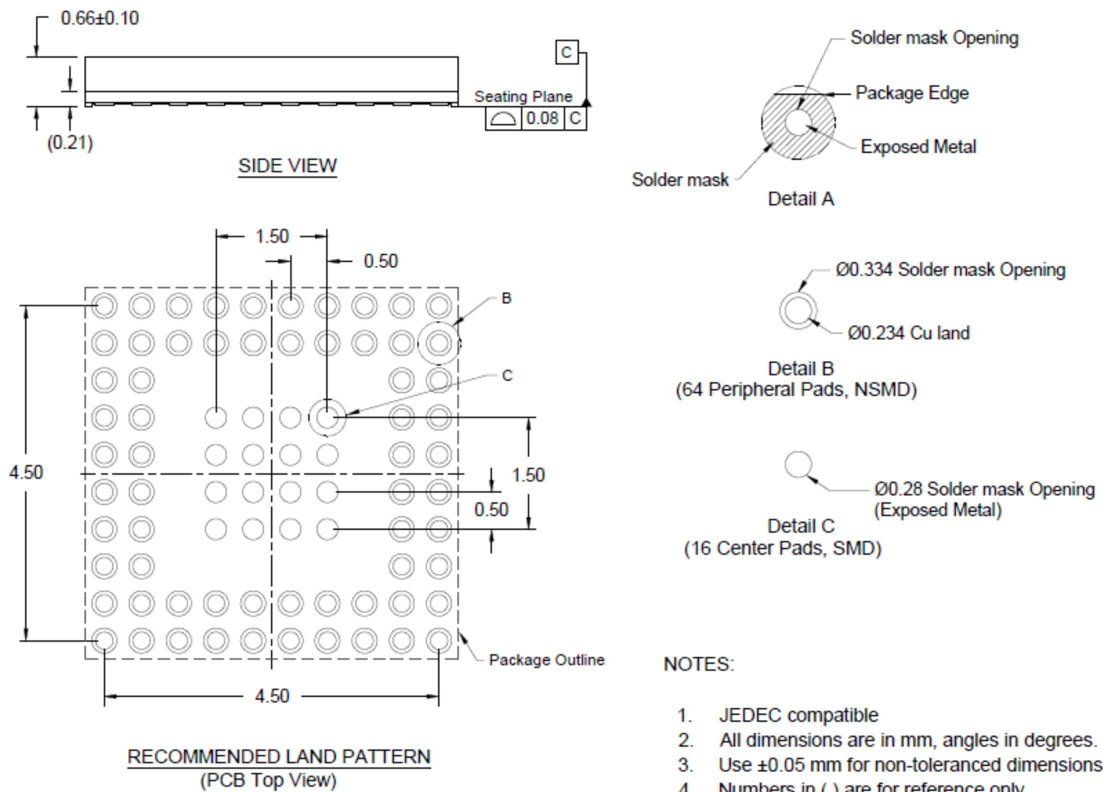


Figure 29. 9QXL1200 Land Pattern

For the 9QXL1200, the grid requires specified circular shapes and spacing, and the GND contact is ensured by the middle pins (see Figure 30). Renesas recommends implementing a squared copper plane and vias in the GND grid landing area.

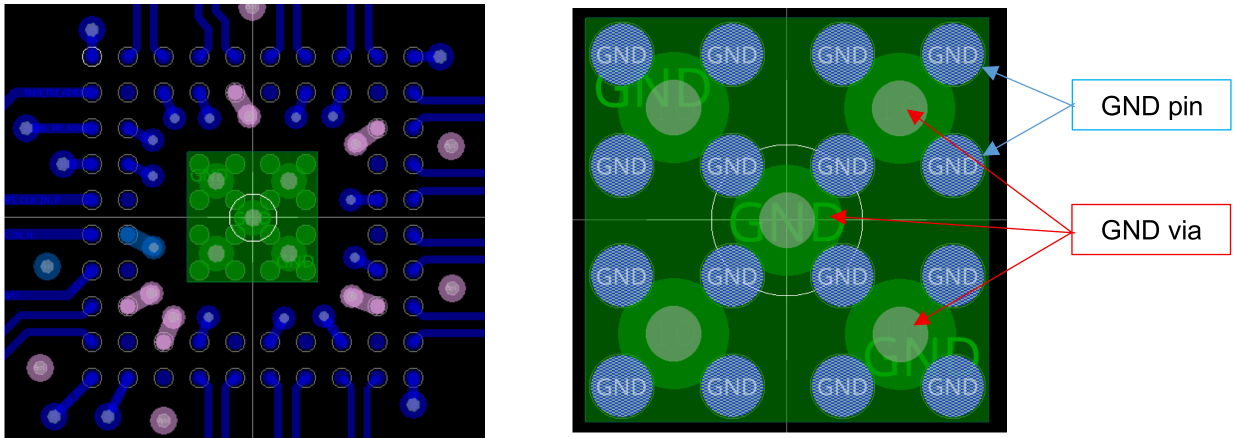


Figure 30. 9QXL1200 Land Pattern Layout

Renesas recommends implementing a square GND plane (1.83 × 1.83 mm) to surround the GND pins (see Figure 31). This plane is fully recovered by varnish for the isolation with the exception of the GND pins. To avoid hitting the external rows pinout, this plane should not exceed specified dimensions.

Important: Do not implement this plane as a QFN EPAD.

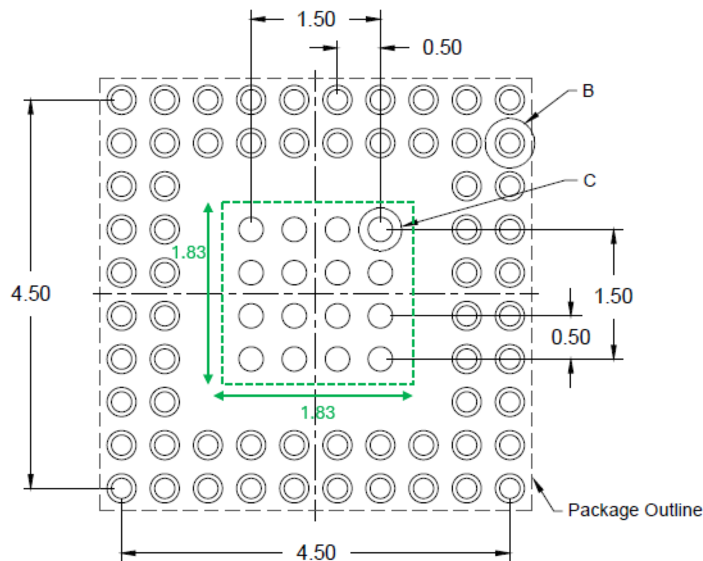


Figure 31. 9QXL1200 GND Plane

To ensure proper contact, the GND via needs to overlap the four GND pins of the part (see Figure 32). These vias need to be filled with nonconductive material and plated fat.

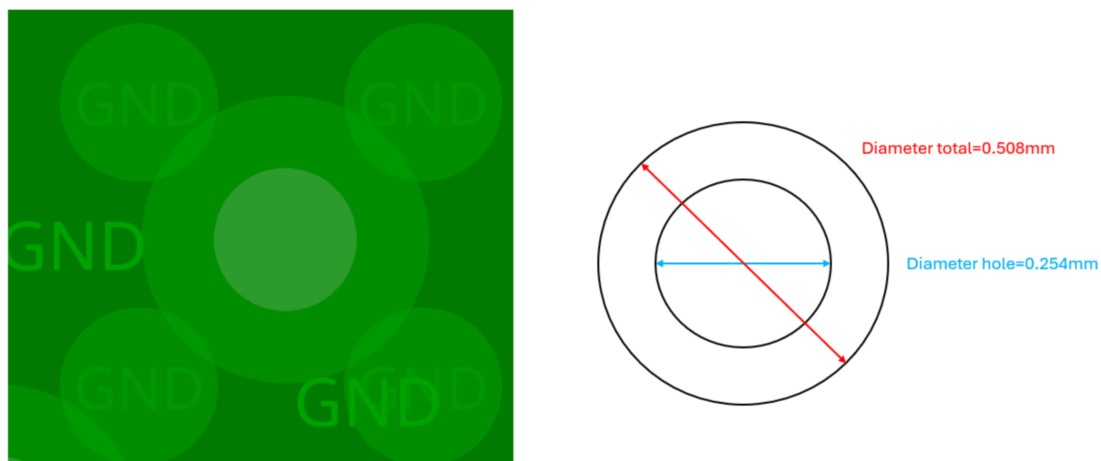


Figure 32. 9QXL1200 GND Plane – Via Implementation

4. Revision History

Revision	Date	Description
1.02	Jun 2, 2026	Added 9Q31201D device.
1.01	Sep 2, 2025	Added LGA package recommendation section 3.5.
1.00	Nov 19, 2024	Initial release.

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