PLL Loop Filter Design and Fine Tuning

This application note provides instructions for calculating and fine tuning PLL loop filters, assuring the PLL is operating in a stable region, and optimizing PLL output phase noise.

Contents

1. Introduction

This document contains basic PLL loop filter information, as well as loop bandwidth and loop filter calculations. Lab experiment results of different loop bandwidth settings are also provided to demonstrate the effect of the loop bandwidth setting. These results demonstrate that optimized phase noise can be obtained by proper loop bandwidth tuning.

2. PLL Loop Filter

A basic PLL block diagram is shown in Figure 1. Board level designers or PLL component users are required to determine the loop filter component values based on the application requirement. Figure 2 and Figure 3 are examples of common passive loop filters: a second order loop filter and a third order loop filter, respectively.

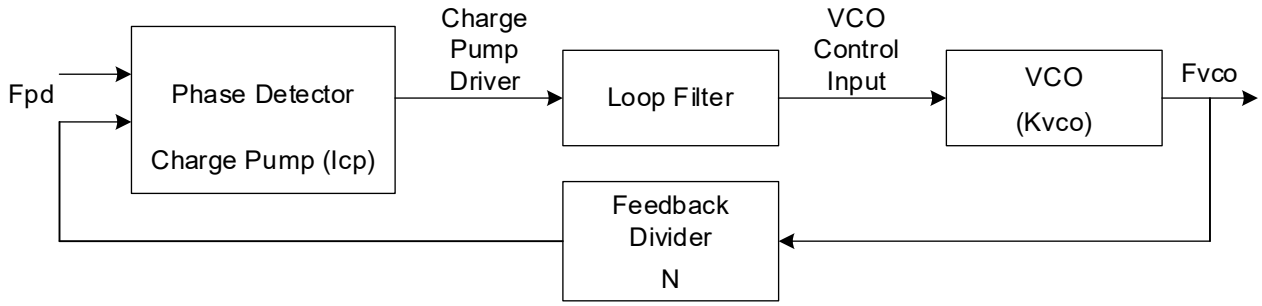

Figure 1. Basic PLL Block Diagram

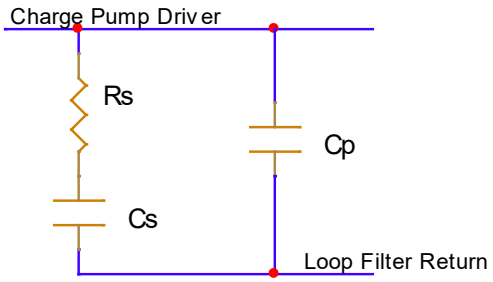

Figure 2. Second Order Loop Filter

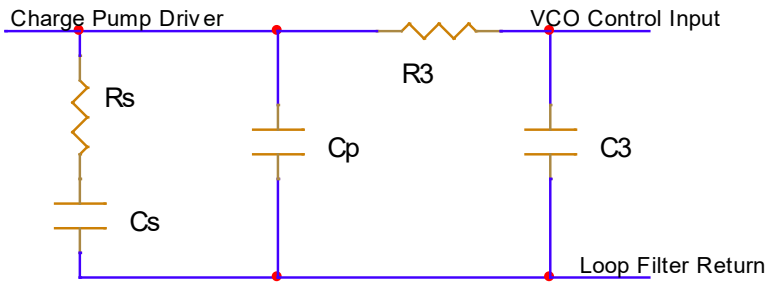

Figure 3. Third Order Loop Filter

3. Loop Bandwidth Calculation

The following equations show how each parameter affects the loop bandwidth.

3.1 Cut-off Frequency (Fc)

$$Fc = \frac{Rs*Icp*Kvco}{N*2*Pi}$$

where

Icp is charge pump current.

Kvco is VCO gain.

N is effective feedback divider.

The loop bandwidth can be adjusted by the parameters in the equation. Increasing Rs, Icp or Kvco will increase loop bandwidth. Increasing feedback divider will decrease the loop bandwidth. The only loop filter component that can affect loop bandwidth is Rs. Other loop filter components affect zero frequency and pole frequencies that can affect the PLL stability.

3.2 Zero Frequency (Fz)

$$Fz = \frac{1}{2\pi*Rs*Cs}$$

3.3 Pole Frequency (Fp)

$$Fp = \frac{1}{2\pi*Rs*Cp}$$

For third order loop filter, the 2nd pole frequency (Fp2) should be approximately 1.5x the first pole frequency (Fp).

$$Fp2 \sim \frac{1}{2\pi*R3*C3}$$

$$Fp2 \sim 3 * Fp$$

Figure 4 shows the approximate frequency region of the loop bandwidth frequency related to the zero frequency and pole frequencies. To keep the PLL operating in a stable region, the loop bandwidth frequency normally falls between zero frequency and pole frequency. Rule of thumb is that loop bandwidth Fc is approximately 3x or greater than zero frequency Fz. Fc is approximately 3x, or greater, below the pole frequency Fp. For 3rd order loop filter, the second pole frequency Fp2 must be greater than the first pole frequency Fp.

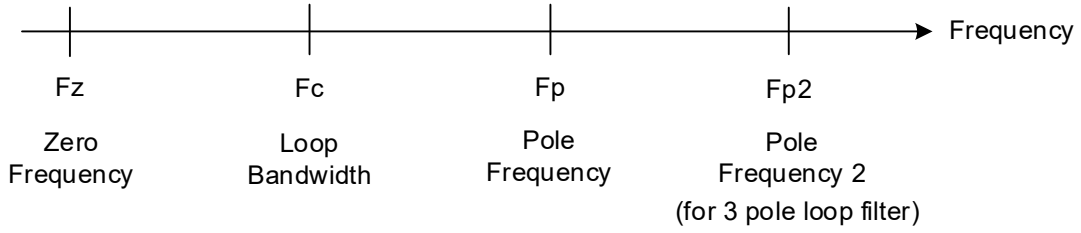

Figure 4. Approximate Region of Zero Frequency, Loop Bandwidth Frequency, and Pole Frequencies

4. Loop Filter Calculation

4.1 Second Order Loop Filter

Figure 5 shows a typical 2nd order loop filter. A step-by-step calculation to determine Rs, Cs, and Cp values is described in this section. The required parameters for this part are also provided. A software tool for calculating the loop filter values is also available. Contact Renesas tech support for more information.

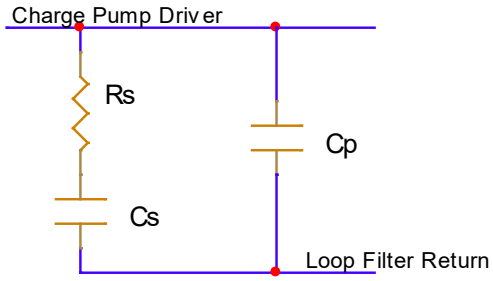

Figure 5. Typical 2nd Order Loop Filter

1. Determine desired loop bandwidth fc. The fc must satisfy the following condition:

$$\frac{Fpd}{fc} >> 20$$

where Fpd is phase detector input frequency.

2. Calculate Rs.

$$Rs = \frac{2*\pi*fc*N}{Icp*Kvco}$$

where N is effective feedback divider.

$$N = \frac{Fvco}{Fpd}$$

Fvco is VCO frequency.

Fpd is the phase detector input frequency.

3. Calculate Cs.

$$Cs = \frac{\alpha}{2*\pi*fc*Rs}$$

where,

α is ratio between loop bandwidth and the zero frequency, α = fc / fz, recommend α greater than 3.

fz is the zero frequency.

4. Calculate Cp.

$$Cp = \frac{Cs}{\alpha*\beta}$$

where,

β is ratio between pole frequency and loop bandwidth, β = fp / fc, recommend β greater than 3.

fp is the pole frequency.

5. Verify maximum Phase Margin, PM.

$$PM = \arctan(\frac{b-1}{2*\sqrt{b}})$$

where

$$b = 1 + \frac{Cs}{Cp}$$

PM needs to be greater than 50 degrees for PLL to be stable.

4.2 Third Order Loop Filter

This section contains design information for a 3rd order loop filter. Figure 6 shows a typical 3rd order loop filter.

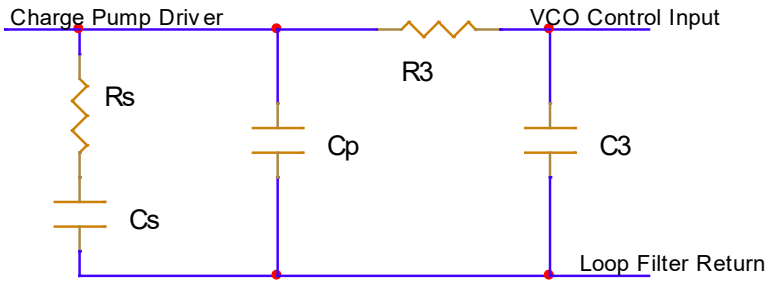

Figure 6. Typical 3rd Order Loop Filter

The Rs, Cs, and Cp can be the actual standard values chosen in the 2nd order loop filter. The following equation helps determine the 3rd order loop filter R3 and C3.

Pick an R3 value (suggested: R3 ~ 1.5xRs).

$$C3 = \frac{Rs*Cp}{R3*\gamma}$$

where,

γ is ratio between the 1st pole frequency Fp and the 2nd pole frequency Fp2. Suggested: γ greater than 1.5.

The Timing Commander™ software tool can calculate the loop filter component values.

5. Loop Filter Calculation Examples

5.1 Second Order Loop Filter

This section provides a calculation example for the VCXO PLL loop filter value. In this example, the reference CLK input frequency is 122.88MHz and the VCXO = 122.88MHz. The PLL output is also 122.88MHz. The 8V19N491-24 VCXO phase lock loop block diagram is shown in Figure 7. A 2nd order loop filter for VCXO is shown in Figure 8.

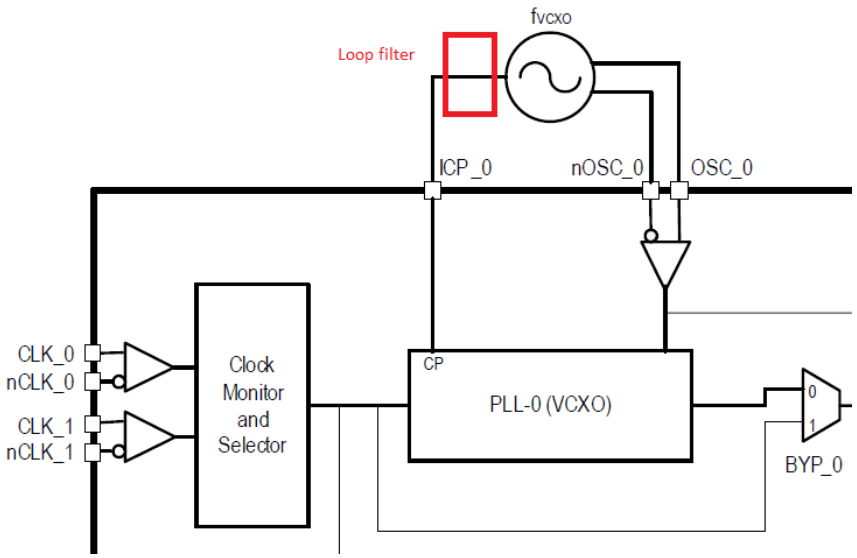

Figure 7. 8V19N491-24 VCXO Phase Lock Loop Block Diagram

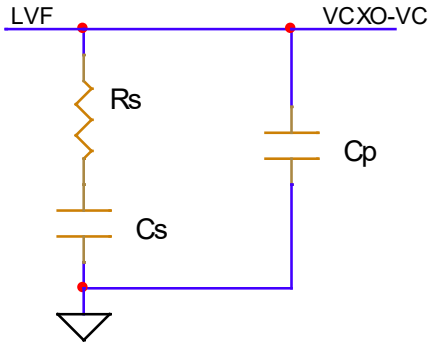

Figure 8. Typical 2nd Order Loop Filter

To calculate loop filter component values for loop bandwidth Fc = 40Hz with the reference CLK input frequency equals to 122.88MHz, set input pre-divider Pv = 1024. The phase detector input frequency Fpd = 0.120MHz. This satisfies the conditions of:

Fpd/Fc >> 20.

The VCXO frequency Fvcxo=122.88MHz, the effective feedback divider

N = Mv = Fvcxo / Fpd = 1024

- Rs can be calculated from the equation:

$$Rs = \frac{2 * \pi * \mathrm{fc} * \mathrm{N}}{\mathrm{Icp} * \mathrm{Kvco}}$$

Rs ~ 24kOhm

Kvco VCO gain can be found or derived from the VCXO datasheet. The VCO gain can also be measured from the lab experiment. In this example, we use Kvco = 9kHz/V.

The 8V19N491-24 charge pump current can be set from 50µA to 1.6mA through registers. In this example, assume the charge pump current is programmed to 1.25mA.

- Cs can be calculated from the following equation:

$$Cs = \frac{\alpha}{2*\pi*fc*Rs}$$

For α = 3, Cs is calculated to be 5.22µF. Cs greater than this value can be used to assure that the α is greater than 3. For example, the actual chosen value can be 10µF from a standard capacitor value.

- Cp can be calculated from the equation:

$$Cp = \frac{Cs}{\alpha*\beta}$$

For β = 4, Cp is calculated to be 145nF. Less than this value can be used for Cp to guarantee that the β is greater than 4 (e.g., actual chosen value Cp can be 47nF).

5.2 Third Order Loop Filter

This section describes how to determine a 3rd order loop filter for the 8V19N491-24 VCXO PLL. A typical 3rd order loop filter is shown in Figure 9.

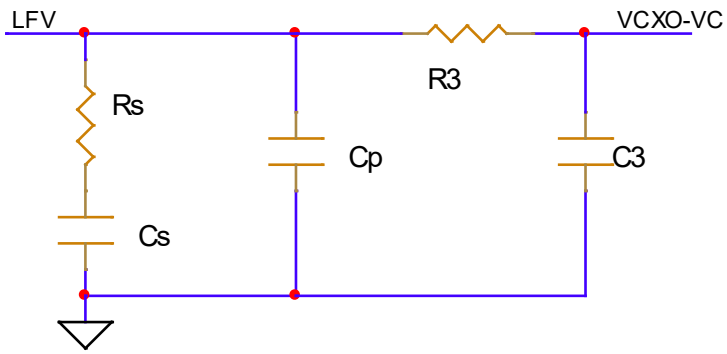

Figure 9. Typical 3rd Order Loop Filter

The Rs, Cs, and Cp are actual chosen standard values from the 2nd order loop filter. In this example, the actual chosen values are Rs = 24kOhm, Cs = 10µF, and Cp = 47nF. The following equation will help determine the 3rd order loop filter R3 and C3.

Pick an R3 value. Suggested: R3 ~ 0.5xRs to ~2.5xRs or greater (R3 = 36kOhm is used in this example).

- C3 can be calculated using the following equation:

$$C3 = \frac{Rs*Cp}{R3*\gamma}$$

Pick γ = 3 in this example.

C3 is calculated to be 10.44nF. A smaller standard capacitor value can be used.

Loop filter calculation tools are available using the same concept as the above calculations. The tool can be used for calculating loop component values after target loop filter is set. The calculated value may not be standard component values but can be chosen using the closest available standard values. After the closest standard values are selected, the final standard values can be entered by overwriting the existing default values and checking the phase noise margin to make sure the PLL is operating in a stable region.

The PM (phase margin) must be above 50 degrees for the PLL to be stable. Keeping the phase margin at approximately 65 degrees is recommended.

6. PLL Loop Filter and Loop Bandwidth Calculation: Examples and Lab Experiments

6.1 Lab Experiment Condition

The same loop filter example will be used for the lab experiment under the conditions of the following components and lab equipment:

Figure 10 shows the tool performs loop calculation as described in this document. Figure 11 shows the loop filter schematic applied in the board used for this experiment.

VCXO PLL of 8V19N491-24, the block diagram is shown in Figure 7. The function of this VCXO PLL is used for cleaning up the REF CLK input phase noise. For simplification, the CLK input frequency of 122.88MHz, VCXO = 122.88MHz and PLL output frequency of 122.88MHz will be used. All the phase noises in the same frequency without scaling the phase noise of each stage is observed.

REF CLK input source used in this example is Tektronix AFG3252. The frequency is set at 122.88MHz sinewave. The phase noise profile is shown in Figure 12. This is high-phase noise source. The effect of VCXO PLL clean up can be clearly observed.

VCXO = 122.88MHz Epson VG3225EFN, Kvco ~ 9kHz/V. The VCO gain, Kvco, can be estimated from the pull range ±ppm provided in the datasheet. The VCXO gain can also be measured in the lab by sweeping VCXO control voltage and output frequency curve. The VCXO open loop phase noise performance is shown in Figure 13. The overlap VCXO phase noise and REF CLK phase noise comparison is shown in the Figure 14. Both are at 122.88MHz.

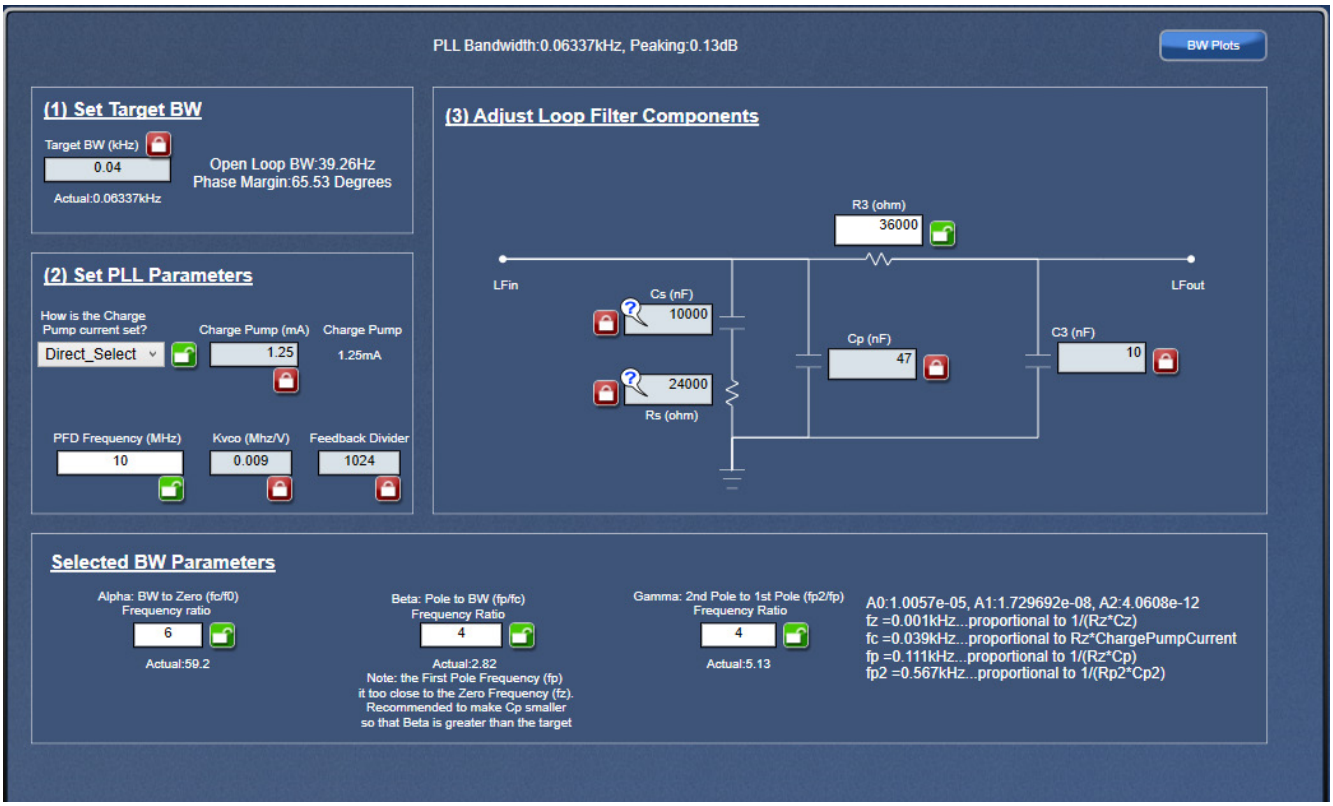

Figure 10. Loop Filter Calculation Tool Example

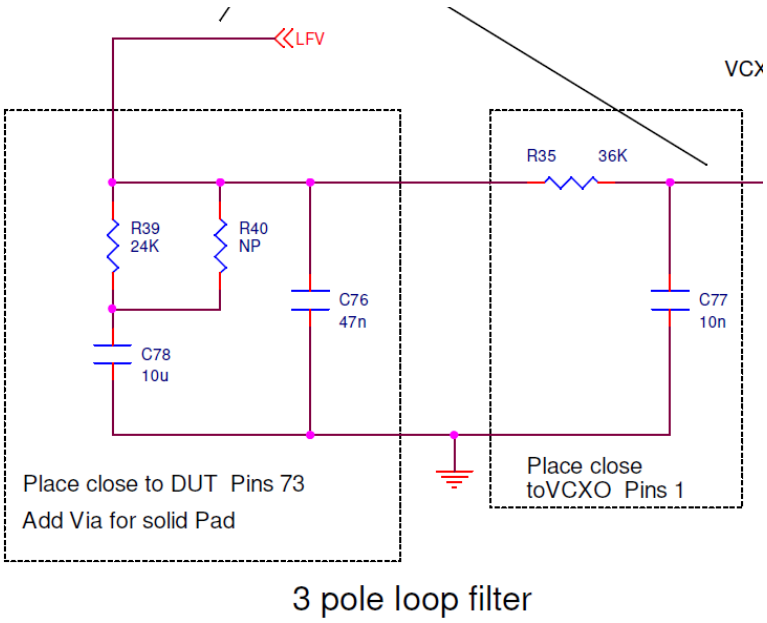

Figure 11. VCXO PLL Loop Filter Values used on the 8V19N491-24 Board

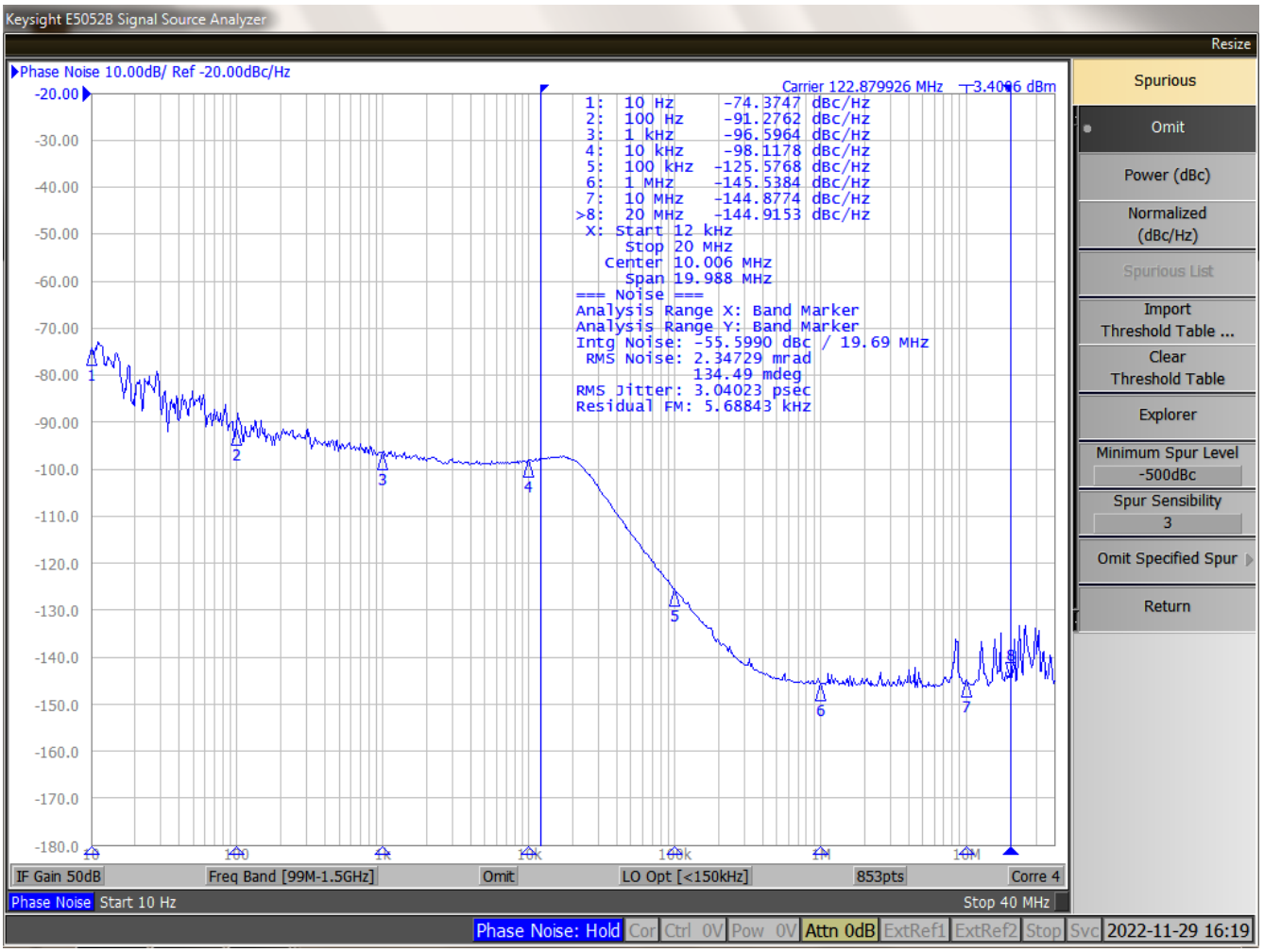

Figure 12. AFG3252=122.88MHz Phase Noise Used as PLL Reference CLK Input Signal Source

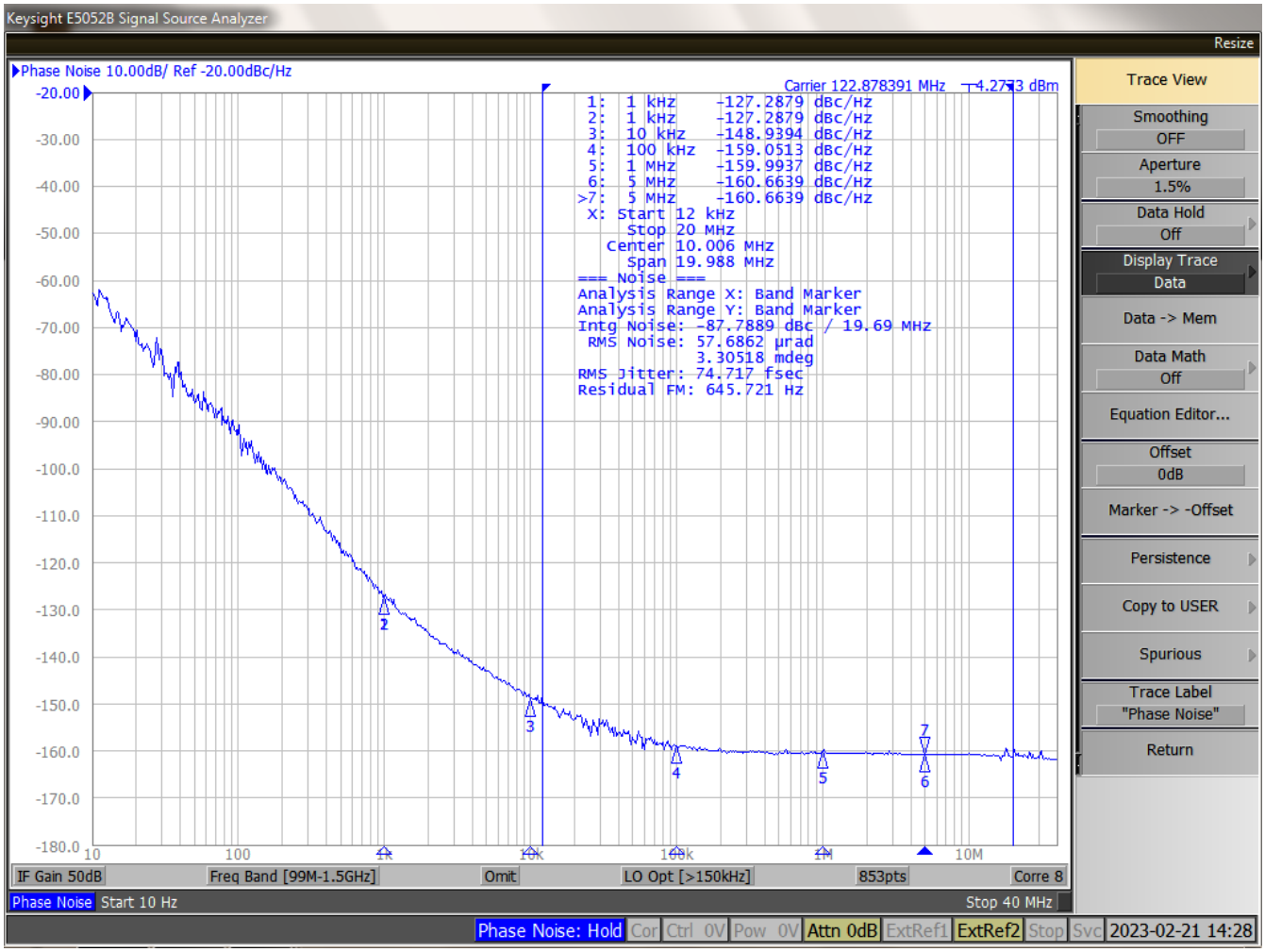

Figure 13. VG3225EFN VCXO Open Loop Phase Noise Performance

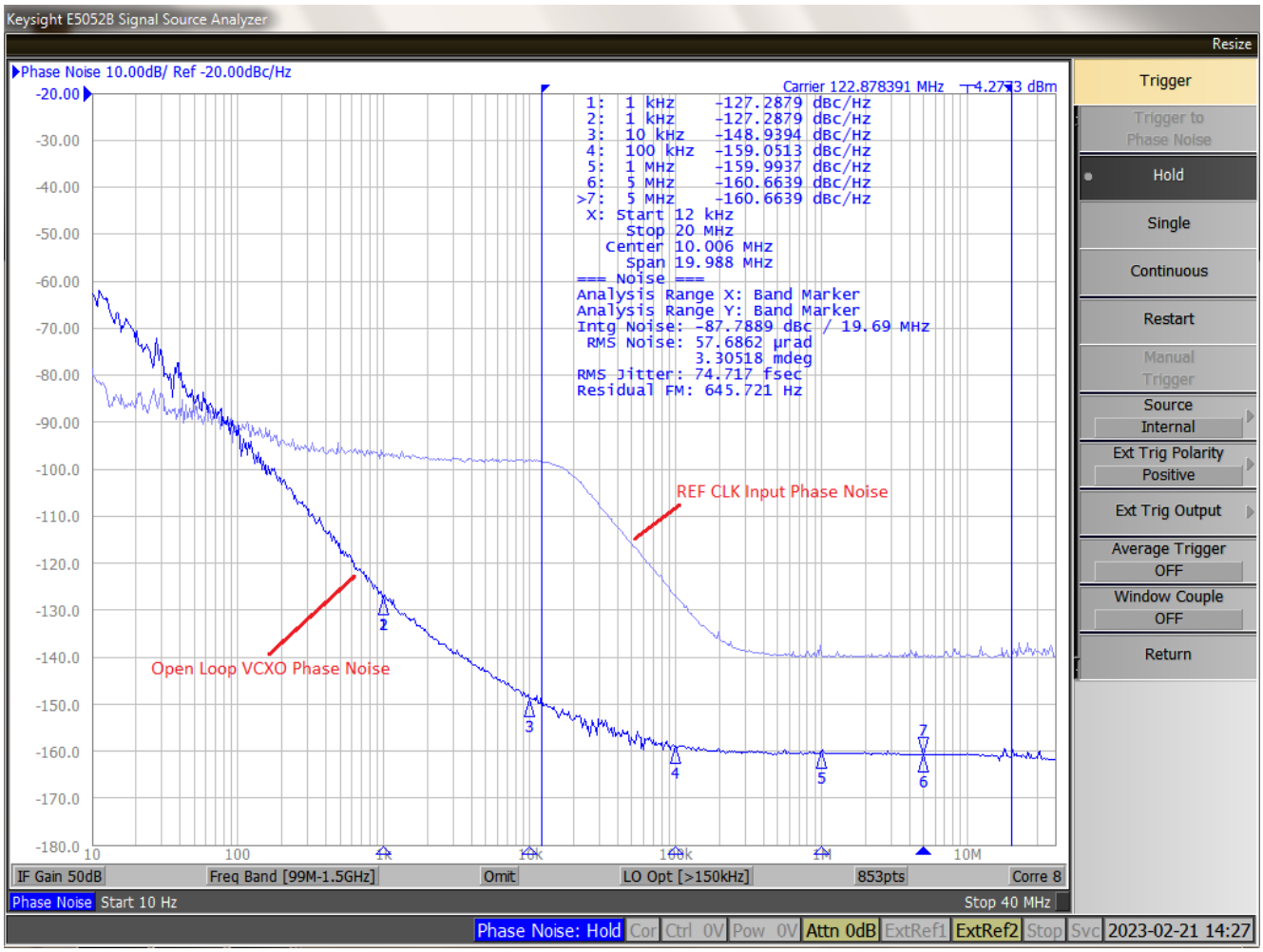

Figure 14. Open Loop VCXO Phase Noise vs AFG3252 REF CLK Input – both at 122.88MHz

6.2 Loop Bandwidth and Phase Noise Fine Tuning

Once the loop filter values are determined, the loop bandwidth can be adjusted further by setting charge current and feedback dividers. Proper setting of the charge pump current and feedback divider is required to assure the loop bandwidth operates at the stable region. Slightly adjusting the loop bandwidth may not be an issue, however, setting loop bandwidth too high or too low may cause issue. In the following experiments, we intentionally increase and decrease the loop bandwidth too high or too low to demonstrate the issue that may be encountered if the loop bandwidth is not set properly. Properly set loop bandwidth phase noise plots are also provided to demonstrate the optimized results.

- Experiment 1 – Loop Bandwidth Set Too High
- Experiment 2 – Loop Bandwidth Too Low
- Experiment 3 – Optimized Loop Bandwidth

6.2.1. Experiment 1 – Loop Bandwidth Set Too High

This experiment demonstrates the effect of loop bandwidth being set too high. In this experiment, the loop bandwidth is increased by increasing charge pump current and reducing the feedback divider. The results in Figure 15 and Figure 16 show that increasing the loop bandwidth to approximately 133Hz will allow more REF CLK phase noise pass through the PLL. The VCXO performance should have been able to be clean up this region.

Another issue in the example is the phase margin is approximately 26 degrees. This is far below the recommended 50 degrees. Phase margin too low is caused by the loop bandwidth being set to too high and close to the pole frequency Fp = 1/(2*pi*Rs*Cp) = 141Hz. This indicates that the PLL is operating in an unstable region and causing peaking at ~200Hz region. To reduce the loop bandwidth, the setting needs to be more than 3 times below the pole frequency.

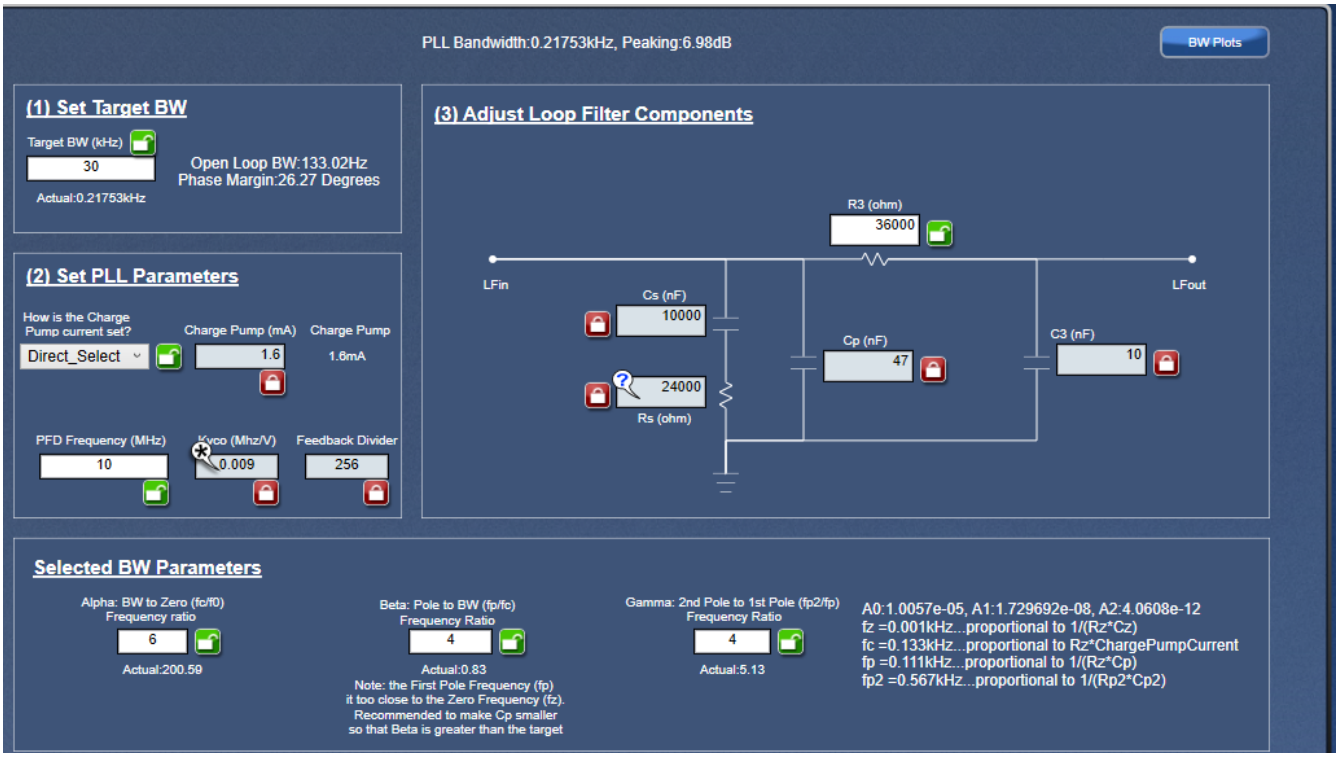

Figure 15. Loop Bandwidth and Phase Margin Result for Increasing Loop Bandwidth

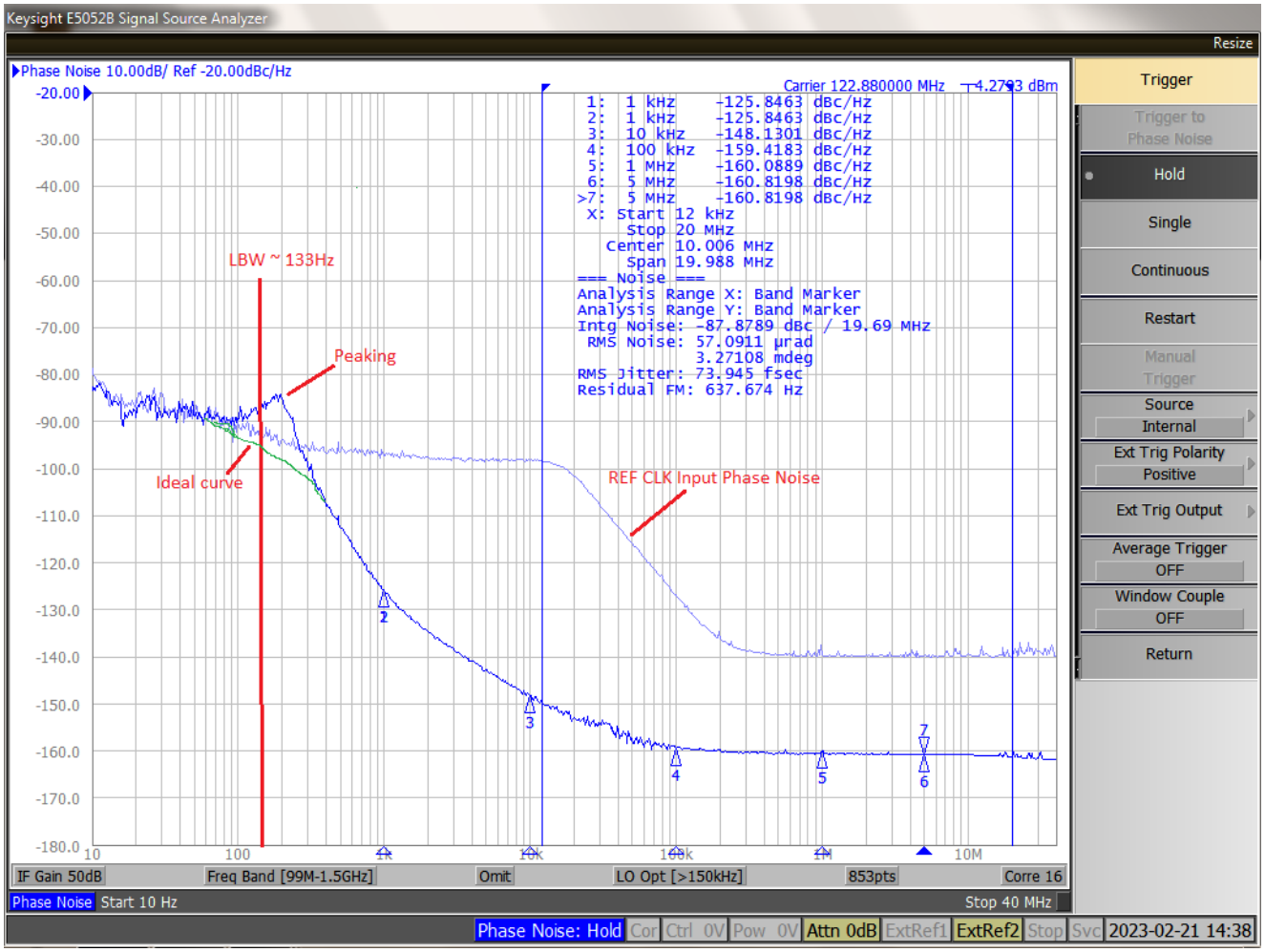

Figure 16. PLL Output Phase Noise for Loop Bandwidth Set Too High

6.2.2. Experiment 2 – Loop Bandwidth Set Too Low

This experiment demonstrates the effect of setting the loop bandwidth too low. In this experiment, the loop bandwidth is decreased by decreasing charge pump current. The results of this example in Figure 17 and Figure 18 show that decreasing the loop bandwidth to approximately 7Hz will allow more VCXO phase noise to pass through the PLL. The phase margin is 80 degrees, therefore, a stable PLL is not an issue in this example. In the low frequency region, the VCXO has a lesser performance than the REF CLK phase noise. The PLL output has a lower phase performance at a lower frequency region. The phase noise at the low frequency region can be improved.

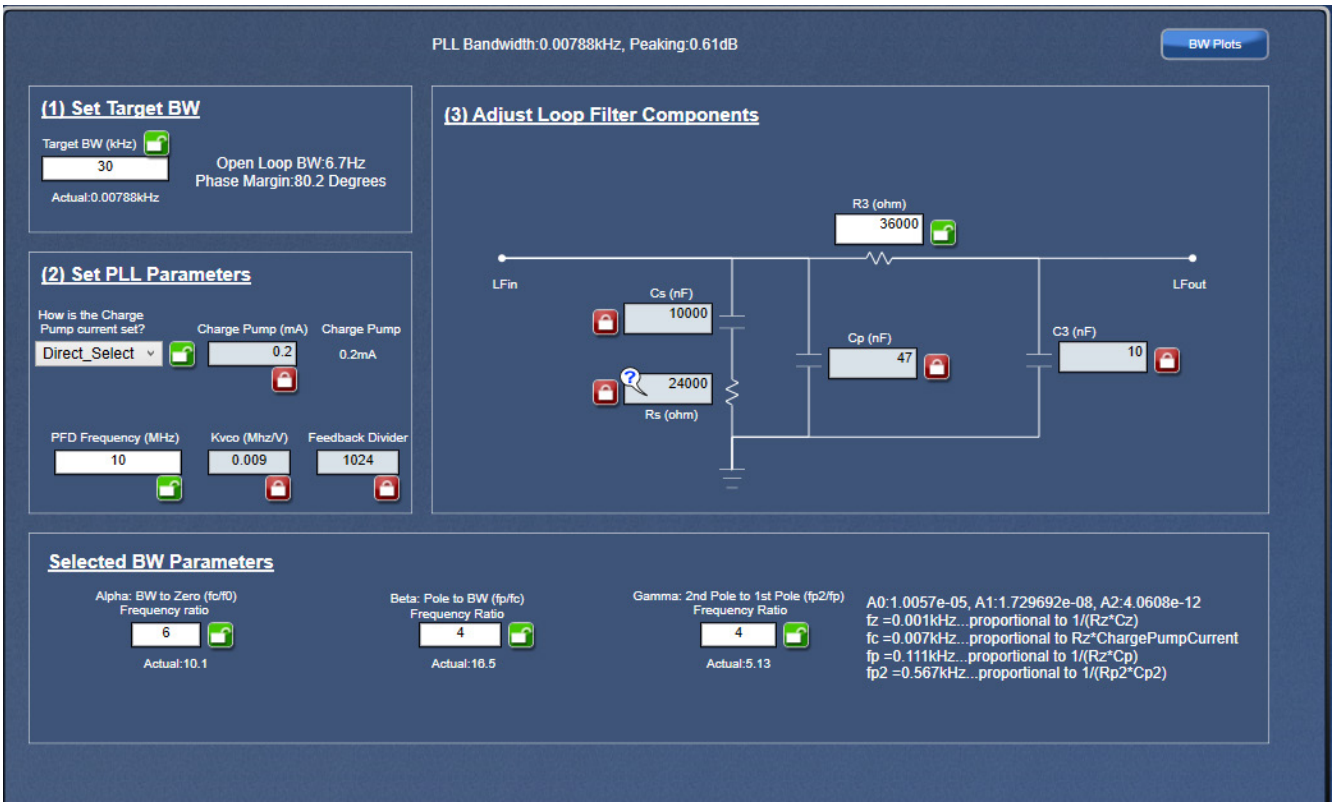

Figure 17. Loop Bandwidth and Phase Margin Result for Setting Loop Bandwidth Too Low

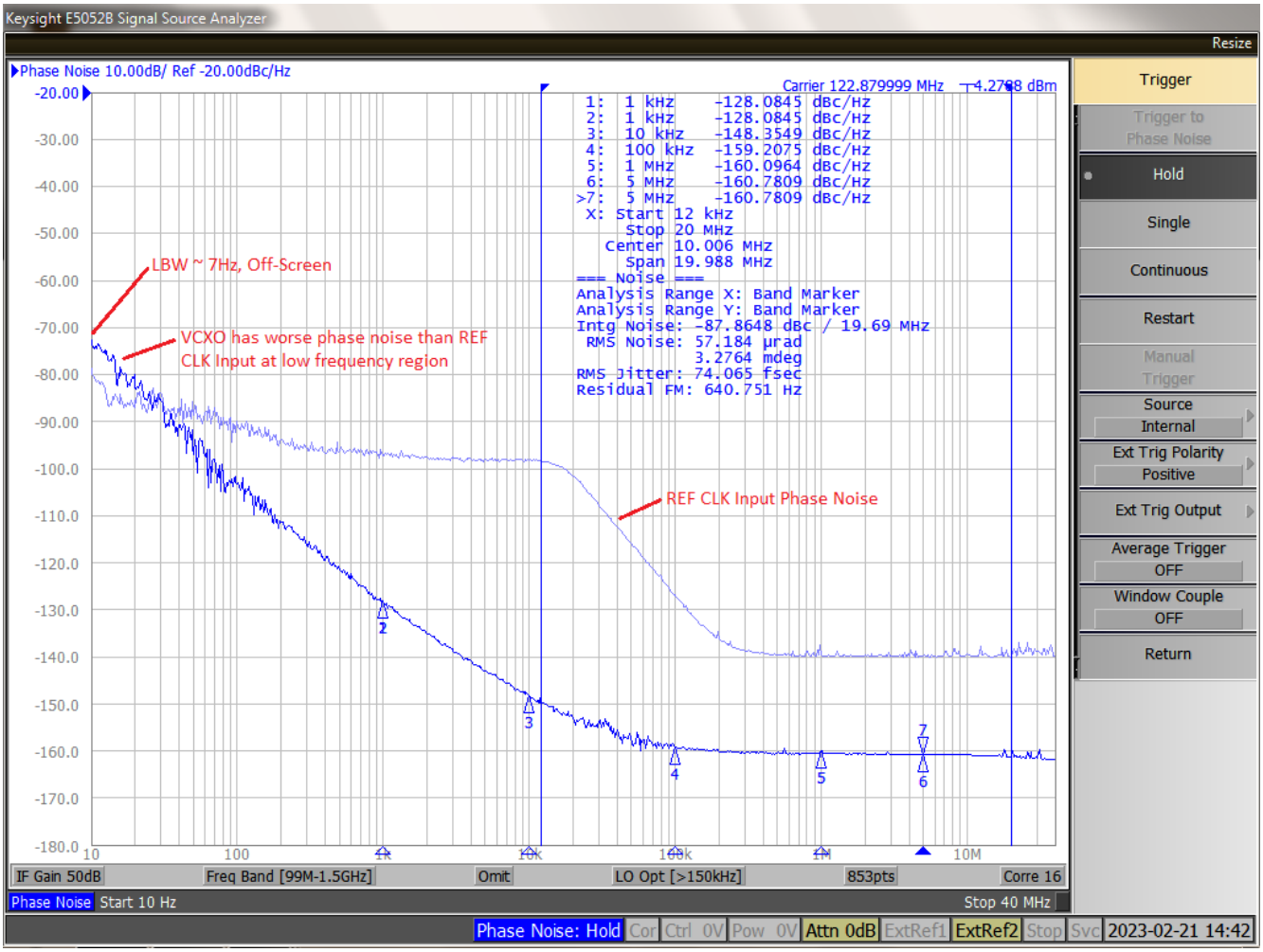

Figure 18. PLL Output Phase Noise for Loop Bandwidth Set Too Low

6.2.3. Experiment 3 – Optimized Loop Bandwidth

Figure 19 shows the loop bandwidth is approximately 40Hz, which is the calculated loop filter values. The phase margin is approximately 65 degrees. The phase noise output result in Figure 20 shows the VCXO PLL operating at a stable region and the phase noise cleaned up at the reference clock source.

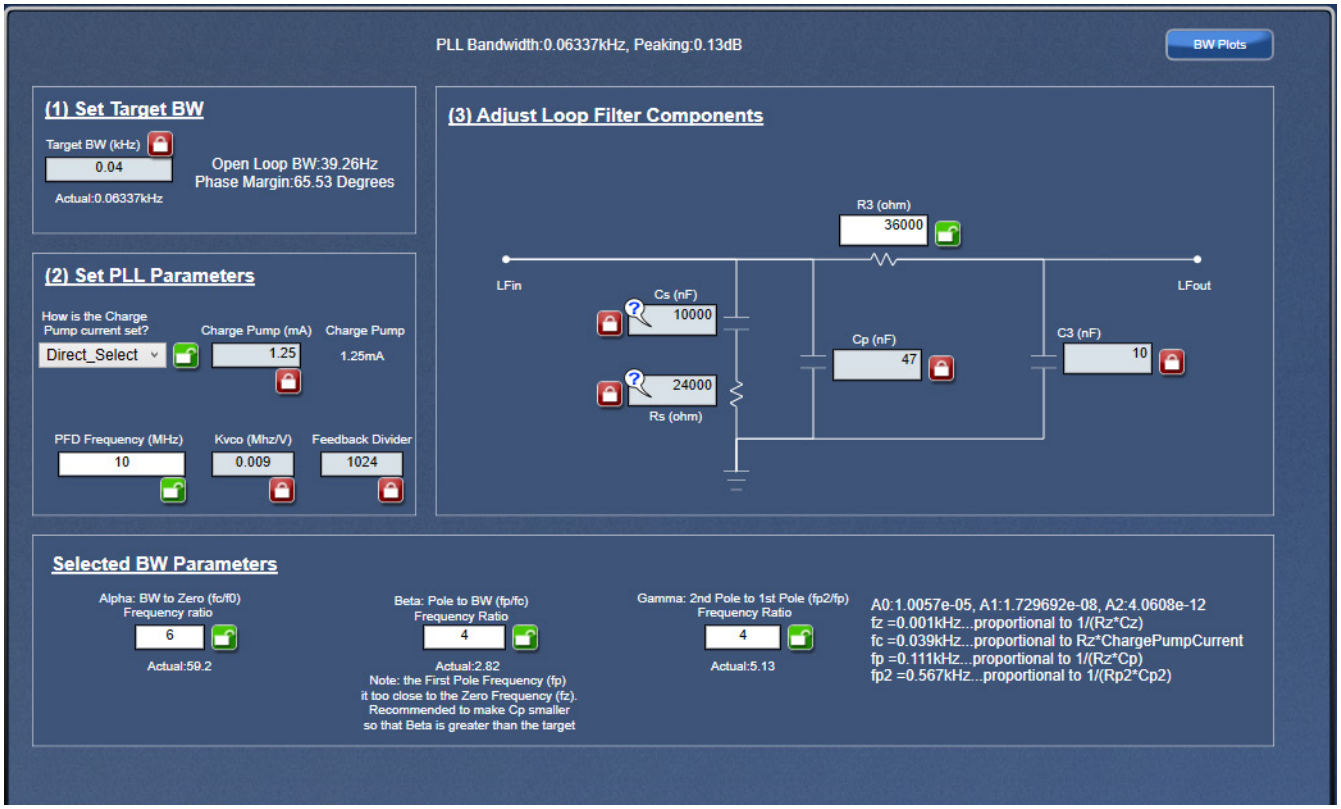

Figure 19. Loop Bandwidth = 40Hz and Phase Margin = 65 degrees

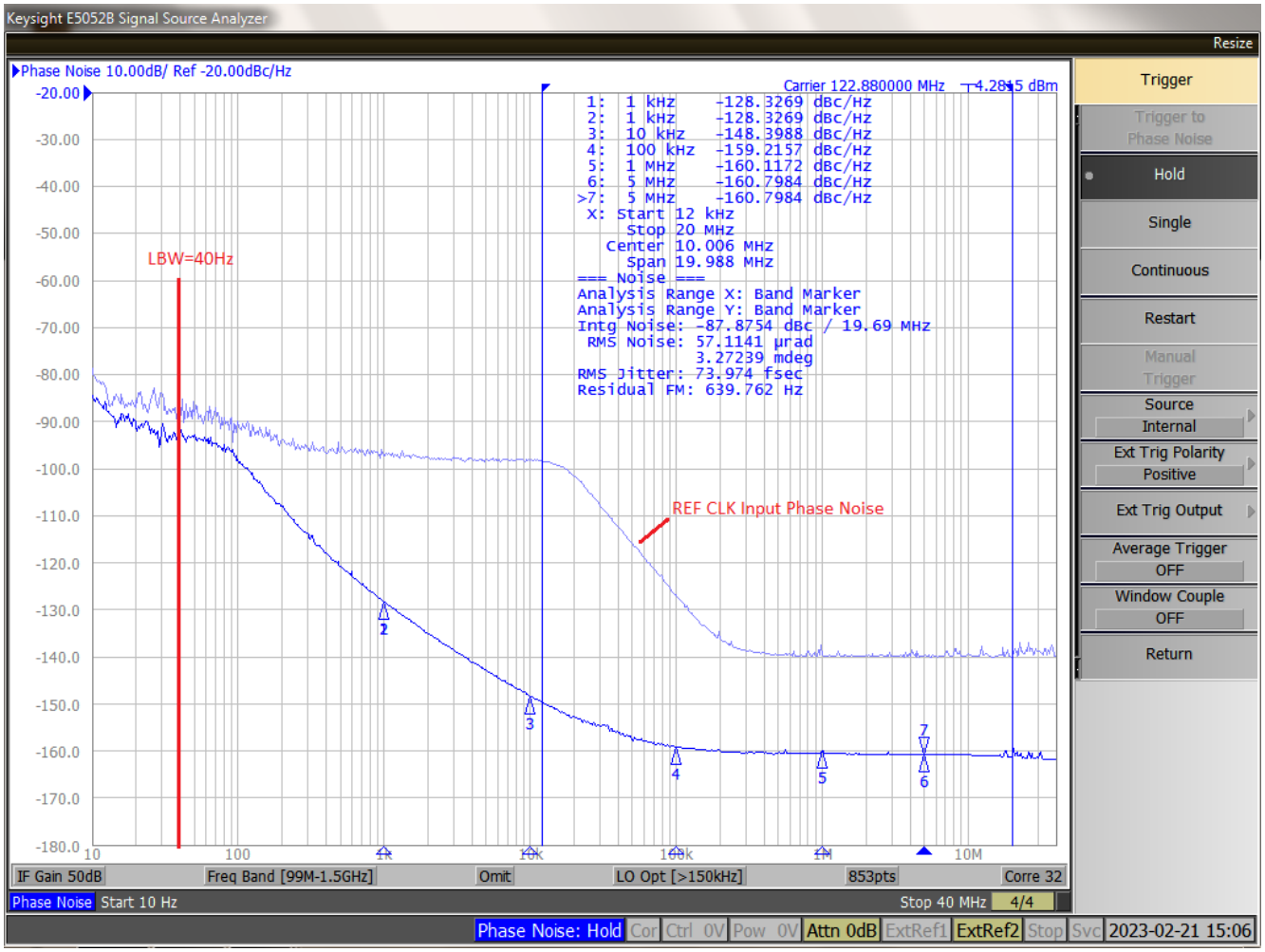

Figure 20. PLL Output Phase Noise with Optimized Loop Bandwidth

7. Revision History

Revision	Date	Description
1.01	Dec 5, 2024	Corrected formula to Rs from Rc in section 4.1 item 3 “Calculate Cs”.
1.00	Feb 28, 2023	Initial release.

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