Application Note

DA9217/DA9121 and DA9220/DA9122 PCB Layout Recommendations

AN-PM-115

Abstract

This application note provides recommendations on how to place and route DA9217/DA9121 and DA9220/DA9122 devices. It also gives guidance on the passive components needed for proper functioning of the system. This document is a guideline only; target applications may have different requirements.

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1 Terms and Definitions

FET	Field effect transistor
GND	Ground
GPIO	General purpose input or output
IC	Integrated circuit
PCB	Printed circuit board
WLCSP	Wafer level chip scale packaging

2 References

[1] DA9217, Datasheet, Dialog Semiconductor.
[2] DA9220, Datasheet, Dialog Semiconductor.
[3] DA9121, Datasheet, Dialog Semiconductor.
[4] DA9122, Datasheet, Dialog Semiconductor.
[5] AN-PM-010, PCB Layout Guidelines for Dialog PMICs, Application Note, Dialog Semiconductor.

3 Introduction

Dialog Semiconductor's DA9217/DA9121 and DA9220/DA9122 devices are power management ICs with integrated power FETs, see datasheets [1][2][3][4]. DA9217/DA9121 is configured as a single channel, dual-phase buck converter, while DA9220/DA9122 is configured as a two-channel, single-phase buck converter.

The input voltage range of 2.5 V to 5.5 V makes DA9217/DA9121 and DA9220/DA09122 suitable for a wide variety of low-voltage systems including 1S Li-Ion battery-supplied applications. The output voltage is configurable in the range of 0.3 V to 1.9 V.

The recommended components and connections for DA9217/DA9121 are shown in Figure 1. DA9220/DA9122's recommended components and connections are shown in Figure 2.

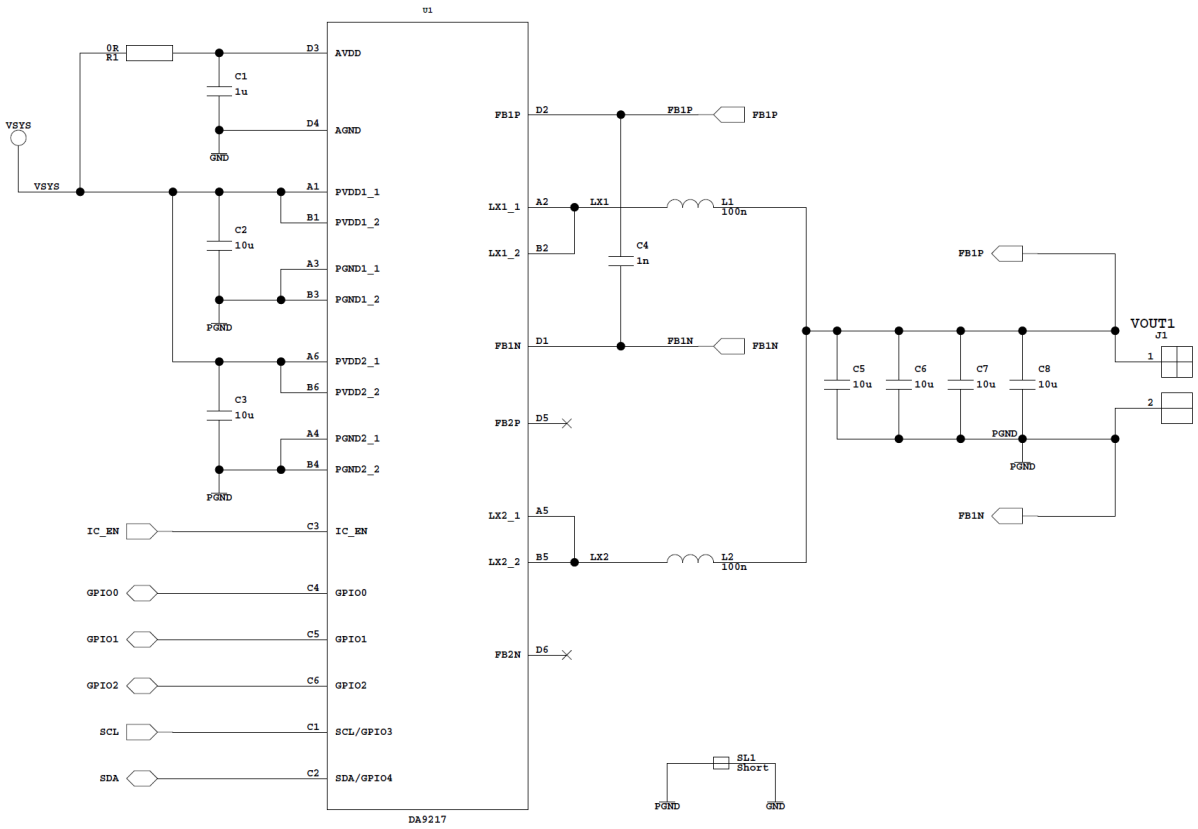

Figure 1: DA9217/DA9121 Recommended Components and Connections

Table 1: DA9217/DA9121 Recommended Components

Application	Part Reference	Value	Temp. Char.	Voltage Rating	ISAT and ITEMP
AVDD Bypass Cap	C1	1 µF	X5R or better	16 V or above	N/A
PVDD Bypass Cap	C2, C3	10 µF	X5R or better	16 V or above	N/A
VOUT Bypass Cap	C5, C6, C7, C8	10 µF	X5R or better	6.3 V or above	N/A
FB Bypass Cap	C4	1 nF	X5R or better	6.3 V or above	N/A
Output Inductor	L1, L2	100 nH	N/A	N/A	4.5 A or above for 3 A per-phase maximum load current. 6.5 A or above for

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Application	Part Reference	Value	Temp. Char.	Voltage Rating	ISAT and ITEMP
					5 A per-phase maximum load current.

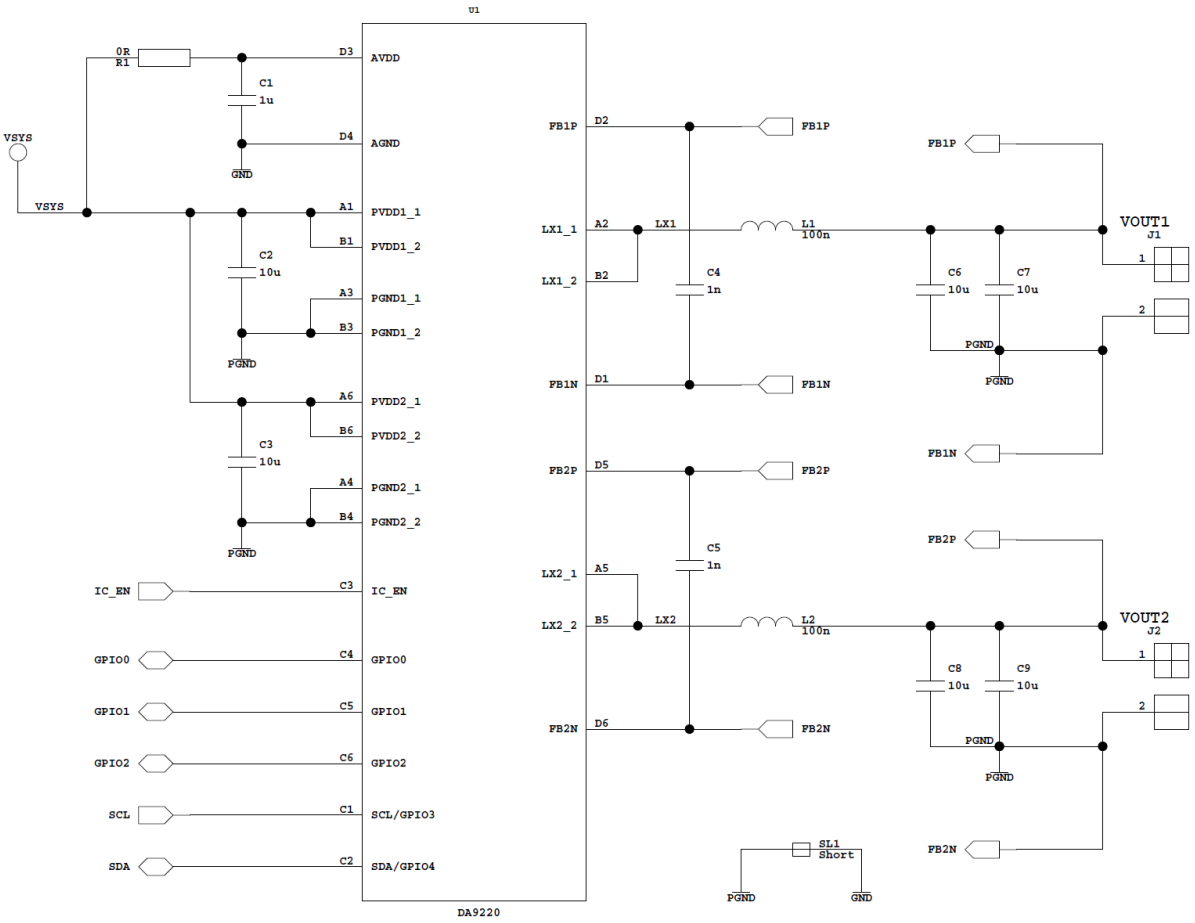


Figure 2: DA9220/DA9122 Recommended Components and Connections

Table 2: DA9220/DA9122 Recommended Components

Application	Part Reference	Value	Temp. Char.	Voltage Rating	ISAT and ITEMP
AVDD Bypass Cap	C1	1 µF	X5R or better	16 V or above	N/A
PVDD Bypass Cap	C2, C3	10 µF	X5R or better	16 V or above	N/A
VOUT Bypass Cap	C6, C7, C8, C9	10 µF	X5R or better	6.3 V or above	N/A
FB Bypass Cap	C4, C5	1 nF	X5R or better	6.3 V or above	N/A
Output Inductor	L1, L2	100 nH	N/A	N/A	4.5 A or above for 3 A maximum load current. 6.5 A or above for 5 A maximum load current.

4 Layout Recommendations

DA9217/DA9121 and DA9220/DA9122 are packaged in a 24-pin WLCSP package with a 0.4 mm pitch.

At least a four-layer PCB stack-up should be used for best PCB layout design. However, the number of routing layers and other PCB parameters are also determined by the other devices in the system.

These recommendations are with reference to the Dialog DA9217/DA9121 or DA9220/DA9122 Evaluation Board, a six-layer PCB. General PMIC layout guidelines are provided in AN-PM-010 [5].

4.1 DA9217/DA9121 and DA9220/DA9122 Package Information

4.1.1 Ball Map

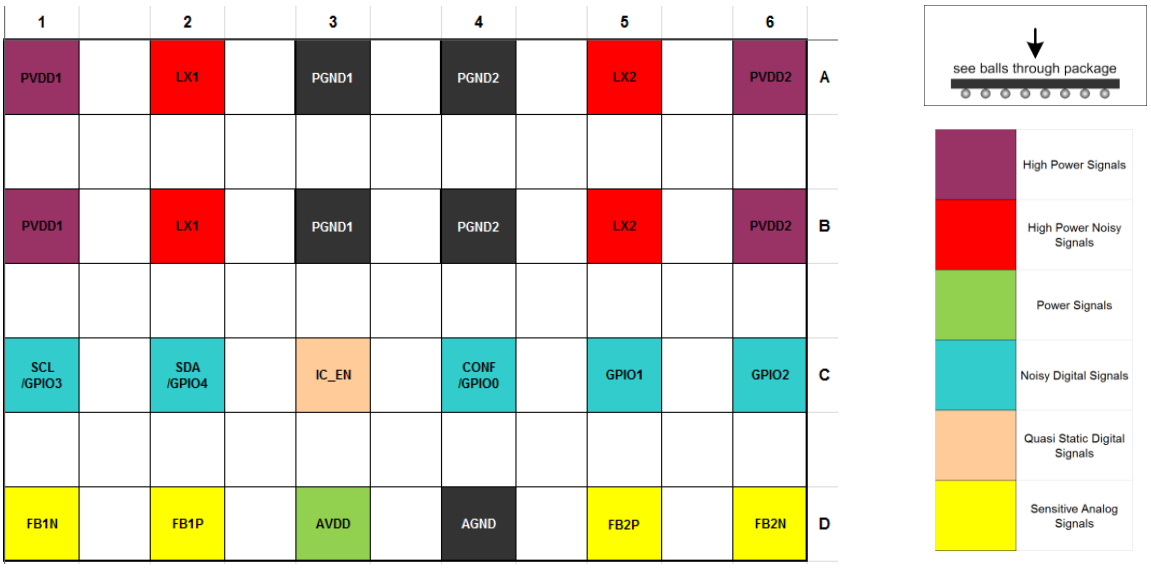
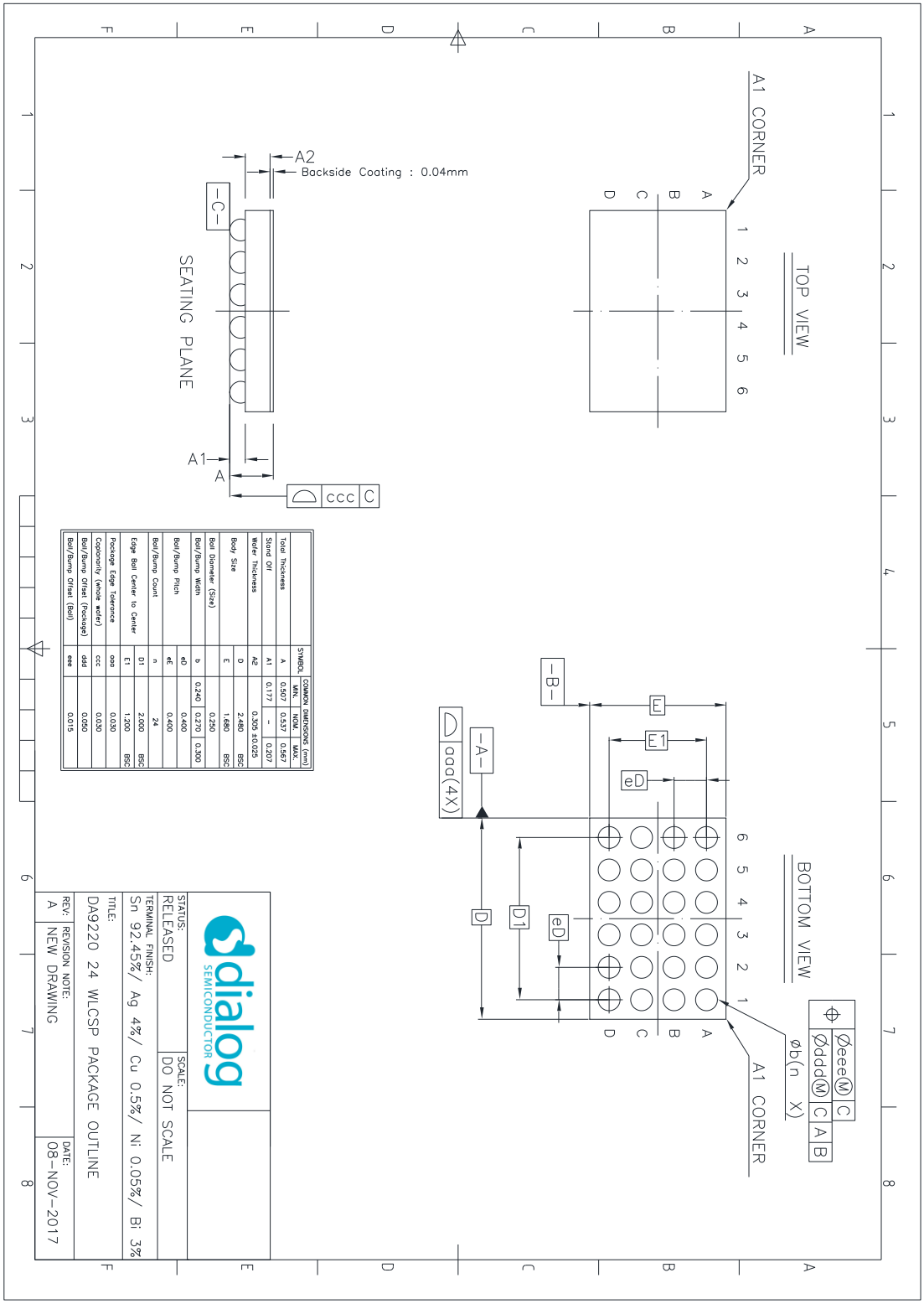


Figure 3: Ball Map

4.1.2 Package Information



	SYMBOL	COMMON DIMENSIONS (mm) MIN.	NOM.	MAX.
Total Thickness	A	0.507	0.537	0.567
Stand Off	A1	0.177	–	0.207
Wafer Thickness	A2		0.305 ±0.025	
Body Size	D		2.480 BSC	
	E		1.680 BSC	
Ball Diameter (Size)	b	0.240	0.270	0.300
Ball/Bump Width			0.250	
Ball/Bump Pitch	eD		0.400	
	eE		0.400	
Ball/Bump Count	n		24	
Edge Ball Center to Center	D1		2.000 BSC	
	E1		1.200 BSC	
Package Edge Tolerance	aaa		0.030	
Coplanarity (Whole wafer)	ccc		0.030	
Ball/Bump Offset (Package)	ddd		0.050	
Ball/Bump Offset (Ball)	eee		0.015	

Figure 4: Package Outline Drawing

4.2 Buck Converter

DA9217/DA9121 and DA9220/DA9122 follow the standard buck layout procedure with output capacitors placed as close as possible to the load. Due to the device's ability to deliver high currents, a wide output trace for minimized parasitic impedance is recommended.

4.2.1 DA9217/DA9121 and DA9220/DA9122 Input

In a buck converter layout, the input capacitor location is critical. Locate the input capacitor as close as possible to the device's input and power GND pins to minimize the parasitic inductance.

In DA9217/DA9121 and DA9220/DA9122 layout design, the input capacitor for each phase should be placed as close as possible to the PVDD<x> and PGND<x> pins, and on the same layer as the DA9217/DA9121 or DA9220/DA9122 device.

If multiple layers are used, it is recommended to use at least two through-hole vias (or at least six microvias) to connect the input voltage (VSYS) between layers to minimize line resistance.

The DA9217/DA9121 and DA9220/DA9122 have separate AVDD supply pins for the internal analog circuits. A 1 µF bypass capacitor should be placed close to the device's AVDD pin. The AVDD pin input and buck converter input (PVDD1 and PVDD2) share the same net, but it is important to separate these traces. Do not connect both traces directly on the same layer.

Ensure that the AVDD pin is connected to the input voltage (VSYS) plane far enough from the buck's input voltage plane so switching noise from the buck converter input (PVDD1 and PVDD2) is not injected to the AVDD pin.

Figure 5 shows the input capacitor placement and routing recommendation.

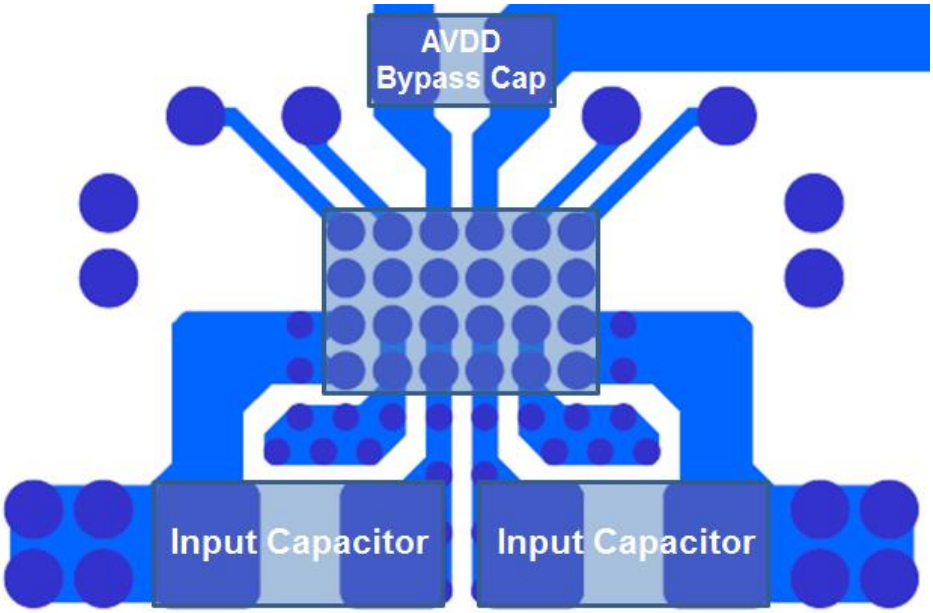


Figure 5: Recommended Input Capacitor Placement and Routing

4.2.2 Ground Connections

Special care should be taken with ground connections because of the high current capability of DA9217/DA9121 and DA9220/DA9122, and because of the device's high-performance requirements.

The power GND terminals (PGND1 and PGND2) of the DA9217/DA9121 and DA9220/DA9122 are placed between each phase's LX pin.

For DA9220/DA9122, it is strongly recommended to separate PGND1 and PGND2 on the component layer and connect them at a solid common GND plane. For DA9217/DA9121, it is not necessary to separate PGND1 and PGND2.

It is best practice to isolate quiet analog GND (AGND) from noisy power GND terminals (PGND1 and PGND2) and to connect them at a single point.

Layer 2 can be used as a return power GND plane, where the device's PGND pins and output capacitor GND can be connected. It is recommended to minimize the line impedance of the PGND pins and output capacitor GND connections by using as many vias as possible. This will also improve the heat dissipation.

NOTE
It is always recommended to use copper plugged vias to achieve the minimum parasitic via impedance and best thermal performance.

Examples of how to connect the GND terminals are illustrated in Figure 6 and Figure **7**.

AGND is isolated from the power GND terminals (PGND1 and PGND2) at the top layer (component layer) and connected at a single point on the bottom layer.

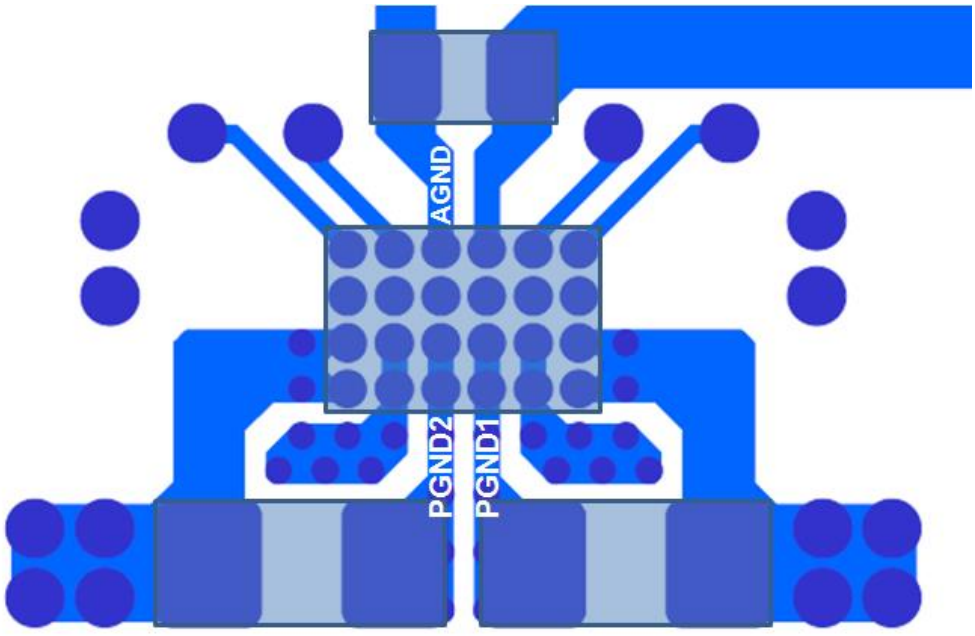


Figure 6: Recommended Grounds Connection for DA9220/DA9122

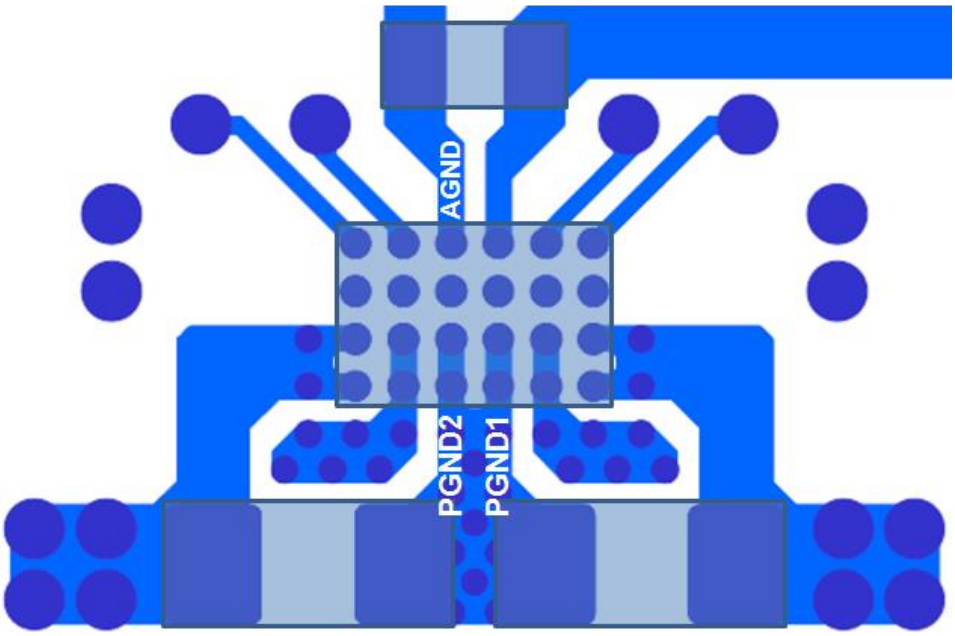


Figure 7: Recommended Grounds Connection for DA9217/DA9121

4.2.3 LX Routing

Switch node/LX node traces (traces between LX pins and output inductors) need to be kept as short as possible since this node generates switching noise, which can interfere with buck converter stability. Very high current will flow through this trace and so the minimum width of trace used for this LX node must be considered. Also, ensure that there are enough vias to deliver the current.

The LX node patterns on Dialog's DA9220/DA9122 Evaluation Board are shown in Figure 8.

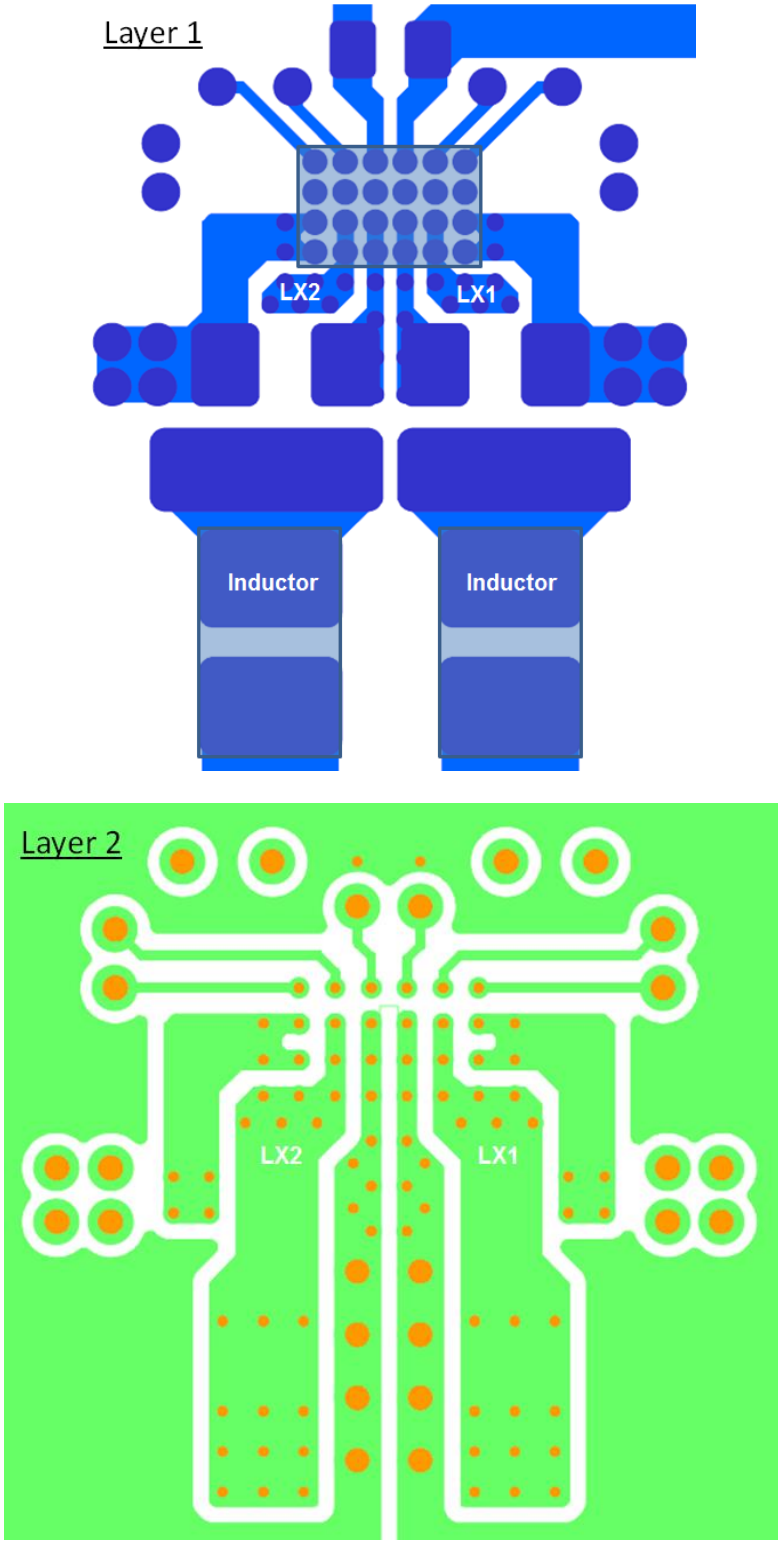


Figure 8: LX Node Pattern on DA9220/DA9122 Evaluation Board

4.2.4 Buck Output

Output capacitors should be placed as close as possible to the load. Do not split the output capacitors into local capacitors (close to the output inductor) and remote capacitors (close to the load) as this may affect the stability of the buck converter.

However, minimizing the distance (which minimizes the line impedance) from the output inductors to the output capacitors (the load) is also important since it directly affects the efficiency and load transient response performance of the buck converter. Care must be taken with the size of the output traces since the output peak current can be up to 10 A for DA9121 and up to 5 A per-channel for DA9122.

It is best practice to transfer the output current at the top layer directly without using any vias. This will give the best performance in terms of efficiency and load transient response performance.

4.2.5 Feedback Lines

Feedback lines must be routed as a differential pair far from any noise source (for example, output inductors, LX node, and so on). It is strongly recommended to place a bypass capacitor (typically 1 nF) between the positive and negative sides of the differential feedback. The bypass capacitor should be placed as close as possible to the IC. It is useful for filtering noise which may be injected to the feedback lines due to a layout limitation (for example, a long feedback pattern or noise from other devices in the system).

Also, ensure that the feedback lines are not overlapping any noisy node traces (for example, the LX node trace) without an insulation plane in between. If DA9217/DA9121 or DA9220/DA9122 is assembled on the top layer, it is recommended to route the feedback lines on Layer 4 or below when the traces are near to the IC and the switch node areas.

NOTE

- The negative feedback trace is at ground potential and care should be taken not to connect any part of the trace to the ground plane.
- The feedback lines must be routed directly from the load point in order to achieve the best voltage accuracy and stability.

Examples of output-voltage feedback-line routing, on the Dialog DA9220/DA9122 Evaluation Board, are shown in Figure 9.

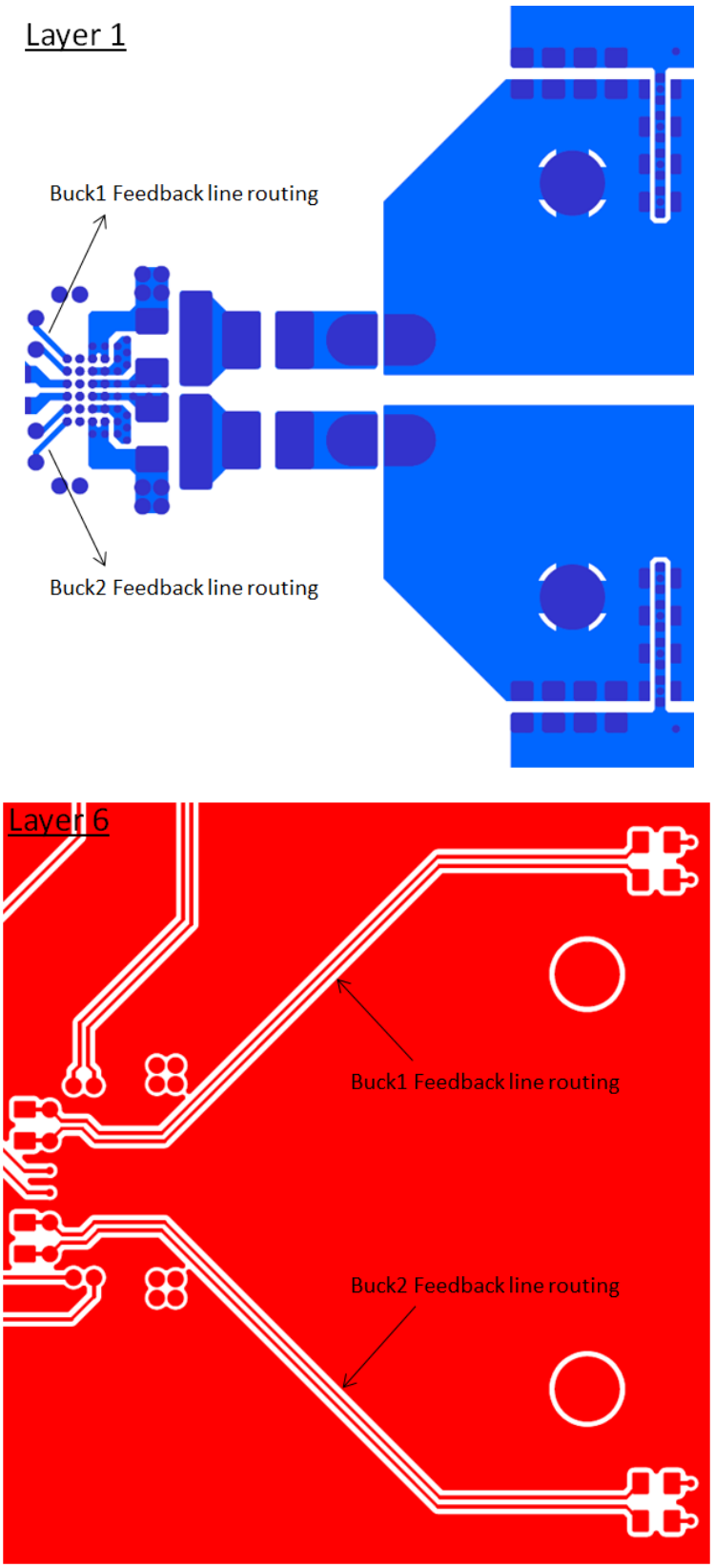


Figure 9: Output Voltage Feedback Line Routing on DA9220/DA9122 Evaluation Board

4.3 Communication Interface (I^2C)

It is recommended to route the communication interface far from any noise source.

Care must also be taken regarding the noise produced by the interface signal in order to avoid coupling to the sensitive analog references and feedbacks. The routing layer is not critical, but it is recommended to use the bottom or top layer.

4.4 GPIO Signals

Generally, GPIOs have the lowest routing priority. Any layer can be used for routing these signals.

However, care must be taken regarding the noise produced by the GPIOs in order to avoid coupling to the sensitive analog references and feedbacks.

Revision History

Revision	Date	Description
0.1	18-Jun-2018	Initial version (draft).
1.0	14-Oct-2019	Released version.
1.1	15-Feb-2022	Rebranded to Renesas.

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Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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