

RZ/G3E Power Estimation Examples

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Information

- The estimation results of power consumption are shown after the next page for reference.
- Please choose the use case which is similar to your application, and refer to the power consumption as a reference.

Target Device

RZ/G3E

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1. Operation Summary in Each Use Case

The power consumption was calculated for three use cases. You choose the use case which is similar to your application, and use the power consumption as a reference.

The estimation conditions of power consumption are shown below.

- $T_j = 65^{\circ}\text{C}$
- Voltage level of each power supply group

The relationship between the power supply pins and the power supply groups is shown in **Table 1.2**.

Power supply group (0.8-V Core, PHY, etc) = 0.8 V,

Power supply group (0.9/0.8-V Core, etc) = 0.9 V,

Power supply group (1.2-V MIPI DSI) = 1.2 V,

Power supply group (1.1-V DDR I/O) = 1.1 V,

Power supply group (1.1/0.6-V DDR I/O) = 0.6 V,

Power supply group (1.8-V I/O, PHY, etc and 1.8/1.2-V I/O) = 1.8 V,

Power supply group (3.3-V USB and 3.3/1.8-V I/O) = 3.3 V

- Process = TT process silicon
- CPU: Cortex-A55@1.8 GHz, LPDDR4X-3200 32bit × 1ch

Table 1.1 Operation Summary of Each Use Case

Use Case	Operation Summary
UseCase1	Use case assuming the below condition • Cortex-A55 (4Core): use rate 50% • System/Bus/Clock: use rate 25% • DDR(LPDDR4X): use rate 10% • AWO Domain: use rate 25%
UseCase2	Use case assuming the below condition • Cortex-A55 (4Core): use rate 40% • Cortex-M33: use rate 10% • System/Bus/Clock: use rate 50% • GE3D*¹: use rate 40% • VSP*²: use rate 40% • DSI*³: use rate 75% • DDR(LPDDR4X): use rate 40% • ADC: use rate 30% • SD: use rate 30% • xSPI: use rate 10%
UseCase3	Use case assuming the below condition • Cortex-A55 (4Core): use rate 55% • Cortex-M33: use rate 10% • System/Bus/Clock: use rate 50% • GE3D*¹: use rate 65% • VSP*²: use rate 80% • DSI*³: use rate 75% • LVDS: use rate 90 • DDR(LPDDR4X): use rate 40% • ADC: use rate 30% • Gbit-Ether: use rate 30% • xSPI: use rate 10%

Note 1. 3D graphics engine

Note 2. Video Signal Processor

Note 3. MIPI DSI Interface

Table 1.2 Power Supply Groups Corresponding to Power Supply Pins

Power Supply Group	Power Supply Pin	Description
0.8-V Core, PHY, etc	VDD08_OTHERS	Power supply for 0.8-V Core (OTHERS and AWO)
	VDD08_AWO	
	PLDVDD08_OTHERS	Power supply for 0.8-V PLL (OTHERS and CM33)
	PLDVDD08_PLLCM33	
	CSI0_MSVDD0P8	Power supply for 0.8-V PHY (MIPI CSI, MIPI DSI, PCIe, and USB)
	DSI_VDD0P8	
	PCIE_VCC08AL01	
	USB2_USDVDD	
	USB30_USVPTX	
0.9/0.8-V Core, etc	VDD09_CA55	Power supply for 0.9/0.8-V Core (CA55)
	PLDVDD09_PLLCA55	Power supply for 0.9/0.8-V PLL (CA55)
1.2-V MIPI DSI	DSI_VDD12	Power supply for 1.2-V PHY(MIPI DSI)
1.1-V DDR I/O	DDR0_VDDQ	Power supply for 1.1-V PHY(DDR I/O)
1.1/0.6-V DDR I/O	DDR0_VDDQLP	Power supply for 1.1/0.6-V PHY(DDR I/O)
1.8-V I/O, PHY, etc	CSI0_MSVDD18	Power supply for 1.8-V PHY (MIPI CSI, MIPI DSI, PCIe, and USB)
	DSI_VDD18	
	PCIE_VCC18AL01	
	PCIE_VCC18ACMN	
	USB20_USVDD18	
	USB21_USVDD18	
	USB30_USVPH	
	USB30_USVDD18	
	PLVDD_OTHERS	Power supply for 1.8-V PLL (OTHERS, CA55, CM33, and DDR)
	PLVDD_PLLCA55	
	PLVDD_PLLCM33	
	DDR0_VAA	
	OTPVDD18	Power supply for 1.8-V OTP
	ADAVDD18	Analog power supply for 1.8-V ADC
	LVDS_VCCQ	Power supply for 1.8-V I/O (LVDS, AWO, and PWC)
	VDD18_AWO	
	VDD18_PWC	
	VDD1833_PRE18_OTHERS_1	Pre-driver power supply for OTHERS and AWO
	VDD1833_PRE18_AWO	
	VDD1833_PRE18_OTHERS_2	Pre-driver power supply for SD/MMC and Ether
1.8/1.2-V I/O	VDD1218_I3C	Power supply for 1.8/1.2-V switching I/O
3.3-V USB	USB2_USVDD33	Power supply for 3.3-V PHY (USB)
3.3/1.8-V I/O	VDD1833_OTHERS	Power supply for 3.3/1.8-V switching I/O
	VDD1833_AWO	
	VDD1833_ET0	
	VDD1833_ET1	
	VDD1833_SD0	
	VDD1833_SD1	
	VDD1833_SD2	
	VDD1833_XSPI	

2. Power consumption in each use case

The estimation result of power consumption in each use case is shown in **Table 2.1**.

Table 2.1 Power Consumption in Each Use Case

								Unit: [W]
Use Case	0.8 V	0.9 V	1.2 V	1.1 V	0.6 V	1.8 V	3.3 V	Total
UseCase1	0.25	1.04	0.00	0.03	0.01	0.02	0.01	1.36
UseCase2	0.97	1.04	0.01	0.13	0.06	0.08	0.07	2.36
UseCase3	1.13	1.14	0.01	0.13	0.06	0.20	0.05	2.72

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

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