Power MOS FET

Absolute Maximum Ratings and Electrical Characteristics

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1. Absolute Maximum Ratings and Electrical Characteristics

1.1 Absolute Maximum Ratings

The following absolute maximum rating items are stipulated independently of each other: Sustained drain-source voltage V_{DSS}

Drain current I_D

Channel dissipation Pch

Also, these items express rating values which cannot be exceeded no matter what the service condition. In many cases, absolute maximum rating items are closely interrelated with other characteristics, and so correct operation cannot be guaranteed when two or more values are at their maximum rated levels.

(1) Drain-Source Voltage V_{DSS}

When a short-circuit is created between the gate and source, the resulting applied voltage between the drain and source is at its maximum value. V_{DSS} varies along with temperature. A shown if Figure 1, a rise in junction temperature Tj above 100°C causes a corresponding increase in $V_{(BR)DSS}$ of approximately 10%. It should also be noted that a drop in Tj causes a proportional drop in $V_{(BR)DSS}$.

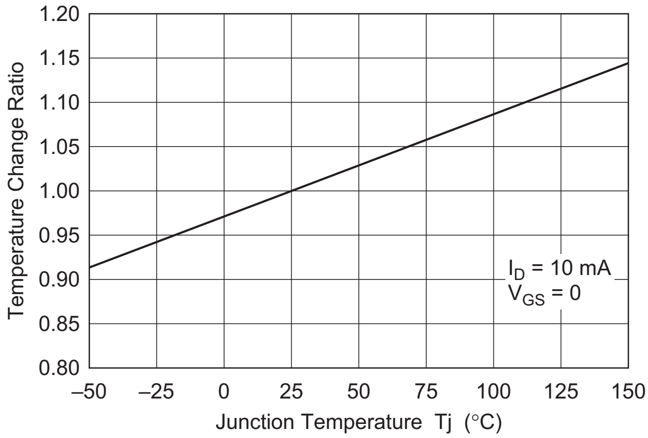


Figure 1 Change in $V_{(BR)DSS}$ Relative to Junction Temperature

(2) Gate-Source voltage V_{GSS}

The device incorporating a protection diode is assumed for the case when a short-circuit is created between the drain and source, The protection diode must be included in the device.

(3) Drain current I_D and drain peak current $I_{D(peak)}$ or $I_{D(pulse)}$

The peak value of the DC drain current is expressed by $I_{D(peak)}$ or $I_{D(pulse)}$, under the limitations imposed by the allowable channel loss, and assuming that the maximum value of the continuous DC to the drain does not exceed I_D and the average current does not exceed I_D.

The generally allowable I_D value during operation can be calculated using the following formula.

$$I_{Dmax.} = \sqrt{\frac{\text{Tch max.} - \text{Tc}}{\theta\text{ch} - \text{c} \cdot R_{DS(on)}\text{max.}}} \text{(A)} \quad \cdots\cdots (1)$$

Similarly, the allowable $I_{D(peak)}$ value can be calculated as shown below.

$$I_{D(peak)}\text{max.} = \sqrt{\frac{\text{Tch max.} - \text{Tc}}{\theta\text{ch} - \text{c(t)} \cdot R_{DS(on)}\text{max.}}} \text{(A)} \quad \cdots\cdots (2)$$

Tch max.: Maximum channel temperatures (150°C)

Tc: Case temperatures

θch–c: DC thermal impedance
θch–c(t): transient thermal impedance
$R_{DS(on)}$max.: maximum drain-source on-resistance value
$\gamma_{S(t)}$: normalized transient thermal impedance (here, 1 shot pulse)

The following formula can be used to obtain pulse width PW and θch-c(t) for duty cycle n%.

$$\theta ch - c_{(t)} = \theta ch - c\left\{\frac{n}{100} + \left(1 - \frac{n}{100}\right)\gamma_{S(t)}\right\} \quad \cdots\cdots (3)$$

The $R_{DS(on)}$ in formulas (1) and (2) takes waste conditions into consideration, and the $R_{DS(on)}$ max value at Tch = 150°C (in accordance with the $R_{DS(on)} - T_C$ characteristics curve of the data sheet) is used.

Calculation example:

Calculate the $I_{D(peak)}$ allowable value when the 2SK1166 is used under the conditions PW = 10 µs, duty = 10%, T_C = 80°C.

(i) According to the transient thermal impedance shown on the data sheet (Fig 2), PW = 10 µs and duty = 10% result in $\gamma_{s(t)} \cong 0.12$. Therefore, θch-c$_{(t)}$ = γs(t), and θch-c = 0.12 × 1.25 = 0.15°C / W.

(ii) According to the data sheet, the $R_{DS(on)}$ maximum value for 0.6 Ω and Tch = 150°C is approximately 2.4 × 0.6 = 1.44 Ω.

Substituting the above values in Formula (2) results in the following calculation of the approximate value 18 A.

$$I_{D(peak)} = \sqrt{\frac{150 - 80}{0.15 \times 1.44}} \cong 18A$$

Important

The $R_{DS(on)}$ value is based upon values obtained under the test conditions noted in the catalog. $R_{DS(on)}$ should be confirmed under actual $I_{D(peak)}$ conditions.

(4) Reverse drain current I_{DR}

Reverse drain current I_{DR} represents the maximum value of the reverse direct current flowing continuously to the equivalent built-in diode formed between the source and drain, within the limitations imposed by the allowable channel loss. In applications such as H bridge circuit output for motor control, the built-in diode is equivalent to a commutation diode. However, breakdown can occur depending on the circuit operating conditions, so the precautions in handling the built-in diode outlined in section 8.1 should be noted.

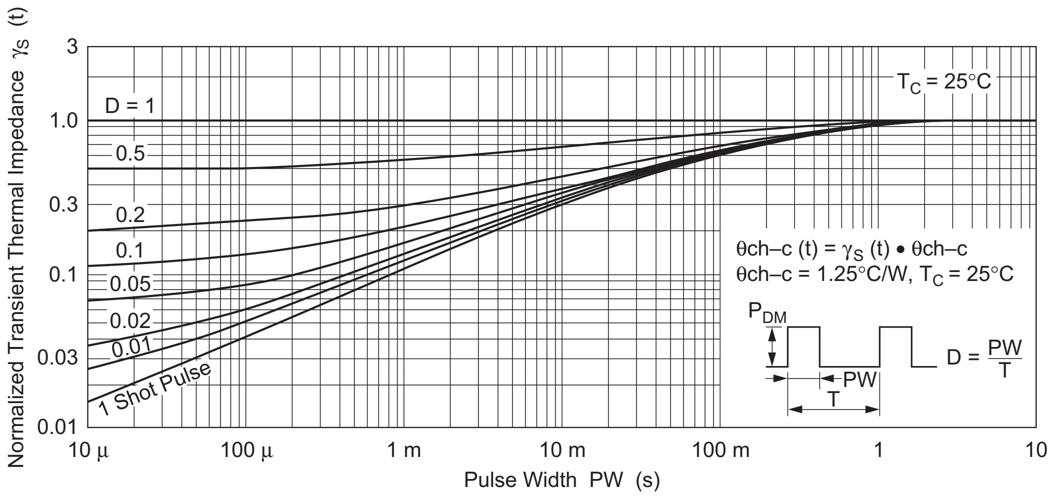


Figure 2 2SK1165, 2SK1166 Transient Thermal Impedance Characteristics (Data Sheet)

(5) Channel dissipation Pch or P_D

Allowable channel dissipation is the drain loss maximum value continuously consumed by the transistor within the limitations imposed by the prescribed heat dissipation conditions. Derating in accordance with the following formula is required in accordance with case temperature T_C.

$$Pch(Tc) = Pch_{(25°C)} \times \frac{Tch\ \ max. - Tc}{Tch\ \ max. - 25} \quad \cdots\cdots (4)$$

Also, the transition duration's allowable channel loss Pch(1) can be calculated using Formula (5) below, in accordance with the transient thermal impedance noted on the data sheet.

$$Pch(t) = \frac{Tch\ max. - Tc}{\theta ch - c(t)} \quad \cdots\cdots (5)$$

Temperature derating is performed using a method similar to Formula. (4).

(6) Channel temperature Tch

As with the transistor's Tj, the allowable channel temperature is the upper limit junction temperature value, which cannot exceed the temperature rise (θch-c • Pd) caused by operating case temperature (T_C) and internal loss (Pd) of the transistor itself, or the sum of such temperatures (T_C + θch-c • Pd).

(7) Storage temperature Tstg

The storage temperature represents the upper and lower ambient temperature limits which the transistor should not exceed when in a non-operational storage condition.

1.2 Electrical Characteristics

(1) Drain-source breakdown voltage $V_{(BR)DSS}$

The test conditions for the drain-source breakdown voltage prescribe I_D and V_{GS} = 0. Temperature fluctuates as previously described.

(2) Gate-source breakdown voltage $V_{(BR)GSS}$

Gate-source breakdown voltage applies to the DII Series, SIII Series and S Series, in which a protect diode is included between the gate and source. Test conditions prescribe I_G (= ±100 µA) and V_{DS} = 0.

(3) Reverse gate current I_{GSS}

Test condition prescribe V_{GS} and V_{DS} = 0. The I_{GSS} for models without a gate protect diode (D Series) is a value of 1 nA or less. Temperature has virtually no affect on this value. For models with a gate protect diode (DII, DIII Series), I_{GSS} is a value in the range of a few hundred nA to 1 µA. Temperature has somewhat of an affect on this value, up to a few µA to a few ten µA when $T_C \cong$ 110°C.

(4) Drain current I_{DSS}

Drain current is the drain-source DC leakage current. Test conditions prescribe V_{DS} and V_{GS} = 0. These values are most susceptible fluctuation caused by temperature changes. As shown in Figure 3, a rise in junction temperature Tj to 100°C makes I_{DSS} a double-digit figure. However, the 25°C I_{DSS} is as illustrated by (B) and (C) when the MOS FET channel current overrides the PN junction leakage current.

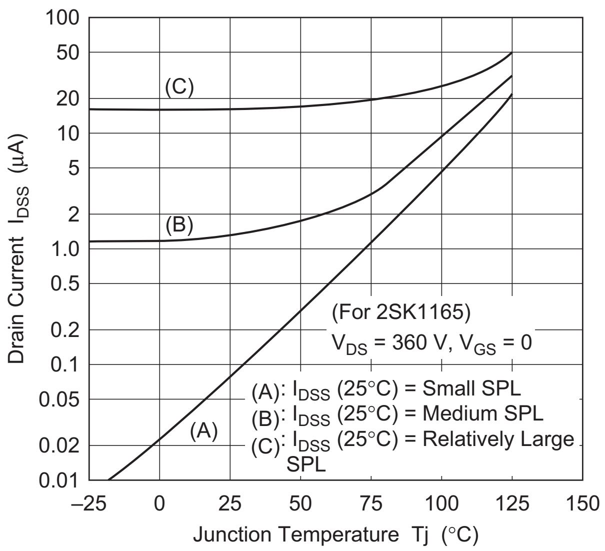


Figure 3 Example of Differences in I_{DSS} for Various Junction Temperatures

(5) Gate-source cutoff voltage $V_{GS(off)}$

The gate threshold voltage at which the Power MOS FET begins to conduct is represented by the symbol $V_{GS(off)}$ or $V_{GS(th)}$. $V_{GS(off)}$ fluctuates with changes in temperature, and carries the negative temperature coefficients shown in Figure 3. Though temperature coefficients differ somewhat according to the model, the range of the fall is –5 to 7 mV / °C. Test conditions prescribe V_{DS} and I_D.

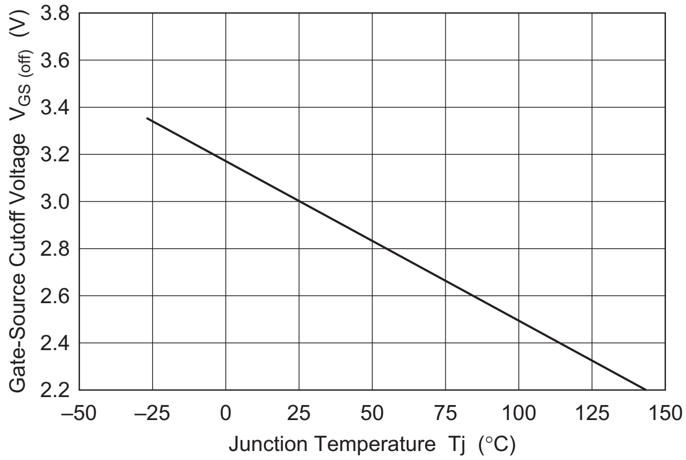


Figure 4 Differences in VGS(off) for Various Junction Temperatures

(6) Drain-source on-resistance $R_{DS(on)}$

On-resistance $R_{DS(on)}$ is one of the most important parameters of the Power MOS FET. Test conditions prescribe I_D, V_{GS}.

$R_{DS(on)}$ fluctuates widely with changes in V_{GS}. This means that at least 10 V must be applied in order to operate the device within the resistance region (resistance loss) with $R_{DS(on)}$ at its minimum. Note, however, that with the DIII-L Series which can be driven by 4 V, the application of 5 V is sufficient to attain the resistance region. Even when V_{GS} is greater than 12 to 15 V, the reduction is $R_{DS(on)}$ is negligible. Making the gate voltage unnecessarily high results in high charging current, an increase in drive loss, and a tendency towards generation of gate-source spike voltage. In addition, turn-off delay time becomes longer (and rise time t_r becomes shorter).

$R_{DS(on)}$ changes along with drain current I_D, and increases above the maximum rated current. $R_{DS(on)}$ also has positive temperature dependency, and the drain current for each set of parameters and temperature characteristics for each model can be found on the data sheet.

(7) Forward transfer admittance $|y_{fs}|$

The Power MOS FET expresses gain similarly to the h_{FE} used by bipolar transistors to express gain. The $|y_{fs}|$ on the data sheet is defined as the rate of change in drain current in relation to changes in gate voltage ($|y_{fs}| = \Delta I_D / \Delta V_{GS}$). $|y_{fs}|$ is an important parameter when a device is operated with in the active region (linear circuit), but it is usually not significant in saturation region operation. Test conditions prescribe V_{DS} ($V_{DS} > I_D \bullet R_{DS(on)}$max), and I_D.

(8) Capacitance Ciss, Coss, Crss

Input capacitance Ciss, output capacitance Coss, and reverse transfer capacitance (Crss) share the following relationships:

Ciss = Cgs + Cgd
Coss = Cds + Cgd
Crss = Cgd

Where:

Cgs = gate-source capacitance
Cds = drain-source capacitance
Cgd = gate-drain capacitance

Cgs and Cgd are generally determined by the chip size and the thickness of the silicon gate oxide film. Cds is P-N connection capacitance, and it is determined by the thickness of the depletion layer spread created when reverse bias is applied to the drain region connection area and the connection. Test conditions prescribe V_{DS}, V_{GS}, and f, and changes in temperature have virtually no affect on capacitance.

Input capacitance Ciss is used in the design of the Power MOS FET driver circuit to calculate the peak rush current required for charging driver loss and input capacitance. Problems can occur, however, if the values noted on the data sheet are used. Refer to 5 Input Dynamic Characteristics for information on such calculations. This section includes information on input dynamic characteristics for each Renesas Power MOS FET model.

(9) Switching time $t_{d(on)}$, t_r, $t_{d(off)}$, t_f

Switching time greatly affects the test circuit's signal source impedance R_S and the drain load resistance R_L. Test conditions prescribe V_{DD}, R_L, V_{GS}, and I_D, as well as the test circuit. The signal source impedance is specified as a 50 Ω pulse generator connection. During actual use, R_S can be reduced for higher speed. The effects of temperature are negligible.

Turn-on delay time $t_{d(on)}$ is the period from 10% of the input gate voltage waveform rise to 10% of the output voltage waveform rise. This period is affected somewhat by the $V_{GS(off)}$ value, getting shorter as $V_{GS(off)}$ becomes smaller.

Rise time t_r is the period from 10% of the output voltage waveform to 90% of the rise. This period is affected by V_{GS} and $V_{GS(off)}$ values, getting shorter as V_{GS} becomes greater or $V_{GS(off)}$ becomes smaller.

Turn-off delay time $t_{d(off)}$ is the period from 90% of the input gate voltage waveform fall to 90% of the output voltage waveform fall. This period is affected by V_{GS} and $V_{GS(off)}$ values, getting shorter as V_{GS} becomes smaller or $V_{GS(off)}$ becomes greater. When the switching operation is accomplished through parallel connection, making $V_{GS(off)}$ values uniform serves to make the current balance of the transition duration uniform.

Fall time t_f is the period from 90% of the output voltage waveform to 10% of the rise. This period tends to be most affected by load resistance R_L, getting longer as R_L becomes greater (light load). This is due to the time constant for drain-source capacitance Cds charging in the off state.

(10) Diode forward voltage V_{DF}

Diode forward voltage is the forward-direction voltage of the equivalent built-in diode between the drain and source. Test conditions prescribe I_F, and $V_{GS} = 0$. When forward bias is applied to the gate, a channel is formed and the diode forward voltage assumes the value of $I_F \times R_{DS(on)}$. Depending on the current region being used, the value for V_F is smaller than that found in standard diodes. Similarly to standard diodes, the temperature characteristic is a negative temperature coefficient (approximately-2.4 mV/°C).

(11) Reverse recovery time t_{rr}

Reverse recovery time t_{rr} is the time it takes for reverse recovery of the equivalent built-in diode between the drain and source. Figure 5 illustrates the reverse recovery time. Test conditions prescribe I_F and di / dt, $V_{GS} = 0$ and the test circuit. In applications such as H bridge circuit output for motor control the built-in diode equivalent to a commutation diode. t_{rr} is high speed, and loss is as low as the i_{rr}. t_{rr} and i_{rr} are affected by di / dt, and the gentler the di / dt slope, the longer i_{rr} is. t_b is the period it takes for the diode withstand voltage to recover from irr, and a smooth di_{rr} / dt characteristic (no detectable vibration waveform when irr recovers to 0) is called a soft waveform which features favorable noise characteristics. The gentler the di / dt slope, the softer the t_b waveform. di / dt characteristics are determined by turn-on time (variable using gate-external resistance), floating inductance of the circuit, and source voltage. The t_{rr} period tends to lengthen as temperature increases.

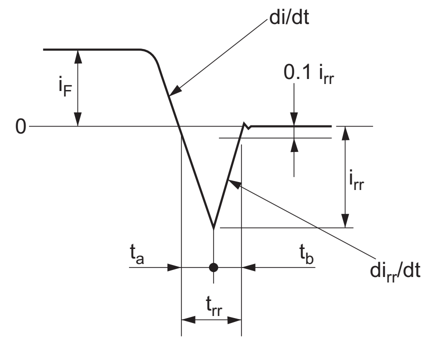


Figure 5 Waveform of Reverse Recovery Time t_{rr}

2. Output Characteristics

Figure 6 shows the output characteristics of the D series 2SK413 and S series 2SK1057 which have the same specification. Whereas in a small signal MOS FET the forward trans-conductance $|y_{fs}|$ is 10 to 20 ms (milli-Siemens) at best, in a power MOS FET it is 1.0 to 15 S. Also, as is obvious from Figure 6, they have what is called pentode characteristics and excellent linearity of $|y_{fs}|$ in relation to I_D.

P channel MOS FETs also have similar characteristics. P channel and N channel types have complementary characteristics.

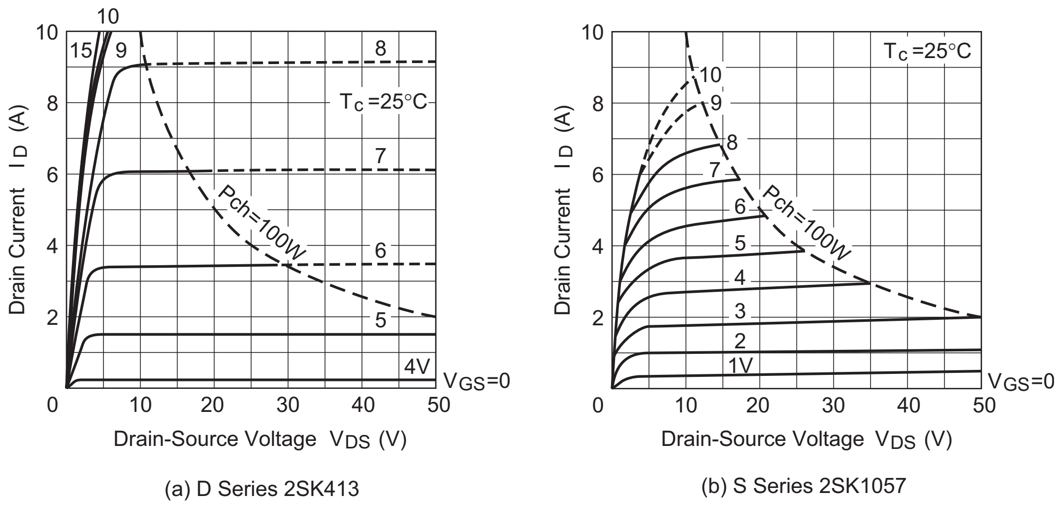


Figure 6 Typical Output Characteristics

3. Frequency Response Characteristics

One of the outstanding features of the power MOS FET is that it has excellent high speed and high frequency characteristics. Therefore, they can be applied in high-speed switching regulators, high-output broadcasting transmitters, etc.

The cut-off frequency of an intrinsic MOS FET is defined by the ratio of the mutual conductance and the input capacitance, and in a typical MOS FET, it will be in the order of GHz. In fact, however, the cut-off frequency is limited by the parasitic resistance and the input capacitance of the gate.

Figure 7, shows the equivalent circuit of MOS FET in the saturation region.

In Figure 7, the cut-off frequency (fc), at which the voltage gain falls to –3 dB of its low frequency value, is given by the following equation.

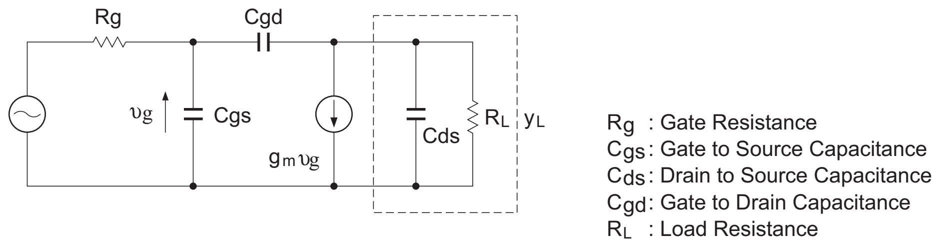


Figure 7 Equivalent Circuit of MOS FET

$$f_c \cong \frac{1}{2\pi} \cdot \frac{1}{Rg\{Cgs + (1 - A_0)Cgd\}} \quad \cdots\cdots (1)$$

Here, A0 is the low-frequency voltage gain, and Rg is the series resistance of the gate. Figure 8 shows the cut-off frequencies of the vertical and the lateral structure devices, found by substituting into equation (1) the parameters (calculated values) of a power MOS FET which has a silicon gate. In the lateral structure, Cgd is much smaller than Cgs, and can be neglected.

In the vertical structure, as explained in paragraph 2, Cgs is a function of the voltage gain (A_0) in the low frequency region, because Cgd is large.

We would like to summarize the above, as follows.

(1) In the case of low voltage gain, the cut-off frequencies of the vertical and the lateral structures show the same level. The input impedance ratio at f_C depends on Rg ratio, so the impedance of the vertical structure is 1.5 to 2 times lower than that of the lateral structure.

(2) In the case of high gain amplifier circuits, the frequency characteristics of the lateral structure and better than that of the vertical structure, because in the vertical structure the feedback capacitance (Cgd) has a great influence.

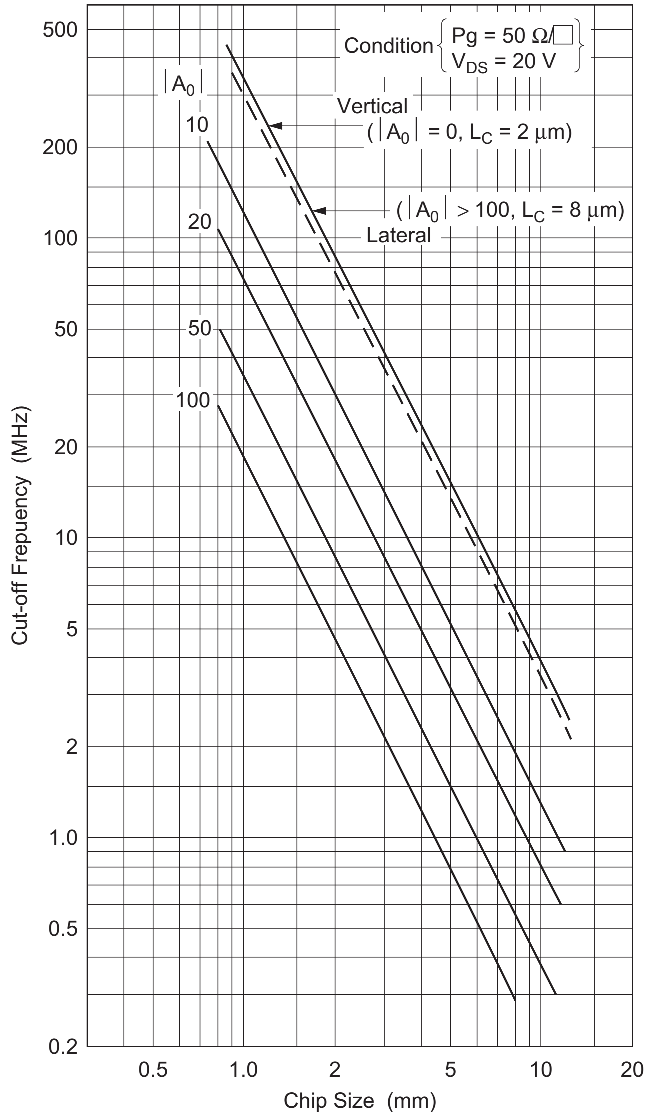


Figure 8 Cut-off Frequency of Silicon Gate Power MOS FETs

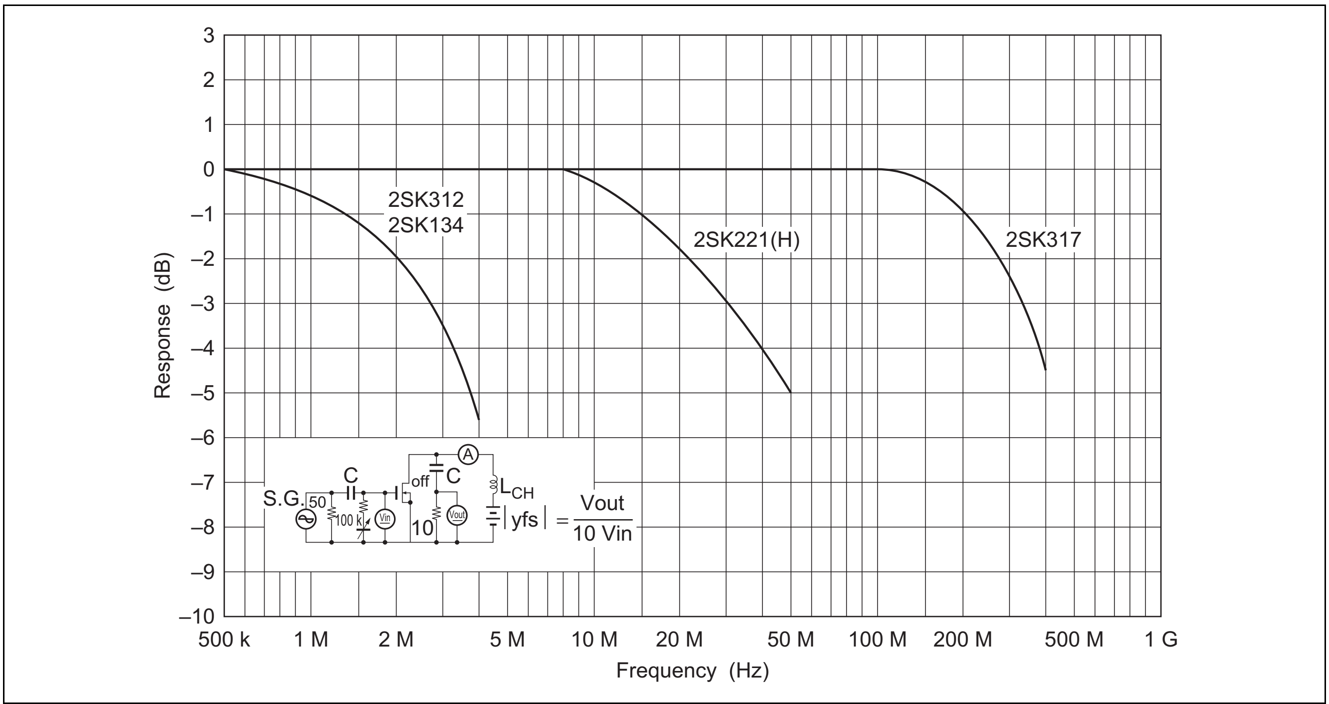


Figure 9 Frequency Response Characteristics of y_{fs} (Source Common)

To further improve the frequency characteristics, the use of low resistance material such as metal is required. This will improve the cut-off frequency by 10 to 100 times. Figure 9 shows the frequency characteristics and the test circuits of typical kinds of MOS FETs. In 2SK317 and 2SK221 (H), the gate material is metal-gate.

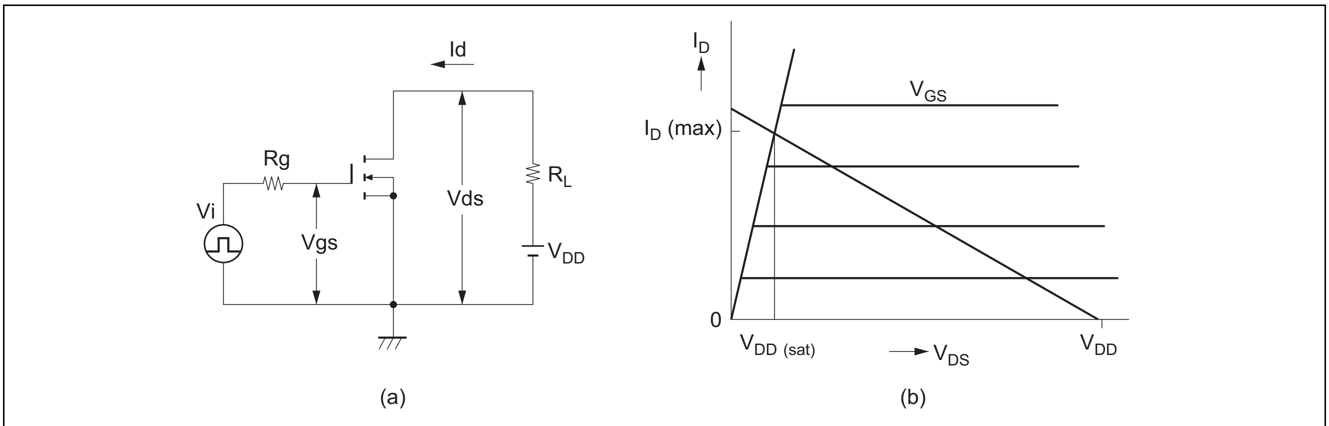


Figure 10 Switching Circuit and Typical Output Characteristics & Load Curve

4. Switching Characteristics

4.1 Switching Characteristics

When using power MOS FETs for power switching, such as in switching regulators, the load of the switching device is usually inductive. Here, however, we would like to assume a resistance load, because it can be treated easily.

Figure 10 shows the resistance load switching circuit (a), simplified current-voltage characteristics, and the load line (b). In this figure, we suppose that the rising curve of current vs. voltage is shown by a straight line, and $g_m = 0$.

Therefore, in Figure 10 (b), the point of the drain voltage = $V_{DS(sat)}$ is included in the non-saturation region, and the region of $V_{DS} > V_{DS(sat)}$ is the saturation region.

In the lateral structure, Cgd is much smaller than Cgs and Cds, so it can be neglected. The time constants are given by the following equations.

$Ti \cong Rg \bullet Cin = Rg \bullet Cgs$ ·· (2)

$To \cong R_L \bullet Cout = Rg \bullet Cds$ ·· (3)

Ti : input time constant

To : output time constant

Then, the switching waveform is shown in Figure 11.

The quantity of charge, Qon, which is stored in the gate and shows how easily the device can be driven, is given by the following equation.

$$Qon = Cgs \cdot V_G \, max \quad \cdots\cdots (4)$$

The transitional charge current (i_{rush}) is given as follows.

$$i_{rush} = \frac{Cgs \cdot V_{Gmax.}}{t_r} \quad \cdots\cdots (5)$$

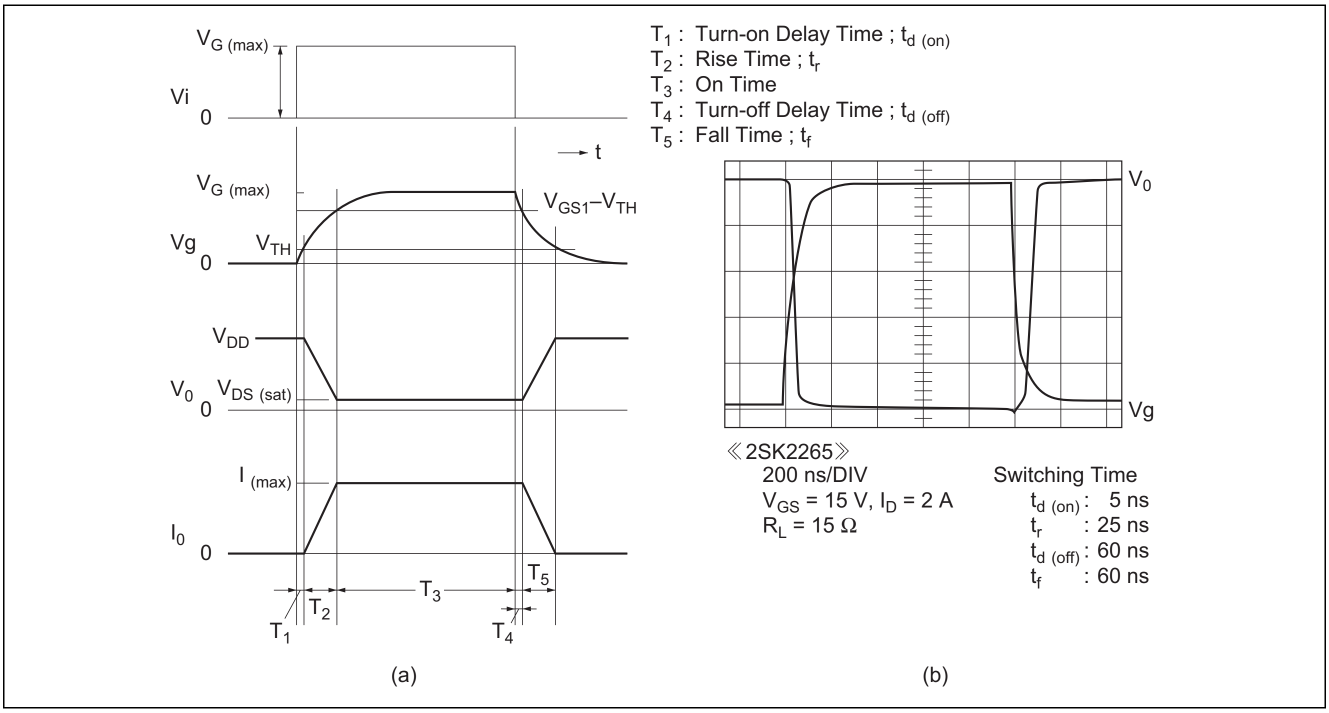


Figure 11 Switching Waveform of Lateral Power MOS FETs

In the vertical structure, the feedback capacitance (Cgd) is large and depends largely on the drain voltage, so the operation analysis will be more complicated. Figure 12 shows the Cgd-drain voltage dependency of the vertical and the lateral structures (2SK1166, 2SK2265) under the conditions of the same chip size and the same 400 V breakdown voltage. With a depletion layer spreading in the drain just under the gate electrode, the value of Cgd will decrease sharply.

Considering the above, we would like to show the Cgd-and gm-drain voltage dependencies in Figure 13 at $V_{GS} > V_{DS}$, Cgd is equal to Cgd_0, the oxide film capacitance just under the drain electrode. When $V_{GS} < V_{DS}$, the depletion layer expands to the drain region, and Cgd << Cgs. The threshold voltage, at which the drain surface is P-inverted, is supposed to be 0. Under these conditions, we would like to look at the switching operations. When the drain voltage is in the region of $V_{DS} > V_{DS(sat)}$, the device is in the saturation region, and in the region of $V_{DS(sat)} < V_{DS} < V_{GS}$, Cgd is equal to Cgd_0. The equivalent circuit is as shown in Figure 13 (c). The time constant of the input capacitance at charging or discharging is given by the following equations.

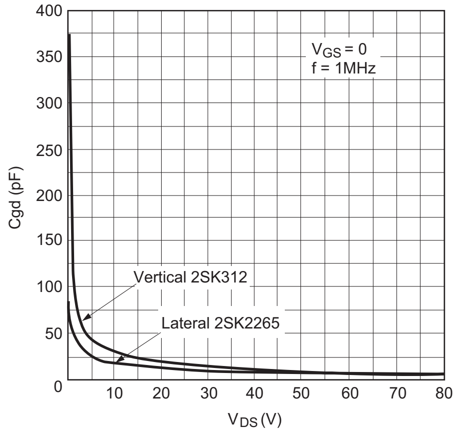


Figure 12 Feedback Capacitance (Cgd)-Drain Voltage Dependency

$$T1 \cong Rg \bullet Cgs\ (V_{DS} > V_{GS})$$
$$T1' \cong Rg\ \{Cgs + (1 + gm \bullet R_L)\}Cgd$$
$$(V_{DS(sat)} < V_{DS} < V_{GS}) \quad \cdots\cdots (6)$$

When $V_{DS} = V_{DS(sat)}$, the device is in the non-saturation region. The equivalent circuit is as shown in Figure 13 (d) and the time constant is given as follows.

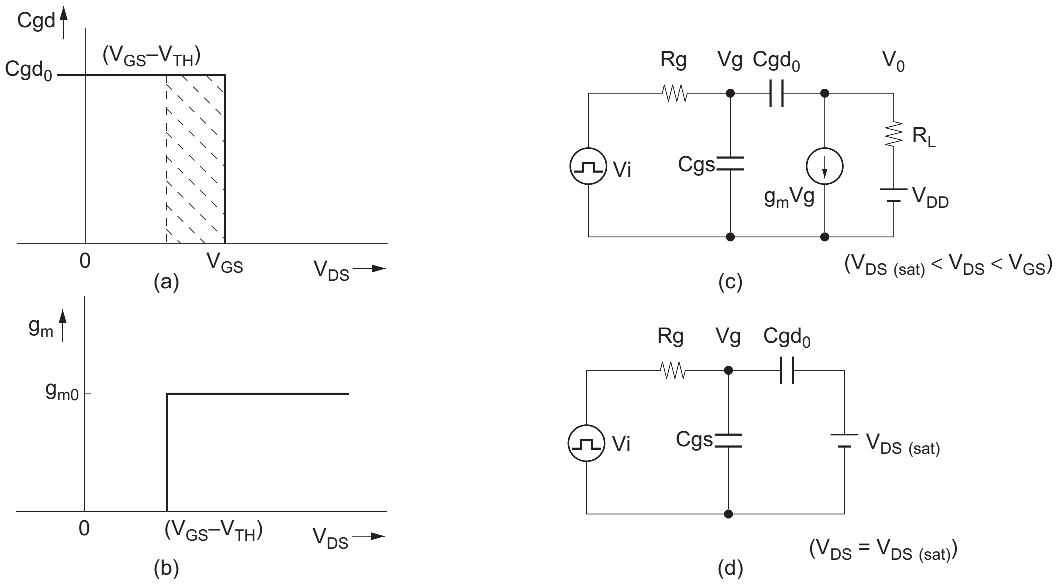


Figure 13 Drain Voltage Dependencies of Cgd and g_m (a), (b), & Equivalent Circuit (c), (d)

$$T2 \cong Rg\ (Cgs + Cgd_0) \quad \cdots\cdots (7)$$

Figure 14 shows the switching waveform as a model, based on the above operations. T_1, T_2, T_4 and T_5 show the turn-on delay time $t_{d(on)}$, the rise time tr, the turn-off delay time $t_{d(off)}$ and the fall time t_f(ton = $t_{d(on)}$ + tr' $t_{(off)} = t_{d(off)} + t_f$) respectively.

T_6 to T_9 show the charging and discharging time of Cgd. T_6 and T_9 indicate the region in which the mirror integration is operated, and it is equal to the time to charge and discharge the changes, whose quantity is equivalent to the shaded part of Figure 13 (a).

Figure 14 (b) shows the gate driving waveform Vg and the output voltage waveform V_0 of the vertical structure, as actually measured. The gate voltage waveform is similar to the basic waveform shown in (a), quantitatively.

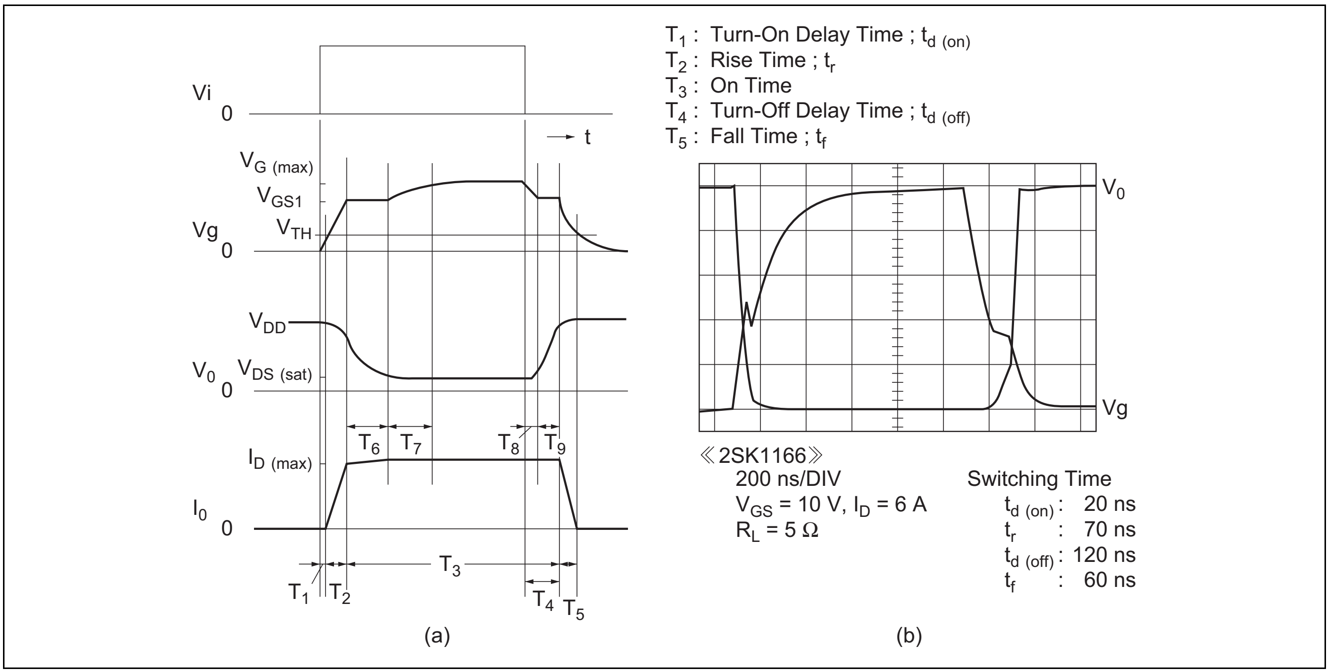


Figure 14 Switching Waveform of Vertical Power MOS FET

This means that we can explain the switching operation using the approximate values of the feedback capacitance and gm shown in Figure 13 (a), and (b). The quantity of stored charges, which shows how easily the gate can be driven, is given by the following equation.

$$\text{Qon} = (\text{Cgs} + \text{Cgd}_0)\, V_G\, \text{max} \quad \cdots\cdots (8)$$

The transitional charge current (i_{rush}) is given as follows.

$$i_{rush} = \frac{(\text{Cgs} + \text{Cgd}_0)V_{\text{Gmax.}}}{t_{on}} \quad \cdots\cdots (9)$$

The following summarizes a comparison of the switching operations of the vertical and the lateral structures.

(1) The gate driving power required is determined by the ratio of the quantity of stored charges in gate capacitance. The driving power for the vertical structure device is larger than that for the lateral structure device by $(\text{Cgs} + \text{Cgd}_0)$ D / (Cgs)S.

(2) When the device is driven by a high speed pulse, the rise time (t_r) and the fall time (t_f), for both structures, are given by the following equations.

$$t_r \cong \text{Cin} \cdot \text{Rg} \cdot ln\left(\frac{V_{\text{Gmax.}} - \text{Vth}}{V_{\text{GSmax.}} - V_{\text{GS1}}}\right) \quad \cdots\cdots (10)$$

$$t_r \cong \text{Cin} \cdot \text{Rg} \cdot ln\left(\frac{V_{\text{GS1}}}{\text{Vth}}\right) \quad \cdots\cdots (11)$$

Here V_{GS1} is the gate voltage for saturation.

In the vertical structure, tr and tf are faster than those of the lateral one, because of the small value of the gate resistance. The turn-off delay time, however, is larger, so the value of t_{off} ($=t_{d(off)} + t_f$) will be larger.

In an actual circuit, the output resistance (R) of the driven circuit will be added to this gate resistance (Rg).

Therefore, in high speed operation, the vertical structure device should be designed so that the output resistance of the drive circuit will be as small as possible, by adding one or two emitter follower circuits to the driver.

Figure 15 and Figure 16 show the turn off time of the device with the drive circuit added and that of the standard measuring circuit. Moreover, as shown in circuit (c), the operation speed will be further improved by making the gate potential negative at cut off time.

In power MOS FETs, in contrast with bipolar transistors, the switching time is not influenced by temperature, and the circuit design will be easier. Figure 17 shows the relation of the switching time vs. temperature characteristics, compared to that of bipolar transistors.

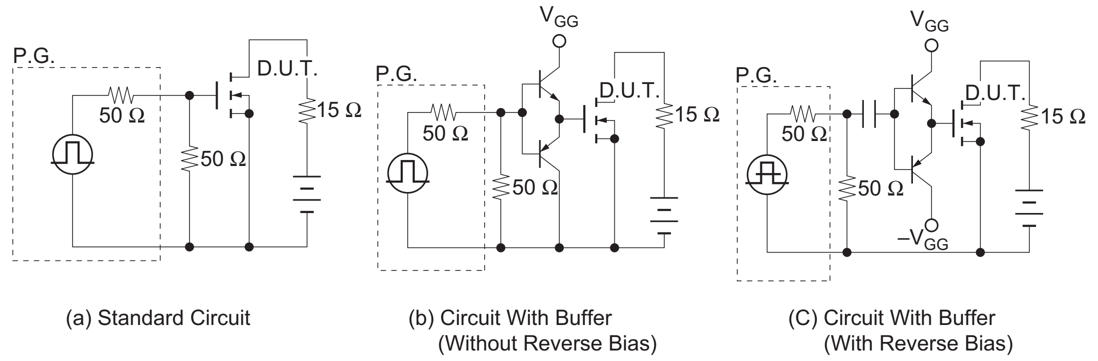


Figure 15 Drive Circuit

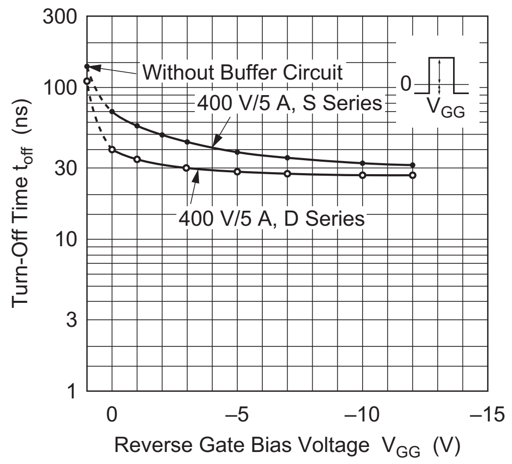


Figure 16 Turn-Off Time vs. Reverse Gate Bias

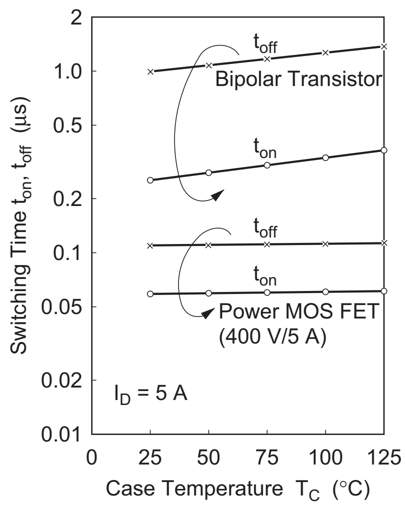


Figure 17 Switching Time vs. Case Temperature

4.2 Method for Calculating Power MOS FET Switching Loss

This section explain how to calculate Power MOS FET switching loss in the case of the approximation waveform illustrated in Figure 18.

Loss for periods t_1, t_2, and t_3 are respectively represented by P_1, P_2, and P_3 as noted below. P_1 is turn on loss, and P_3 is turn off loss.

The following method for calculating P_1 and P_2 is provided as reference.

$$P_1 = \frac{1}{6} \cdot f \cdot t_1 (V_D \cdot I_b + 2I_b{}^2 \cdot Ron) \quad \cdots\cdots (1)$$

$$P_2 = \frac{1}{3} \cdot f \cdot t_2 \cdot Ron(I_p{}^2 + I_p \cdot I_b + I_b{}^2) \quad \cdots\cdots (2)$$

$$P_3 = \frac{1}{6} \cdot f \cdot t_3 (V_P \cdot I_p + 2I_p{}^2 \cdot Ron) \quad \cdots\cdots (3)$$

(1) When loss P_1 for period t is repeated for period T

$$\begin{aligned}
P_1 &= \frac{1}{T}\int_0^{t_1} (i(t) \cdot \vartheta ds(t))dt \\
&= \frac{1}{T}\int_0^{t_1} \frac{Ib}{t_1} t\left(-\frac{V_D - Ib \cdot Ron}{t_1} t + V_D\right)dt \\
&= \frac{1}{T}\int_0^{t_1} \left(-\frac{Ib \cdot Vb}{t_1{}^2} t^2 + \frac{Ib^2 \cdot Ron}{t_1{}^2} t^2 + \frac{Ib \cdot V_D}{t_1} t\right)dt \\
&= \frac{1}{T}\left[-\frac{Ib \cdot V_D}{t_1{}^2} \cdot \frac{t^3}{3} + \frac{Ib^2 \cdot Ron}{t_1{}^2} \cdot \frac{t^3}{3} + \frac{Ib \cdot V_D}{t_1} \cdot \frac{t^2}{2}\right]_0^{t_1}
\end{aligned}$$

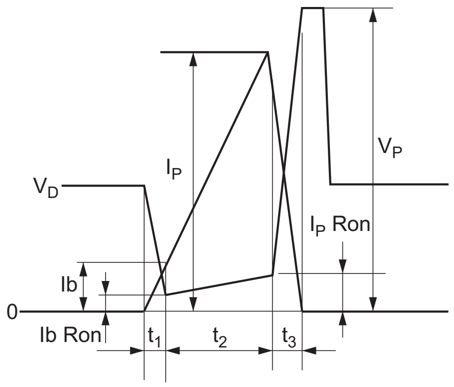


Figure 18 Voltage and Current Approximation Waveform

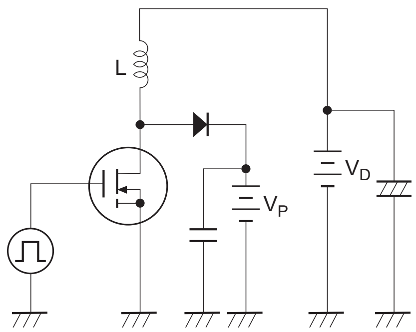


Figure 19 L Load Switching Circuit

$$P_1 = \frac{1}{T}\left(-\frac{Ib \cdot V_D}{t_1^2} \cdot \frac{t_1^3}{3} + \frac{Ib^2 \cdot Ron}{t_1^2} \cdot \frac{t_1^3}{3} + \frac{Ib \cdot V_D}{t_1} \cdot \frac{t_1^2}{2}\right)$$

$$= \frac{1}{T}\left(-\frac{1}{3} \cdot V_D \cdot Ib \cdot t_1 + \frac{1}{3} Ib^2 \cdot Ron \cdot t_1 + \frac{1}{2} V_D \cdot Ib \cdot t_1\right)$$

$$= \frac{1}{T}\left(\frac{1}{6} V_D \cdot Ib \cdot t_1 + \frac{1}{3} Ib^2 \cdot Ron \cdot t_1\right)$$

$$= \frac{1}{6T}\left(V_D \cdot Ib + 2Ib^2 \cdot Ron\right) t_1$$

$$\frac{1}{T} = f$$

$$\therefore P_1 = \frac{1}{6} \cdot f \cdot t_1 \left(V_D \cdot Ib + 2Ib^2 \cdot Ron\right)$$

(2) Loss P_2 for Period t_2

$$P_2 = \frac{1}{T}\int_0^{t_2} \left\{\left(\frac{Ip - Ib}{t_2} t + Ib\right)\left(\frac{Ib - Ib}{t_2} Ron \cdot t + Ib \cdot Ron\right)\right\} dt$$

$$\frac{Ip - Ib}{t_2} = a$$

$$P_2 = \int_0^{t_2} (a\, t + Ib)(a \cdot Ron \cdot t + Ib \cdot Ron)\, dt$$

$$P_2 = \frac{1}{T}\int_0^{t_2} (a^2 \cdot Ron \cdot t^2 + 2a \cdot Ib \cdot Ron \cdot t + Ib^2 \cdot Ron) dt$$

$$= \frac{1}{T}\left[a^2\, Ron \cdot \frac{t^3}{3} + 2a \cdot Ib \cdot Ron \frac{t^2}{2} + Ib^2 \cdot Ron \cdot t\right]_0^{t_2}$$

$$= \frac{1}{T}\left\{\frac{(Ip - Ib)^2}{t_2^2} \cdot Ron \cdot \frac{t_2^3}{3} + 2\frac{Ip - Ib}{t_2} \cdot Ib \cdot Ron \cdot \frac{t_2^3}{2} + Ib^2 \cdot Ron \cdot t_2\right\}$$

$$= \frac{1}{T}\left\{\frac{1}{3} t_2 (Ip - Ib)^2 Ron + (Ip - Ib) Ib \cdot Ron \cdot t_2 + Ib^2 \cdot Ron \cdot t_2\right\}$$

$$= \frac{1}{T}\left\{\frac{1}{3} Ip^2 \cdot Ron \cdot t_2 - \frac{2}{3} Ip \cdot Ib \cdot Ron \cdot t_2 + \frac{1}{3} Ib^2 \cdot Ron \cdot t_2 \right.$$
$$\left. + Ip \cdot Ib \cdot Ron \cdot t_2 - Ib^2 \cdot Ron \cdot t_2 + Ib^2 \cdot Ron \cdot t_2\right\}$$

$$= \frac{1}{3T} \cdot Ron \cdot t_2 (Ip^2 + IpIb + Ib^2)$$

$$\frac{1}{T} = f$$

$$\therefore P_2 = \frac{1}{3} \cdot f \cdot Ron \cdot t_2 (Ip^2 + Ip \cdot Ib + Ib^2)$$

5. Input Dynamic Characteristics

Generally, when calculating the peak-rush current necessary for charging drive loss and gate input capacity in designing the power MOS FET drive circuit, evaluate from the following equations.

Drive loss $Pd = f \bullet Cin \cdot V_{GS}$ .... (12)

Peak rush current $i_{(rush)}$ $i_{(rush)} = \dfrac{Cin \cdot V_{GS}}{t}$ .... (13)

Where, input capacity Cin is generally the value when the bias is fixed in the data sheet. If using this value as it is, some problems occur. This is because in the Cin, gate drain capacity Cgd, which is mirror capacity, exists, and is function of the drain-source voltage V_{DS}.

Also, since the gate-source capacity, Cgs is a function of V_{GS}, it contains complicated elements. These details are described in 4 Switching Characteristics. It is very complicated to design the drive circuit. As a function of V_{GS} and V_{DS}, gate charge load Qg should be regulated.

(1) Gate charge factor

Figure 20 shows the measurement circuit of the gate charge load, Qg. This measuring theory is that when driving the gate with constant current, Ig, the time axis, t is multiplied by Ig and the time axis reads as the load, Qg.

Figure 21 shows Qg – V_{GS}, V_{DS} characteristics at Turn-on and Turn-off measured in 2SK299. The vertical axis represents the drain-source voltage V_{DS}, and the gate-source voltage V_{GS}. The horizontal axis represents the gate charge load Qg. In waveforms (a) and (b), the stage rised from zero shows the gate-source capacity Cgs charging time, and the next flat stage shows the gate-drain capacity Cgd charging time. To the contrary, waveforms (c) and (d) shows the discharging time. The loads necessary for charging Cgs and Cgd are different from each other.

Figure 22 shows Qg – V_{GS} characteristics when $V_{DD} \cdot I_D$ of 2SK299 is a parameter. In Figure 22(b) waveform, the charge necessary for flowing V_{DD} = 100 V and I_D = 1 A is 16 nC. At this time, necessary is about 5.2 V. (This value changes by Vth, g_m).

However, in the actual switching operation, it is generally used in the following conditions that drain-source voltage is in "ON" (saturation) state, and a margin is added to reduce the ON resistance, and the overdrive when V_{GS} = 10 to 15 V. Therefore, when designing the drive voltage as I_D = 1 A, V_{GS} = 10 V, the gate charge load is 28 nC. Qg is different between V_{DD} = 100 V and V_{DD} = 200 V because Cgd varies with V_{DS}.

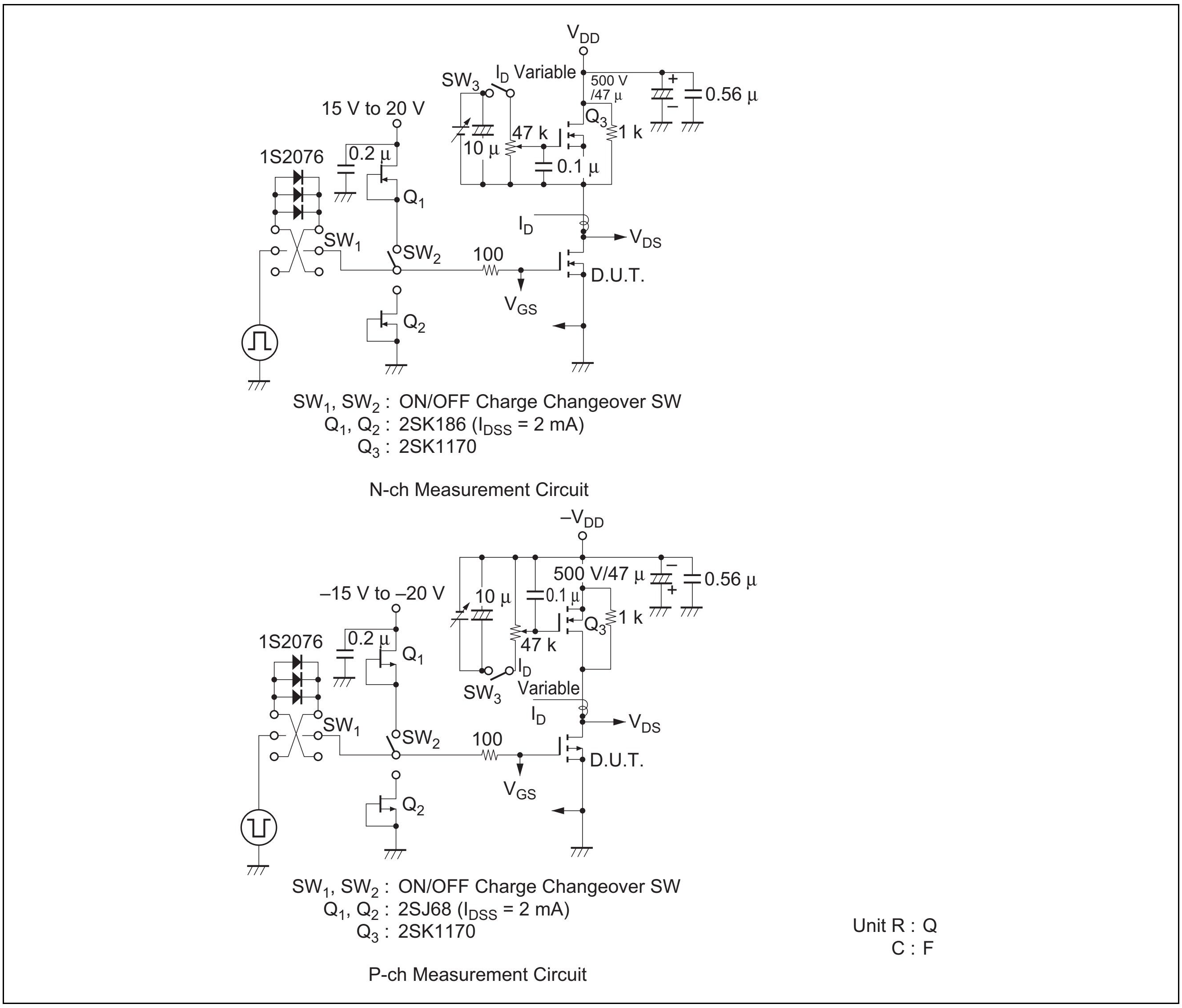


Figure 20 Gate Charge Measurement Circuit

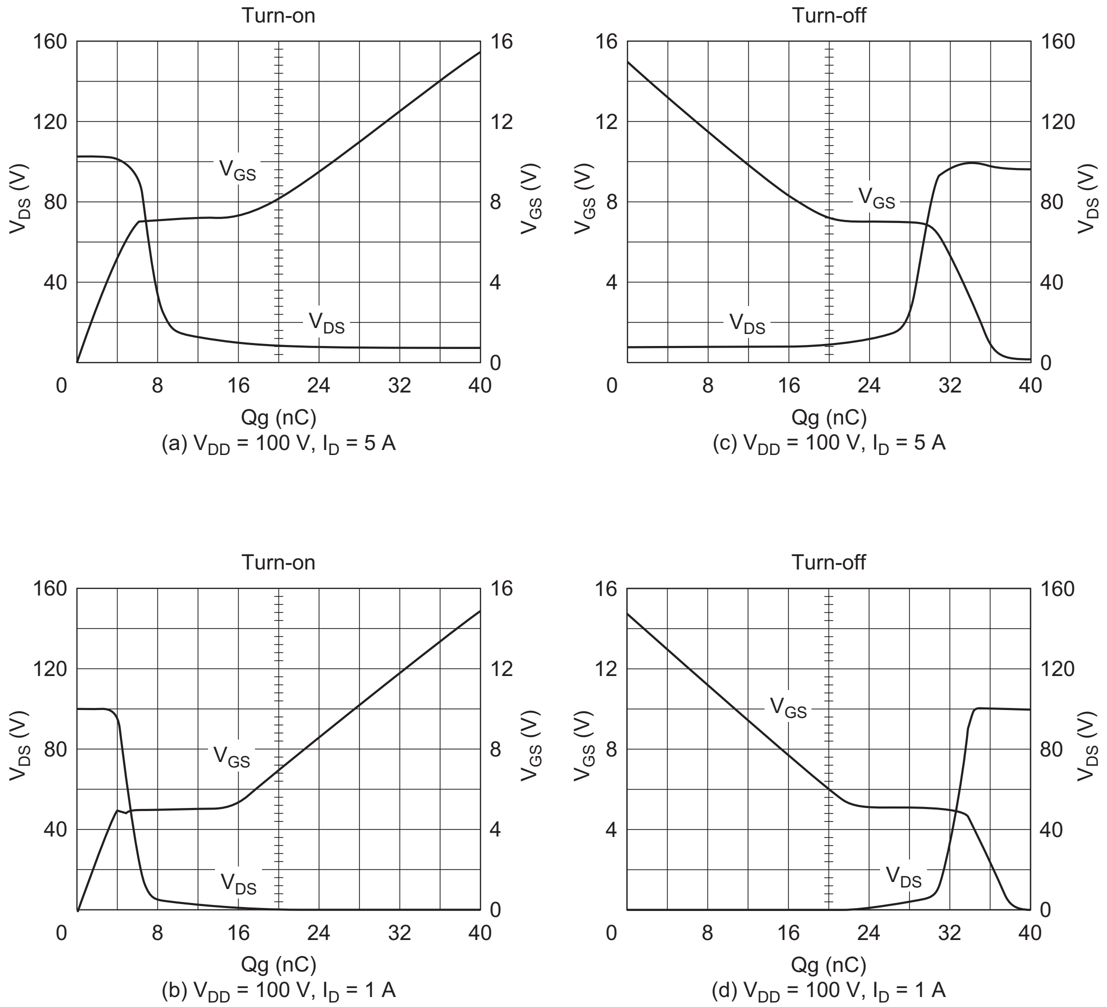


Figure 21 2SK299 Qg – V_{GS} • V_{DS} Characteristics

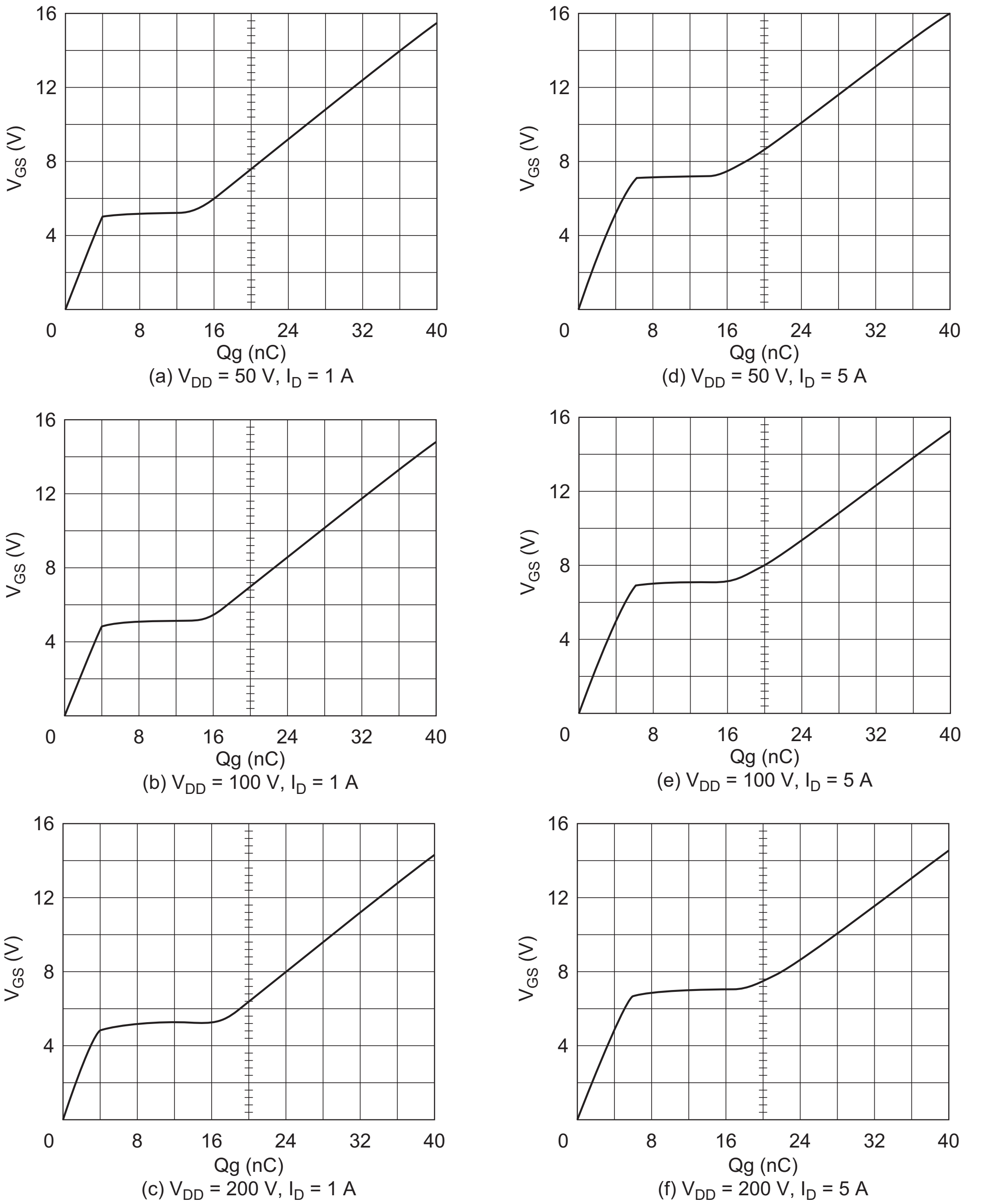


Figure 22 2SK299 Qg – V_{GS} Characteristics

(2) Designing of driven circuit

The drive loss and necessary peak rush current of the drive circuit are evaluated by the following equations with the gate charge load Qg.

Drive loss $P_D = f \bullet Qg\, V_{GS}$ .... (14)

Peak rush current $i_{(rush)} = \frac{Q}{t}$ .... (15)

<Example>

Using the 2SK299, when f = 100 kHz, V_{DD} = 100 V, V_{GS} = 15 V, switching time ton = 50 ns, and I_D = 5 A, what is the drive loss and necessary peak rush current?

<Solution>

Since Qg in the above conditions is 39 nC in Figure 22 (e).

$$\begin{aligned} Pd &= f \cdot Qg \cdot V_{GS} \\ &= 100 \times 10^{3} \times 39 \times 10^{-9} \times 15 \\ &= 58.5\text{mW} \end{aligned}$$

$$i_{(rush)} = \frac{Qg}{t} = \frac{39 \times 10^{-9}}{50 \times 10^{-9}} = 0.78\text{A}$$

As shown above, the answer can be obtained with ease.

Figure 23 shows the comparison between the drive loss measured by the Figure 24 Circuit and the drive loss calculated using the equation (14). The horizontal axis represents frequency. As shown in this figure, calculated value and measured value match well, which indicates that determining the gate charge Qg facilitates designing the drive circuit accurately.

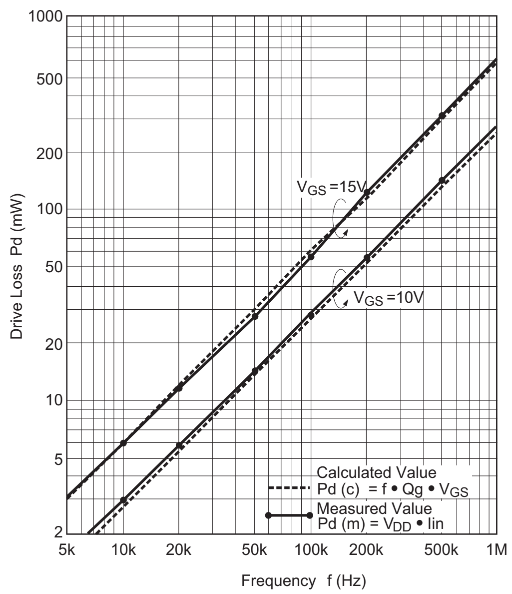


Figure 23 Drive loss of Power MOS FET (2SK320)

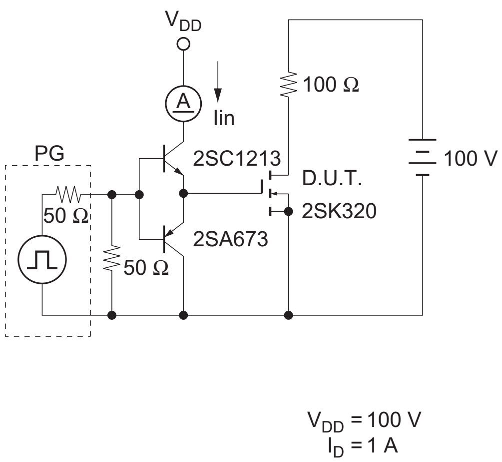


Figure 24 Test Circuit

(3) Gate Charge Characteristics

Figure 25 shows typical gate charge characteristics and the waveforms of V_{GS}, V_{DS} and I_D. The characteristic curve can be divided into three areas. Area 1 indicates a period in which the gate source capacity (Cgs) is charged until the V_{GS} reaches the value required to supply specific drain current I_D. The FET is "off" between the threshold voltage $V_{GS(th)}$ and t1 during this period.

When the V_{GS} value exceeds $V_{GS(th)}$, the drain current I_D begins to flow and becomes stable at t_2. Area 2 is a transition area between the V_{DS} active and inactive areas. That is, the drain source pressure V_{DS} varies and the gate drain (mirror) capacity Cgd is charged. This mirror effect increases Cin, activates the FET, the V_{DS} transition lessens, and as a result, the effect is lost at t_3. In area 3, the V_{DS} is inactive and doesn't very much. That is, the $V_{DS(on)}$ of the FET is maintained as $I_D \times R_{DS(on)}$. Cin(3) in area 3 is larger than Cin(1), but smaller than Cin(2). Cin(1) and Cin(3) correspond to Ciss and are equivalent to the value of Cgs + Cgd. However, Ciss and Cgs + Cgd are not equal because the value of V_{DS} defers between areas 1 and 3 (the Cgd value differs). That is, Cin(3) of area 3 is larger than Cin(1) because of the large Cgd caused by the thin depletion layer immediately under the gate.

(4) Calculating Method of Switching Time

Using the Gate Charged Characteristic Qg Figure 26 (c) shows a standard circuit which measures switching time, and Figure 26 (a) shows the transient response characteristic of gate input pressure. In the figure (a), when Cin is fixed, the V_{GS} characteristic is;

$$V_{GS(t)} = V_{GS}\left\{1-\exp\left(-\frac{t}{Cin \cdot R_S}\right)\right\} \quad \cdots\cdots (16)$$

Vg_1 and Vg_2 are;

$$Vg1 = V_{GG}\left\{1-\exp\left(-\frac{t_1}{Cin \cdot R_S}\right)\right\} \quad \cdots\cdots (17)$$

$$Vg2 = V_{GG}\left\{1-\exp\left(-\frac{t_2}{Cin \cdot R_S}\right)\right\} \quad \cdots\cdots (18)$$

t_1 and $t_2 - t_1$ can be got from formulas (17) and (18). They are as follows because Cin differs between area 1 and 2 as seen from Figure 27.

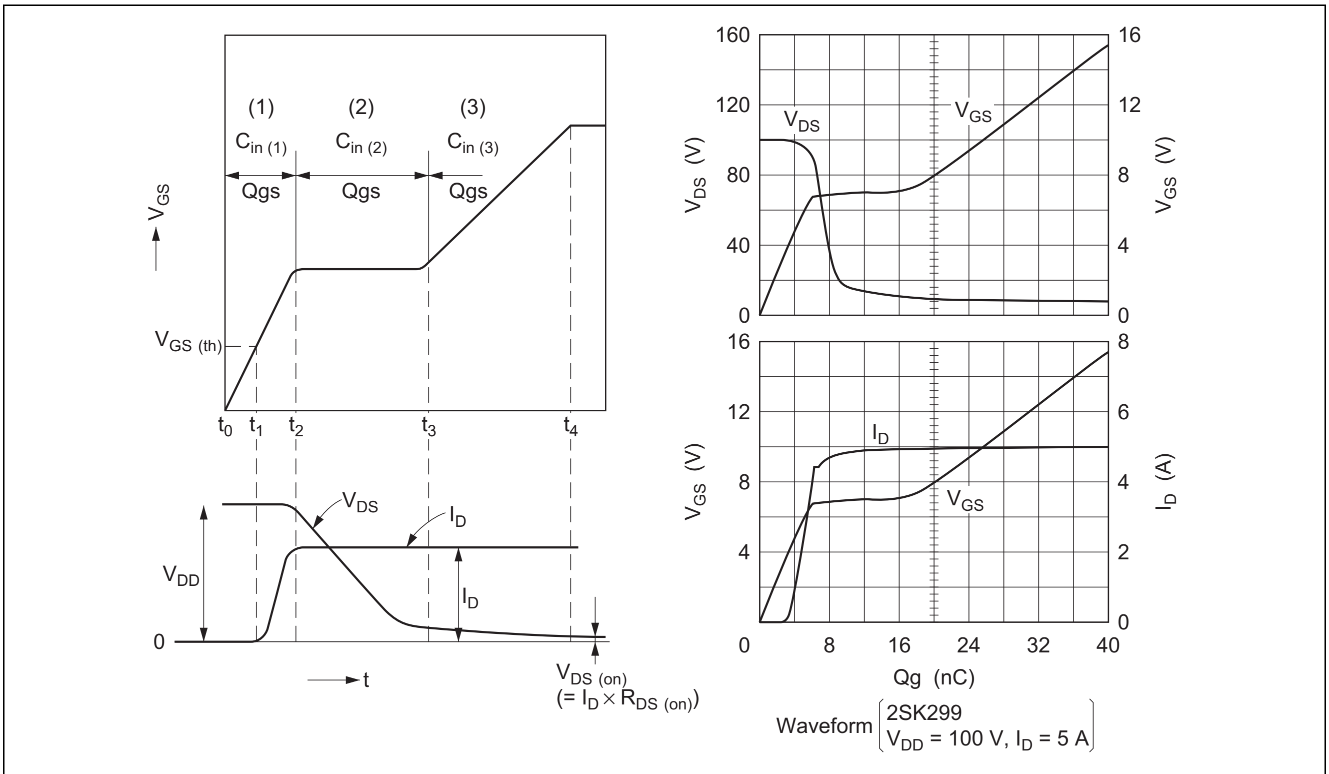


Figure 25 Typical Gate Charge Waveform and VDS, ID Waveforms

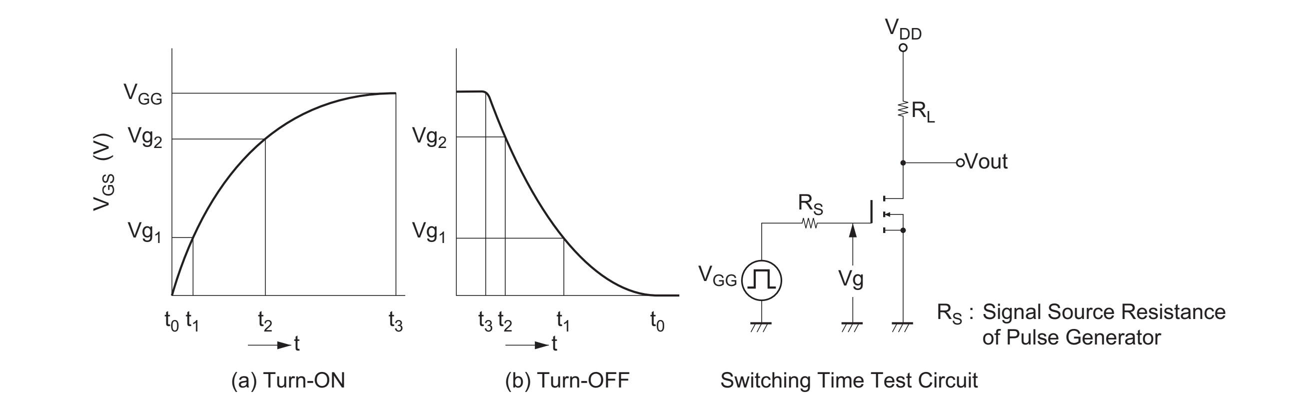


Figure 26 Switching Time Test Circuit and VGS Waveforms

$$t_1 = (Cin_{(1)} \cdot R_S) ln\left(\frac{V_{GG}}{V_{GG} - Vg1}\right) \quad (19)$$

$$t_2 - t_1 = (Cin_{(2)} \cdot R_S) ln\left(\frac{V_{GG} - Vg1}{V_{GG} - Vg2}\right) \quad (20)$$

Cin(1) and Cin(2) of area 1 and area 2 are obtained with following formulas.

$$Cin_{(1)} = \frac{\Delta Q}{\Delta Vg} = \frac{Qg1}{Vg1} \quad (21)$$

$$Cin_{(2)} = \frac{\Delta Q}{\Delta Vg} = \frac{Qg2 - Qg1}{Vg2 - Vg1} \quad (22)$$

In the Figure 27 waveforms, t1 is the turn-on delay time td(on), and $t_2 - t_1$ is the rise time tr. If substituting formulas (21) and (22) for formulas (19) and (20), td(on) and tr are;

$$\therefore t_{d(on)} = \frac{Qg1}{Vg1} \cdot R_S ln\left(\frac{V_{GG}}{V_{GG} - Vg1}\right) \quad (23)$$

$$\therefore t_r = \left(\frac{Qg2 - Qg1}{Vg2 - Vg1}\right) \cdot R_S ln\left(\frac{V_{GG} - Vg1}{V_{GG} - Vg2}\right) \quad (24)$$

The turn-off delay time $t_{d(off)}$ and fall time tf can be also obtained using the above method. With Figure 26 (b);

$$V_{GS(1)} = V_{GG} \cdot \exp\left(-\frac{t}{Cin \cdot R_S}\right) \quad (25)$$

t_2 and $t_1 - t_2$ are;

$$t_2 = (Cin_{(1)} \cdot R_S) ln \frac{V_{GG}}{Vg2} \quad (26)$$

$$t_1 - t_2 = (Cin_{(2)} \cdot R_S) ln \frac{Vg2}{Vg1} \quad (27)$$

With Figure 28 Cin(1) and Cin(2) are;

$$Cin_{(1)} = \frac{\Delta Q}{\Delta Vg} = \frac{Qg3 - Qg2}{V_{GG} - Vg2} \quad (28)$$

$$Cin_{(2)} = \frac{\Delta Q}{\Delta Vg} = \frac{Qg2 - Qg1}{Vg2 - Vg1} \quad (29)$$

In the Figure 28 waveforms, t_2 is the turn-off delay time $t_{d(off)}$, and $t_1 - t_2$ is the fall time t_f.

$$\therefore t_{d(off)} = \left(\frac{Qg3 - Qg2}{V_{GG} - Vg2}\right) \cdot R_S l_n \left(\frac{V_{GG}}{Vg2}\right) \quad \cdots\cdots (30)$$

$$\therefore t_f = \left(\frac{Qg2 - Qg1}{Vg2 - Vg1}\right) \cdot R_S l_n \left(\frac{Vg2}{Vg1}\right) \quad \cdots\cdots (31)$$

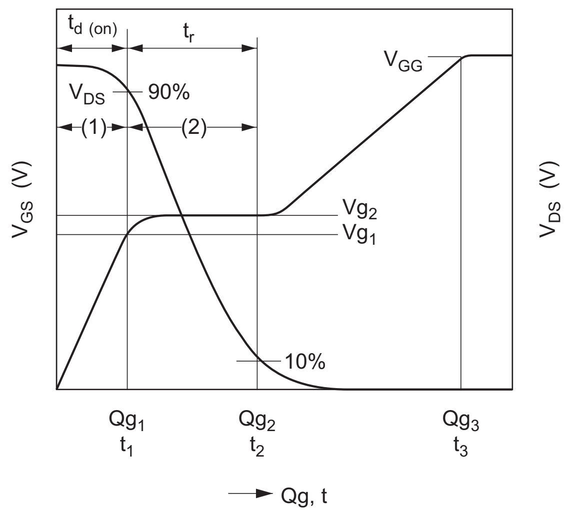


Figure 27 Gate Charge Characteristic (Turn-on)

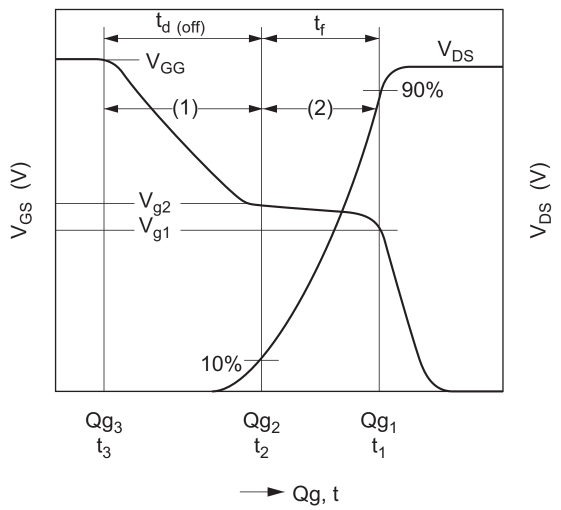


Figure 28 Gate Charge Characteristic (Turn-off)

6. Area of Safe Operation (ASO)

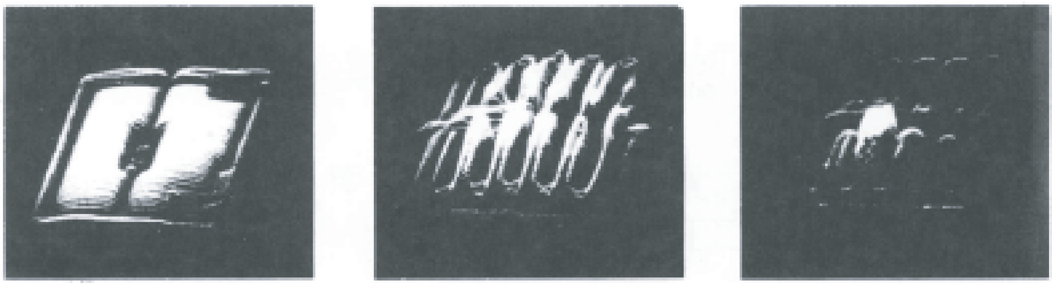
6.1 Forward Bias ASO

The most basic and important characteristic required for a power device is a high breakdown strength.

Since the current flowing in power MOS FETs does not concentrate locally, power MOS FETs are free from secondary breakdown in the high voltage region.

Figure 29 shows thermal mapping of chip surfaces, under power on, for a power MOS FET and conventional bipolar transistor.

Whereas the thermal mapping in the power MOS FET is uniform, a hot spot is generated in the bipolar transistor, although the power applied is one-half that applied to the power MOS FET. Figure 30 shows breakdown points of power MOS FETs in relation to those of bipolar transistors. ASO of bipolar transistors is limited by secondary breakdown in the high voltage region. On the other hand, in a power MOS FET, the guaranteed area of safe operation is equal to the range of thermal limitation. ASO design is very simple.



V_{DS} = 60 V, I_D = 2 A

(A) Power MOS FET (2SK135, 2SK1058)

V_{CE} = 30 V, I_C = 4 A

(B) Bipolar Transistor (2SC1343)

V_{CE} = 60 V, I_C = 1 A

(C) Generation of Hot Spot Bipolar Transistor (2Sc1343)

Figure 29 Chip Surface Temperature at Power ON

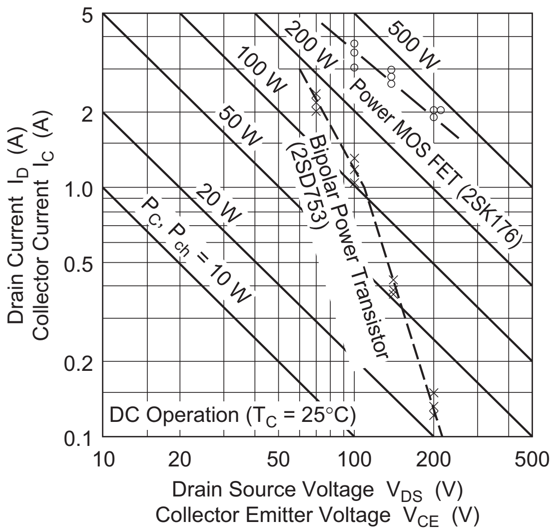


Figure 30 Area of Safe Operation

Determining Whether Power MOS FET Repeat Pulse Switching Operations Fall Within the ASO (Reference)

In order to determine whether or not Power MOS FET continuous pulse switching operations fall within the ASO, first calculate junction temperature Tj. If the calculated value falls within the prescribed Tj max., the operation is within the ASO. The following shows an example of such a calculation.

Example 1: For a repeat pulse switching operation with constant power loss

Junction temperature Tj is expressed by the following formula:

$$Tj = Tc + \Delta Tj$$
$$= Tc + \theta ch\text{–}c(t)\ (I_D{}^2 \bullet Ron + SW\ loss)$$

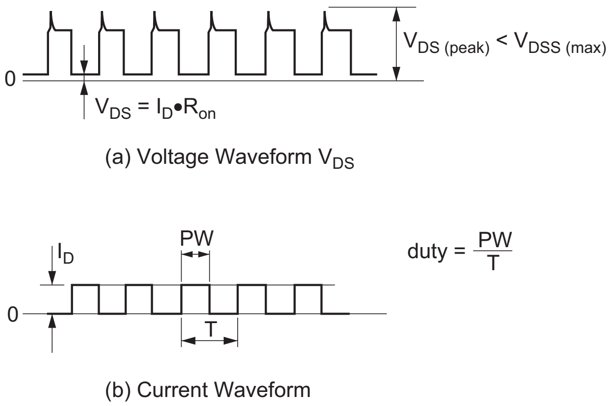


Figure 31 Waveforms for Repeat Pulse Switching Operation with Constant Power Loss

when:

Tc: case temperature
θch–c(t): PW = t, duty n% transient thermal resistance
Ron: on-resistance max (Tj max = 150°C)
SW loss: loss caused by t_{on}, t_{off} during switching

Example:

When using 2SK556 (Pch = 100 W, θch-c = 1.25°C / W, Tj max = 150°C), are the switching (Power MOS FET $V_{GS} \geq$ 10 V) conditions within the ASO when case temperature T_C = 80°C, I_D = 10 A, PW = 10 µs, and duty = 20% (f = 50 kHz)? Here, note that SW loss is half of Ron loss.

(1) First, the transient thermal resistance θch-c(t) for PW = 10µs and duty = 20% is calculated using $\gamma_{(t)}$ = 0.21 from the data sheet, giving us θch-$c_{(t)}$ = γs(t) • θch-c = 0.21 × 1.25 = 0.263°C / W.
Next, chi-c(t) for PW = t and duty = n% can be calculated using the following formula:

$$\theta ch - c(t) = \theta ch - c\left\{\frac{n}{100} + \left(1 - \frac{n}{100}\right)^{*} \gamma_{S(t)}\right\}$$

(*$\gamma_{s(t)}$ is 1 shot pulse for rated transient thermal resistance.)

(2) The data sheet reveals that Ron max for 2SK556 is 0.55Ω. For a Tj max of 150°C, this value should be increased 2.2 to 2.4 times:

Ron = 2.4 × 0.55 = 1.32 Ω

(3) Consequently, junction temperature Tj is:

$$\begin{aligned} Tj &= Tc + \theta ch - c(t)(I_D{}^2 \cdot Ron + SW\ loss) \\ &= 80 + 0.263\left\{\left(10^2 \times 132\right) + \frac{1}{2}\left(10^2 \times 1.32\right)\right\} \\ &= 80 + 52 \\ &= 132°C \end{aligned}$$

Since Tj < Tj max, the operating conditions fall within the ASO.

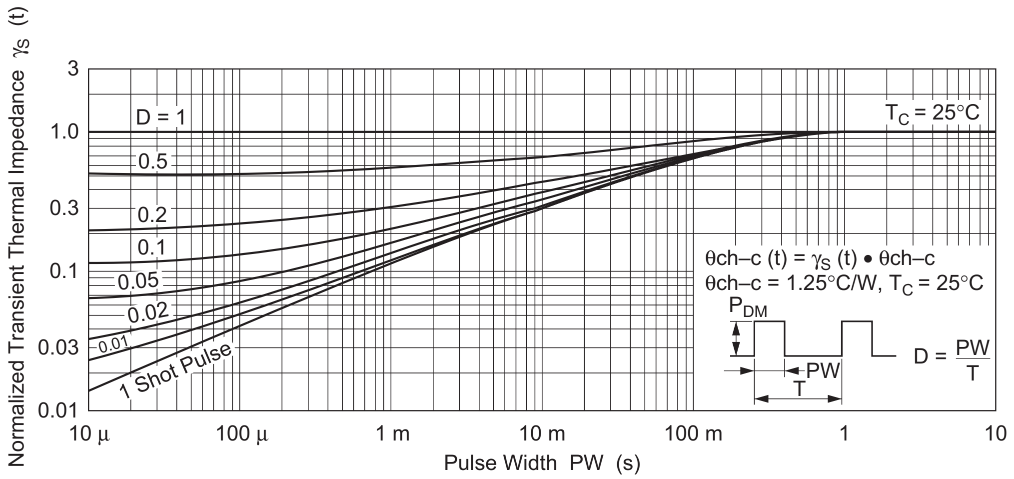


Figure 32 2SK556 Catalog Data

Example 2: For a repeat pulse switching operation with non-constant power loss (i.e. fluctuating load, short, etc.)

Figure 33 (b) shows a method that can be effectively used for calculating an approximation (to simplify strict conditions) for the type of waveform shown in Figure 33 (a). Figure 33 (c) shows junction temperature Tj(peak) when loss P1 under continuous repeat operation conditions average loss P2, and peak period (I_{D2}) loss P_3 are applied. Tj(peak) can be calculated using the following formula:

$$\begin{aligned}
\mathrm{Tj(peak)} &\cong \mathrm{Tc} + P_1 \cdot \theta\mathrm{ch-c}(t_1) + P_2 \cdot \theta\mathrm{ch-c}(t_2 + t_3) \\
&\quad + P_3 \cdot \theta\mathrm{ch-c}(t_3) - P_1 \cdot \theta\mathrm{ch-c}(t_2 + t_3) - P_2 \cdot \theta\mathrm{ch-c}(t_3) \\
&= \mathrm{Tc} + \theta\mathrm{ch-c}(t_1)(I_{D1}{}^2 \cdot \mathrm{Ron1} + \mathrm{SW\ loss}) \\
&\quad + \frac{t_1}{T} \cdot I_{D2}{}^2 \cdot \mathrm{Ron2} \cdot \theta\mathrm{ch-c}(t_2 + t_3) + I_{D2}{}^2 \cdot \mathrm{Ron2} \cdot \theta\mathrm{ch-c}(t_3) \\
&\quad - \frac{t_1}{T} \cdot I_{D1}{}^2 \cdot \mathrm{Ron1} \cdot \theta\mathrm{ch-c}(t_2 + t_3) - \frac{t_1}{T} \cdot I_{D2}{}^2 \cdot \mathrm{Ron2} \cdot \theta\mathrm{ch-c}(t_3)
\end{aligned}$$

When:

θch–c$_{(t1)}$: PW = t_1, duty n% transient thermal resistance
θch–c $_{(t2)}$: PW = t_2 1shot pulse transient thermal resistance
θch–c $_{(t3)}$: PW = t_3 1shot pulse transient thermal resistance
SW loss : loss caused by t_{on}, t_{off} during switching
Ron : on-resistance max.(Tj max. = 150°C)

Example:

When using 2SK556, a waveform is produced such as that shown in Figure 33 (a), determine whether the following conditions are within the ASO: case temperature T_C = 50°C, I_{D1} = 3 A, t_1 = 10 µs, duty = 50% (f = 50 kHz), t_2 = 100 µs.

(1) The data sheet reveals that Ron_1 for I_{D1} = 3 A is o.55 Ω max. For a Tj max of 150°C, this value should be increased 2.2 to 2.4 times:

$Ron_1 = 2.4 \times 0.55 = 1.32\ \Omega$

(2) The data sheet reveals that according to I_D–Ron characteristics, Ron_2 for I_{D2} = 30 A is $Ron_2 \cong 0.8\ \Omega$ typ. For a Tj max of 150°C, Ron max should be increased 1.3 time:

$Ron_2 = 2.4 \times 1.3 \times 0.8 = 2.5$ (in actual practice, observation of the waveform is essential)

(3) For PW = t_1 = 10 µs, duty 50% transient thermal resistance θch-c$_{(t1)}$, the data sheet provides for $\gamma_{s(t)}$ = 0.5:

θch-c$_{(t1)}$ = γs(t) • θch-c = 0.5×1.25 = 0.625°C / W

(4) For PW = (t_2 + t_3) = 110 µs 1 shot θch-c$_{(t2 + t3)}$, the data sheet provides for $\gamma_{s(t)}$ = 0.04:

θch-c$_{(t2 + t3)}$ = $\gamma_{s(t)}$ • θch-c = 0.04×1.25 = 0.05°C / W

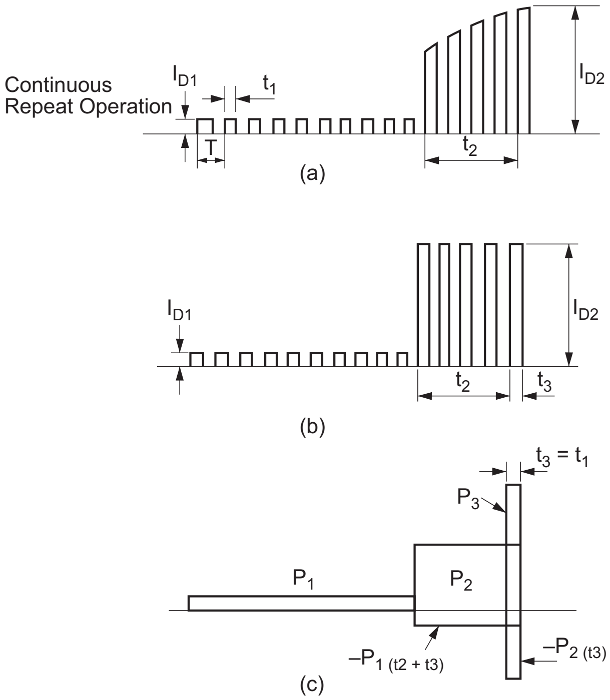


Figure 33 Sample Waveforms for Repeat Pulse Switching Operation with Non-constant Power Loss

(5) For PW = t_1 = 10 µs 1 shot θch-$c_{(t3)}$, the data sheet provides for $\gamma_{s(t)}$ = 0.015:

$$\theta ch\text{-}c_{(t3)} = \gamma_{s(t)} \bullet \theta ch\text{-}c = 0.015 \times 1.25 \cong 0.02°C / W$$

$$\begin{aligned}
\therefore Tj(peak) &= Tc + \theta ch - c(t_1)(I_{D1}{}^2 \cdot Ron1 + SW\ loss) \\
&\quad + \frac{t_1}{T} \cdot I_{D2}{}^2 \cdot Ron2 \cdot \theta ch - c(t_2 + t_3) + I_{D2}{}^2 \cdot Ron2 \cdot \theta ch - c(t_3) \\
&\quad - \frac{t_1}{T} \cdot I_{D1}{}^2 \cdot Ron1 \cdot \theta ch - c(t_2 + t_3) - \frac{t_1}{T} \cdot I_{D2}{}^2 \cdot Ron2 \cdot \theta ch - c(t_3) \\
&= 50 + 0.625\left\{(3^2 \times 1.32) + \frac{1}{2}(3^2 \times 1.32)\right\} + \frac{1}{2}(30^2 \times 2.5) \times 0\ 05 \\
&\quad + 30^2 \times 2.5 \times 0.02 - \frac{1}{2}(3^2 \times 1.32) \times 0.05 - \frac{1}{2}(30^2 \times 2.5) \times 0\ 02 \\
&= 50 + 11.1 + 56.3 + 45 - 0.3 - 22.5 \\
&= 139.6°C
\end{aligned}$$

Since Tj < Tj max, the operating conditions fall within the ASO.

6.2 Reverse Bias ASO

For power switching applications, such as switching regulators, the load of the switching device is usually inductive. Therefore, not only the forward bias ASO, as described in the preceding section, but also the reverse bias ASO should be considered. Generally, in a switching power supply, the emitter-base junction is reverse biased to reduce tstg and tf. In this case, the larger the current becomes, the smaller tstg and tf will be. And, according to it, the reverse bias ASO will be narrower, which means the operation area is more limited, as shown in Figure 34. On the other hand, in a power MOS FET, it is possible to make toff smaller by reverse bias of the gate, without narrowering the operation area. This gives flexibility in circuit design.

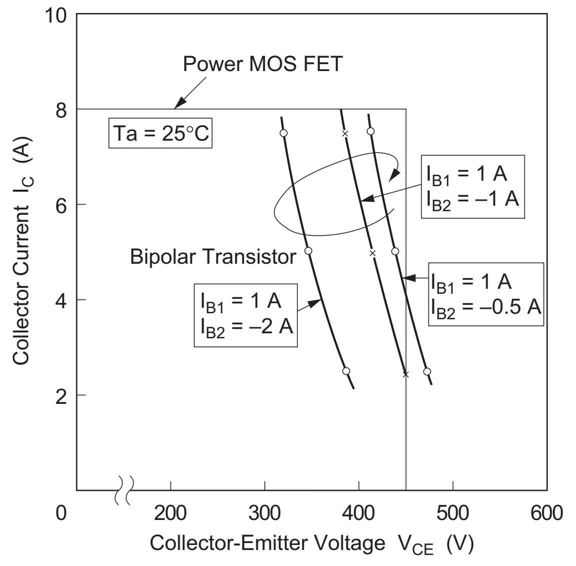


Figure 34 Reverse ASO

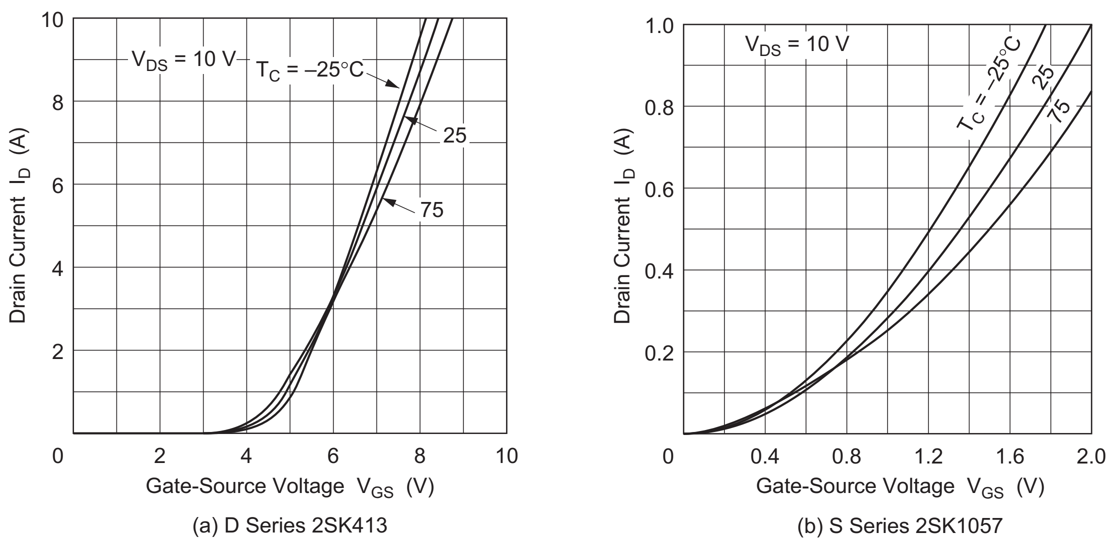


Figure 35 Typical Transfer Characteristics

7. Temperature Characteristics

Figure 35 shows the transfer characteristics of power MOS FETs. In the high current area, the temperature coefficient is negative and current concentration does not occur. A wide area of safe operation is provided and destruction by thermal runaway is largely prevented.

Since the transfer characteristics of power MOS FETs are of the enhancement type, as in the case of bipolar transistors, power MOS FETs don’t require a complex biasing circuit like depletion type FETs do.

The cross point at which the temperature coefficient becomes zero, is quite different between the D series device and the S series device, owing to their structures and processes. The cross point is 2 to 6 A D series device, and about 100 mA, in S series device, although it depends on device type.

Therefore, by setting the idling current about 100 mA, the S series MOS FET, when applied to a class-B push pull audio power amplifier, can dispense with a current temperature compensation circuit, which is required in bipolar transistor circuits.

8. Source-Drain Diode Characteristics

In both D series and S series Power MOS FETs, as shown in Figure 36 and Figure 37 a diode exists parasitically, between source and drain.

The forward current and the breakdown voltage ratings of this diode have the same characteristics as those of the power MOS FET.

Figure 38 shows the VF-IF characteristics of this diode, and Figure 39, the waveform of the backward recovery time (t_{rr}).

Also we would like to shown in Figure 40 the t_{rr}'s on a line scale, comparing the Fast Recovery Diode with some MOS FET's.

As is obvious from it, this diode has excellent characteristics, much the same as a typical diode. Moreover, when this diode is used in a bridge circuit, PWM amplifier output stage, etc, it can dispense with the external commutating diode, resulting in a reduction of the number of components.

If a channel is produced by making V_{GS} positive, the current flows equally in both directions.

When the current is low, V_F is given by $I_F \times$ Ron. The V_F of this diode is smaller than that of a typical diode. Therefore, in some cases, this diode is better than a typical one.

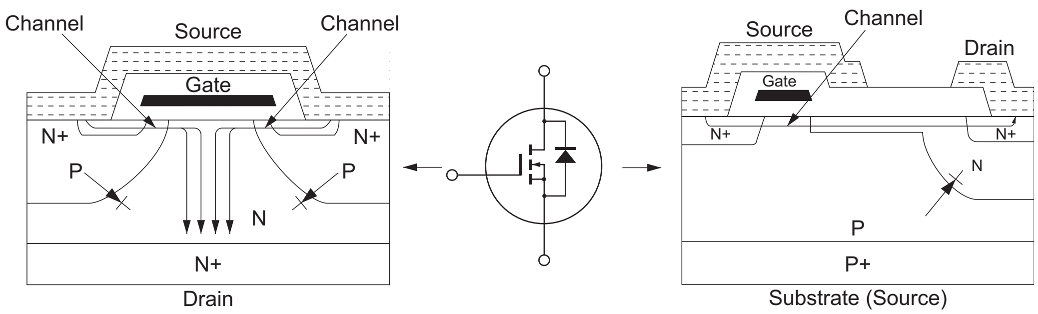


Figure 36 Structure of D Series) (Vertical type) (N channel)

Figure 37 Structure of S Series (Lateral type) (N channel)

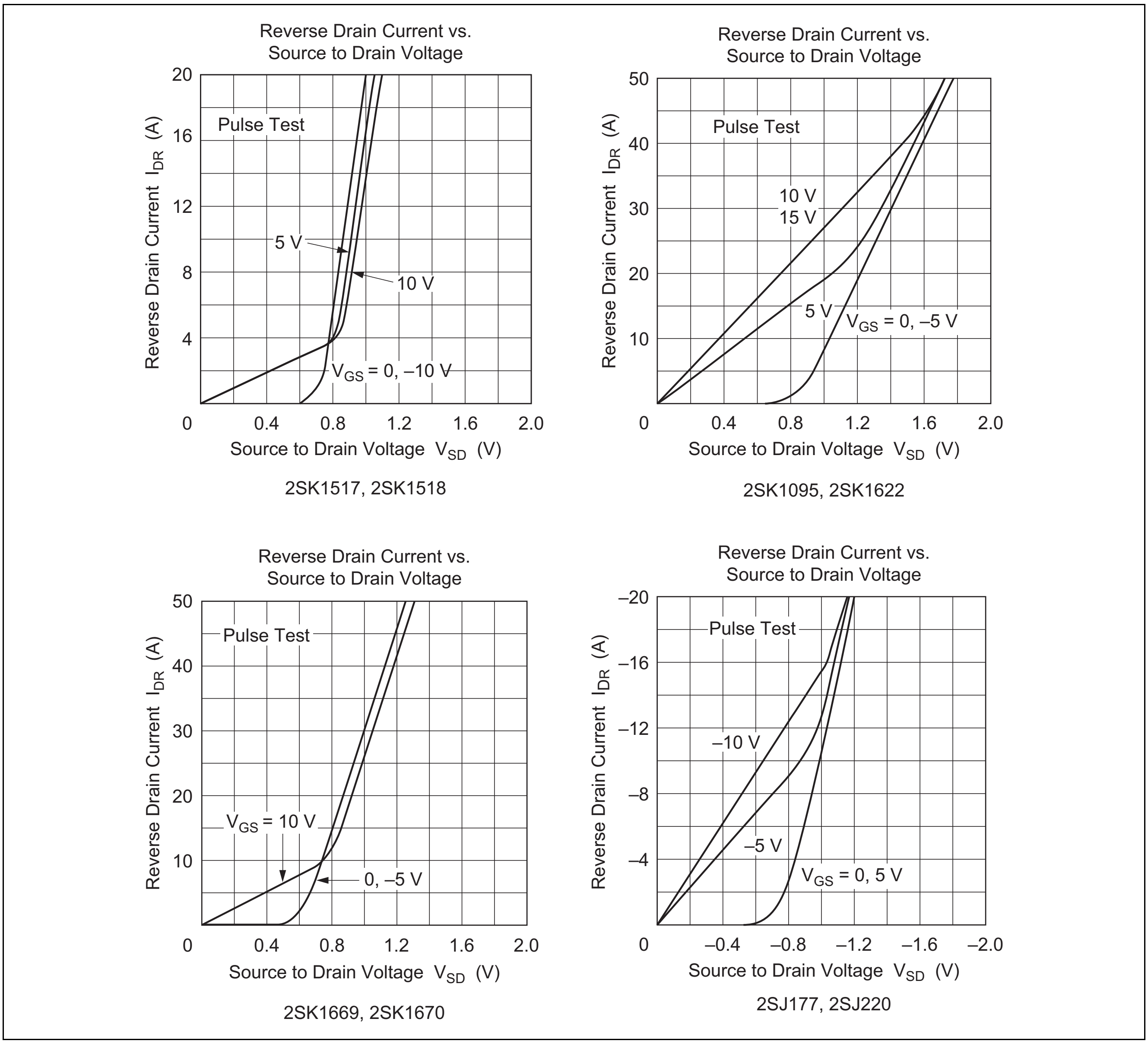


Figure 38 V_F-I_F Characteristics

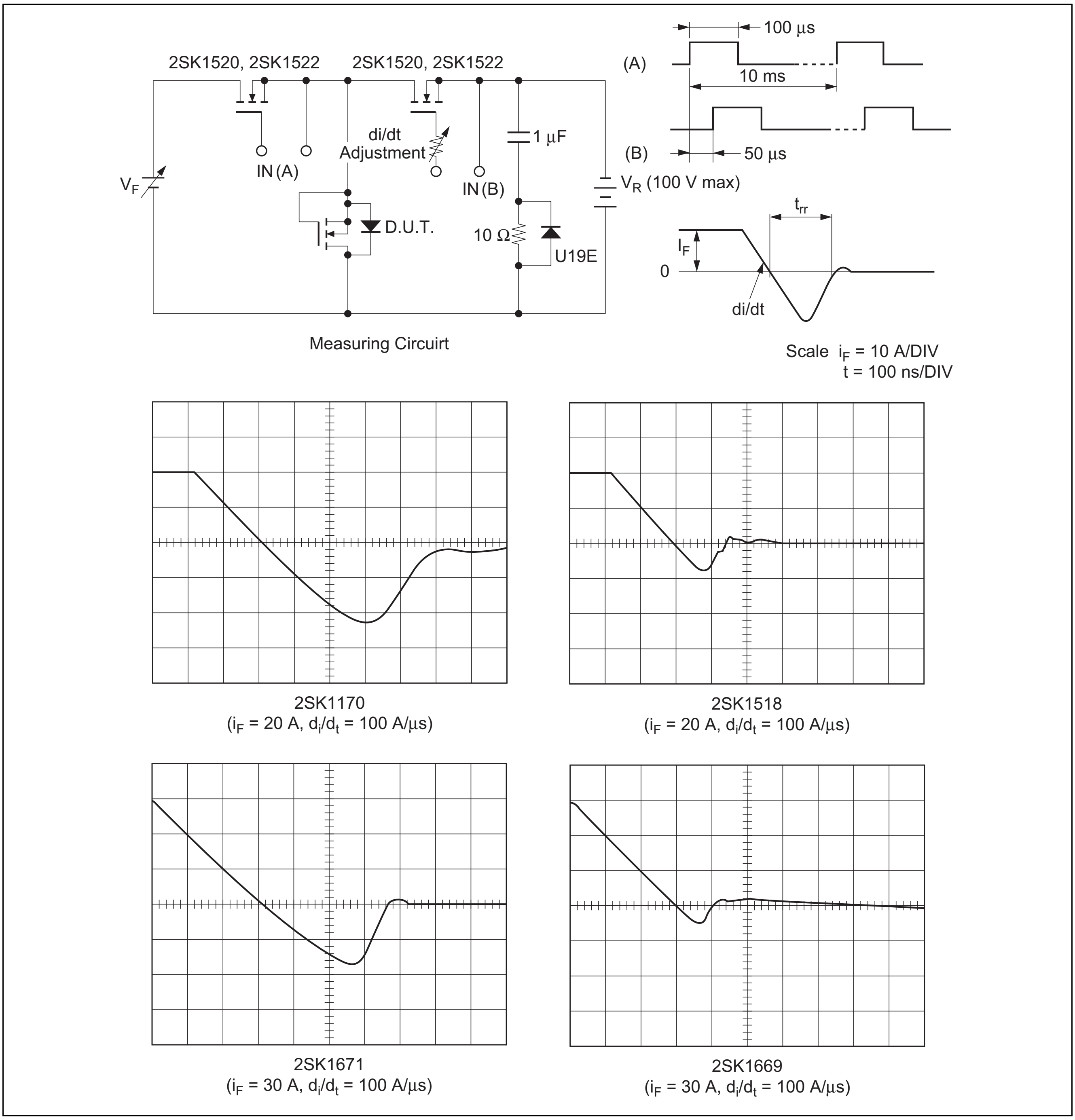


Figure 39 t_{rr} Waveform of the Built-in Diode

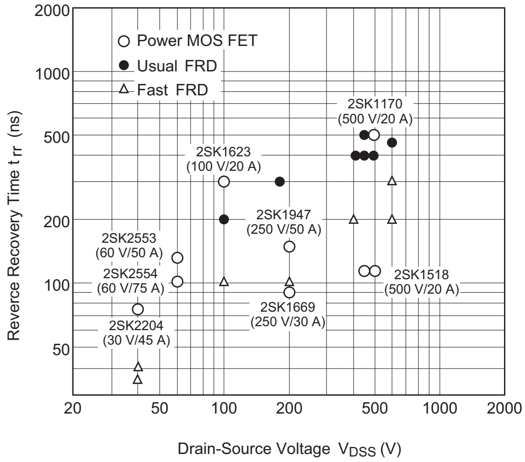


Figure 40 Comparison to the Built-in Diode and the FRD t_{rr}

8.1 Precautions in Handling the Built-in Diode

An built-in diode of the power MOS FET is used as a commutating diode in a motor control circuit. In this case, if the reverse voltage is charged immediately after a high current is supplied to the diode, it may be destroyed depending on the circuit and the operating conditions.

Figure 41 and 42 show a basic motor control circuit and the waveform of the motor control operation. These waveforms are at Q_2 and Q_3 off and Q_1 and Q_4 on. Q_4 is continuously on when Q_1 is chopping.

Gate drive signal is put into G_1, then Q_1 is switched on and i_{D1} flows. When Q_1 current i_{D1} is switched off, forward current, i_F flows through the built-in diode of Q_2 by the energy accumulated at the motor inductance. If Q_1 is switched on in this condition, Q_2 is into on state under the influence of reverse recovery time, trr of built-in diode on Q_2, and high level of reverse current (recovery current), i_{Dr} flows.

This excess recovery current may destroy the diode at a point in the shaded area in the figure, which indicates the period in which the built-in diode voltage recovers. Therefore, restricting the recovery current i_{Dr} is an effective method to prevent diode destruction. Table 2 shows the detailed circuit countermeasures.

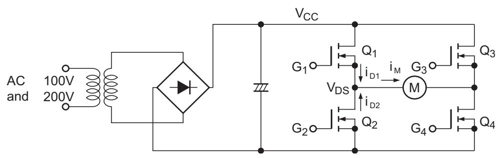
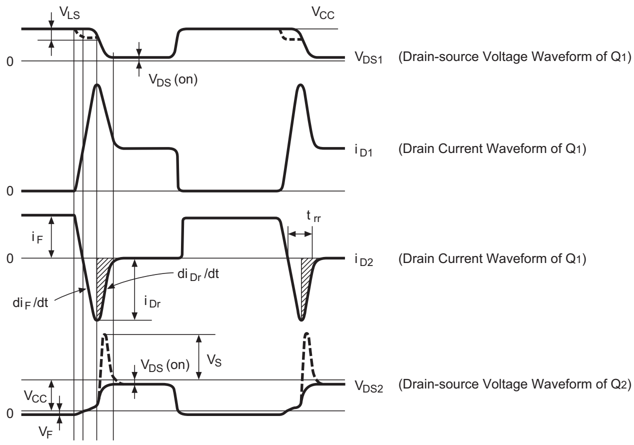


Figure 41 Typical Motor Control Circuit

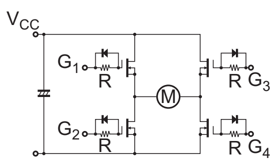
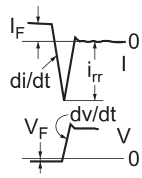
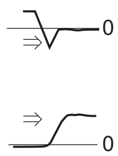
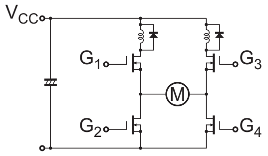
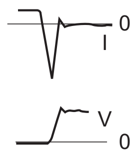
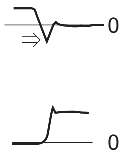
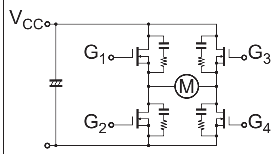
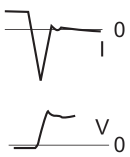
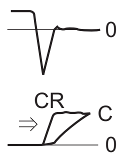
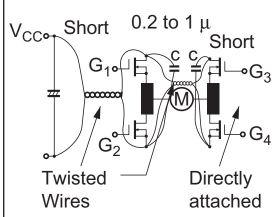
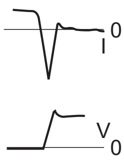
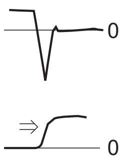
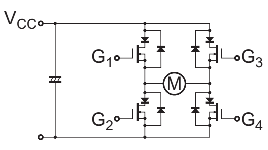
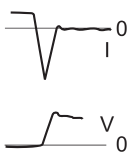
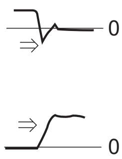


<Description>

i_F: Forward Current of Q_2 Built-in Diode
V_F: Forward Voltage Drop of Q_2 Built-in Diode
$V_{DS(on)}$: Drain-Source Saturation Voltage of Q_2
t_{rr}: Reverse Recovery Current Time of Q_2 Built-in Diode
V_{LS}: Voltage Drop with Current Inductance L_S
i_{Dr}: Reverse Recovery Current of Q_2 Built-in Diode (Dependes on the Drive Signal Source Impedance di_F/dt of Q_1, Circuit Inductance L_S, Supply Voltage V_{CC}, and Electric Charge Q_{rr} (or t_{rr}) in the Built-in Diode)
V_S: Spike voltage (Dependes on the Inductance L_S, i_{Dr}, and di_{Dr}/dt of the Circuit)

Figure 42 Waveform of the Motor Control Operation

Table 2 Circuit Countermeasures against Built-in diode Destruction

<table>
<tr><th rowspan="2">Classifi-cation</th><th rowspan="2">Countermeasures</th><th rowspan="2">Circuit</th><th colspan="2">Waveforms of the built-in diode</th><th rowspan="2">Circuit constants, etc.</th></tr>
<tr><th>Before improvement</th><th>After improvement</th></tr>
<tr><td>(1)</td><td>Delay the turn-on time, by inserting a resistor and diode which are connected in parallel into the gate of the Power MOS FET. This controls di / dt and dv / dt of the built-in diode to restrict the recovery current (in this case, the turn-off time does not have to be delayed).</td><td></td><td></td><td></td><td>R = 330 Ω to 820 Ω (di / dt = 20 to 50 A / µs)</td></tr>
<tr><td>(2)</td><td>Insert an L and diode connected in parallel into the drain of the Power MOS FET. This controls di / dt to restrict the recovery current i_{rr}.</td><td></td><td></td><td></td><td>L = 2 µH to 20 µH</td></tr>
<tr><td>(3)</td><td>Insert a C or CR snubber between the drain and source of the Power MOS FET to restrict dv/dt and voltage spike of the built-in diode.</td><td></td><td></td><td></td><td>R = 10 to 47 Ω
C = 0.01 µF to 0.1 µF Wiring of the snubber be as short as possible.</td></tr>
<tr><td>(4)</td><td>Wires between +, – terminals of the power supply line and the drain / source of each arm (in the case of N/N) should be twisted. C are also connected. By directly attaching wires to the upper and lower arms and minimizing stray inductance, the voltage spike and dv/dt are restricted.</td><td></td><td></td><td></td><td>Should be done together with countermeasures (1) to (3).</td></tr>
<tr><td>(5)</td><td>Connect the fast diode to the external of the Power MOS FET not to flow the current in the built-in diode.</td><td></td><td></td><td></td><td></td></tr>
</table>

9. Design of High Breakdown Voltage Application (Series Operation)

(1) Totem pole connection

Figure 43 shows a basic “totem pole” circuit, in which power MOS FETs are connected in series. This circuit has been used extensively as a saturated logic circuit, the basic circuitry for TTL IC. Operation of this circuit will be explained.

When no bias is applied to Q_1, Q_1 is cut off because power MOS FETs have enhancement type transfer characteristics, thus the following relationships hold;

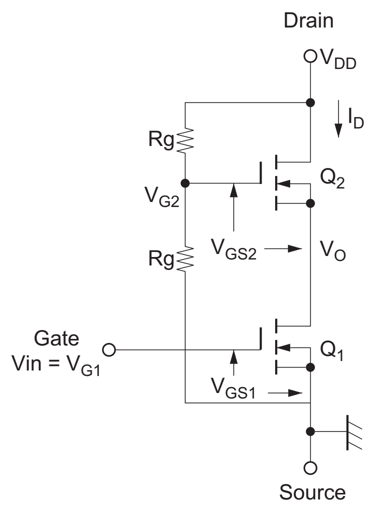


Figure 43 Basic Totem Pole Circuit

$$V_{G1} = 0, \ I_D = 0$$

$$V_{G2} = 1/2 \ V_{DD} (\therefore V_{G2} = V_{DD} \frac{Rg}{Rg + Rg})$$

$$\begin{aligned} V_D &= V_{G2} - V_{GS2} \\ &= 1/2 \ V_{DD} - Vth_2 \end{aligned}$$

where Vth_2 is the threshold voltage of Q_2. Generally, $Vth_2 << V_{DD}$. Therefore $V_O \cong 1/2V_{DD}$.

And the voltage applied to Q_1 and Q_2 will be about 1/2 V_{DD}.

Next, let us consider a transient state. When the gate bias of Q_1 is increased gradually from zero, Q_1 will become conductive and so will Q_2 at the same time. If load resistance Z_L is inserted between V_{DD} and drain of Q_2, drain voltage will be $V_D = V_{DD} - Z_L \bullet I_D$ and V_O (= $1/2V_D - V_{GS2}$) will gradually decrease.

If V_{DD} has much larger value than V_{GS2} and Q_2 is driven up to the saturation region, then the characteristics of an equivalent MOS FET would be dependent on Q_1.

Generally, when devices are operated in series, voltage unbalance due to switching time difference presents a problem. This problem is overcome in power MOS FETs because switching time can be made as short as several tens of nanoseconds.

Figure 44 and 45 show breakdown and output characteristics where a single device is used. When this device is used in the circuit shown in Figure 43, the breakdown and output characteristics would be as shown in Figures 46 and 47. Breakdown voltage in Figure 46 is twice as high as in Figure 44. The disadvantage is that on-resistance is also doubled, as is obvious from Figures 45 and 47. A method of improving on-resistance is described in the following section.

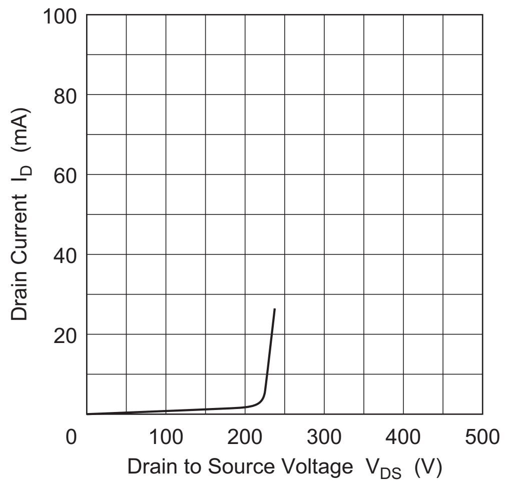


Figure 44 Breakdown Characteristics (Single Device)

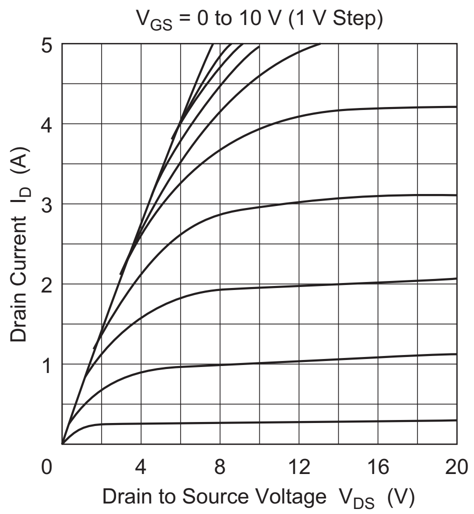


Figure 45 Output Characteristics (Single Device)

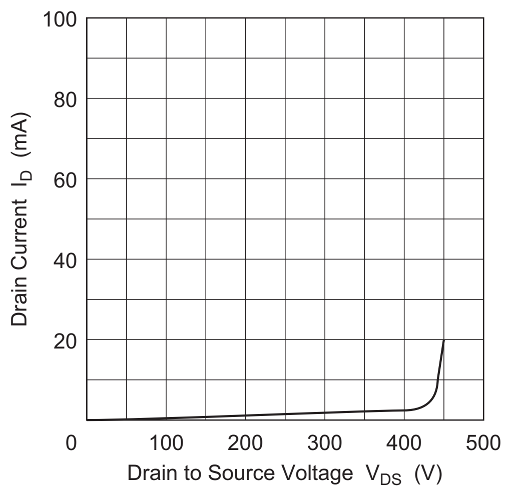


Figure 46 Breakdown Characteristics

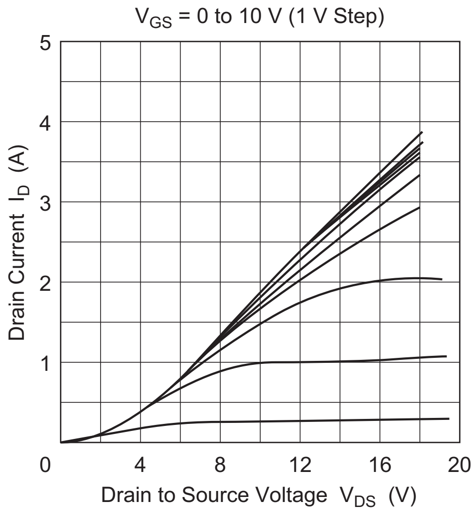


Figure 47 Output Characteristics

(2) How to reduce on-resistance in basic circuit

On-resistance (or saturation voltage) can be reduced by performing level shift of the Q_2 gate potential in the positive direction. This can be accomplished, for instance, by the methods shown in Figure 48. Figure 49 shows the output characteristics for a case where the gate is level-shifted to the positive side. (14 V is the maximum allowable gate-to-source voltage.)

In the circuit shown in Figure 48 as in the basic circuit, the equivalent drain to source breakdown voltage is twice as high as when a single device is used.

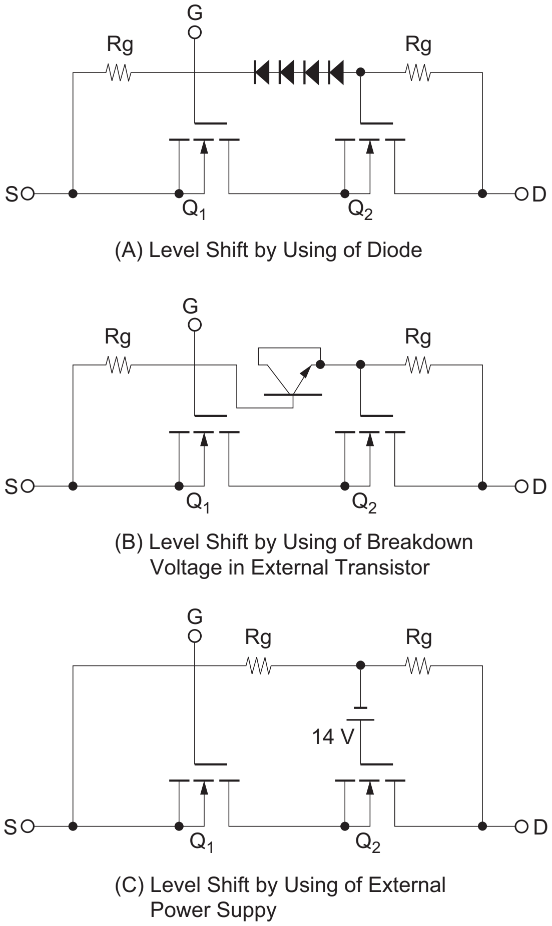


Figure 48 How to Reduce ON-Resistance

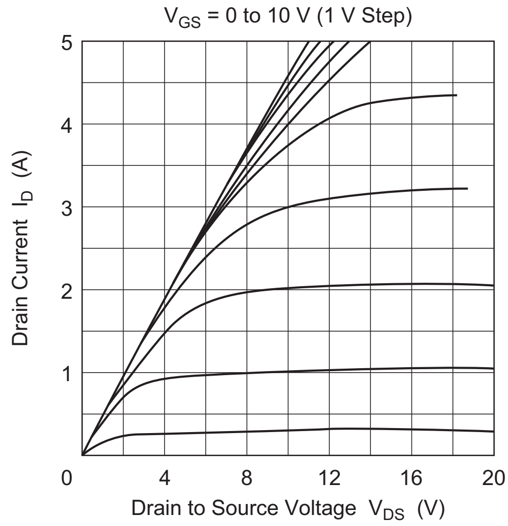
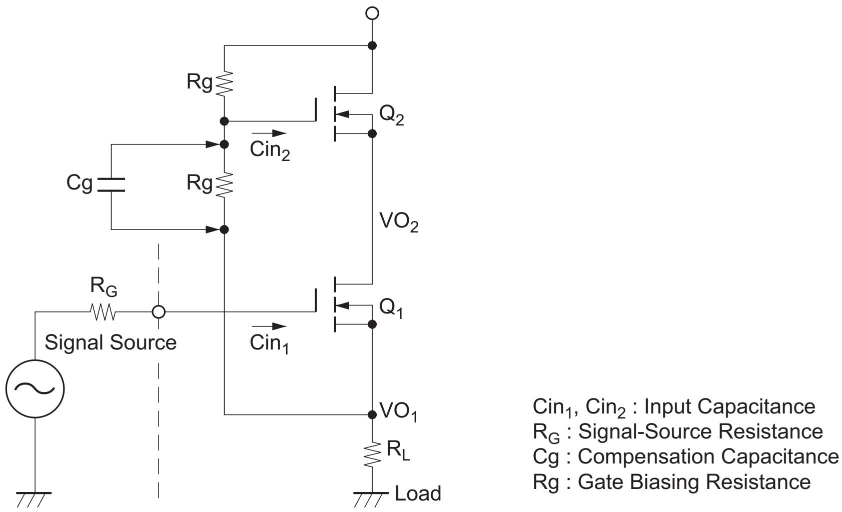


Figure 49 Output Characteristics ((C) Circuit)

(3) Improvement of high frequency characteristics in totem pole connection

When the circuit shown in Figure 43 is modified for a source follower, because of the different operation of Q_1 and Q_2, a phase differential occurs under the influence of the power MOS FET input capacitance (about 500 pF for 2SK1057, 600 pF for 2SJ161, f = 1 MHz). As a result, characteristics worsen, as high frequency gain droops and phase shift increases.



Figures 50 Improved Totem Pole Circuit

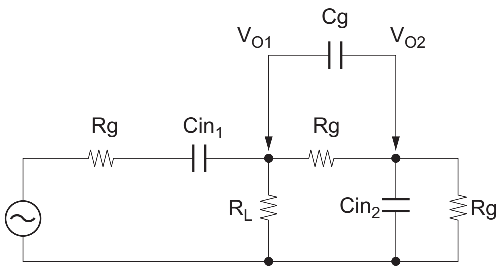


Figure 51 Passive Equivalent Circuit of Totem Pole

This is expressed in Figure 50. The equivalent circuit with passive devices alone is represented in Figure 51. It has been verified experimentally that the phase differential of V_{O1} and V_{O2} can be eliminated and driving in the same phase can be achieved by equalizing Cg with Cin_2 and that phase shift as 100 kHz can be limited within –90 degrees.

10. Analysis of Oscillation in Source Follower Circuits

<Reference>

There have been many works on analysis of oscillation in source follower circuits. The most general analysis for source follower circuits is about the case in which the real part of the input impedance is negative and the imaginary part is ZERO. An example is described as followers. The simplified equivalent circuit of source follower is shown in Figure 22.

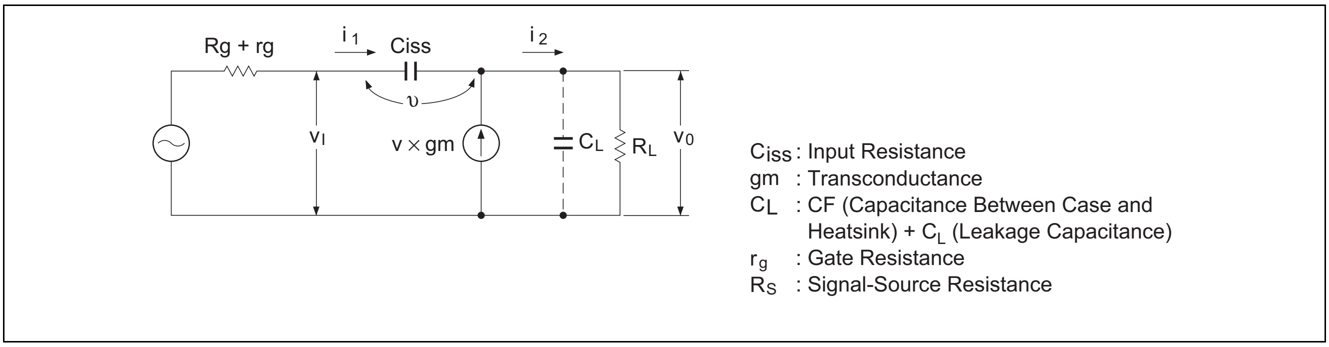


Figure 52 Equivalent Circuit of Source Follower Circuit

The input impedance Zin can be obtained as follows;

$$Zin = \frac{Vi}{i_1} = \frac{1}{j\omega Ciss} + R_L\left(1 + \frac{g_m}{j\omega Ciss}\right) \quad \cdots\cdots (1)$$

In the case of load consisting of paralleled resistor and capacitor Substitute $\frac{R_L}{1 + j\omega C_L R_L}$ instead of R_L in equation (1).

$$Zin = \frac{1}{j\omega Ciss} - \frac{j\omega C_L R_L{}^2}{1+\omega^2 C_L{}^2 R_L{}^2} - \frac{j\omega \ g_m \ R_L}{(1+\omega^2 C_L{}^2 R_L{}^2)\omega^2 Ciss} + \frac{R_L}{1+\omega^2 C_L{}^2 R_L{}^2} - \frac{\omega^2 C_L R_L{}^2 g_m}{(1+\omega^2 C_L{}^2 R_L{}^2)\omega^2 Ciss} \quad \cdots\cdots (2)$$

The condition for negative resistance is;

$$R_S + r_g + \frac{R_L}{1+\omega^2 C_L{}^2 R_L{}^2} - \frac{C_L R_L{}^2 g_m}{(1+\omega^2 C_L{}^2 R_L{}^2)Ciss} < 0 \quad \cdots\cdots (3)$$

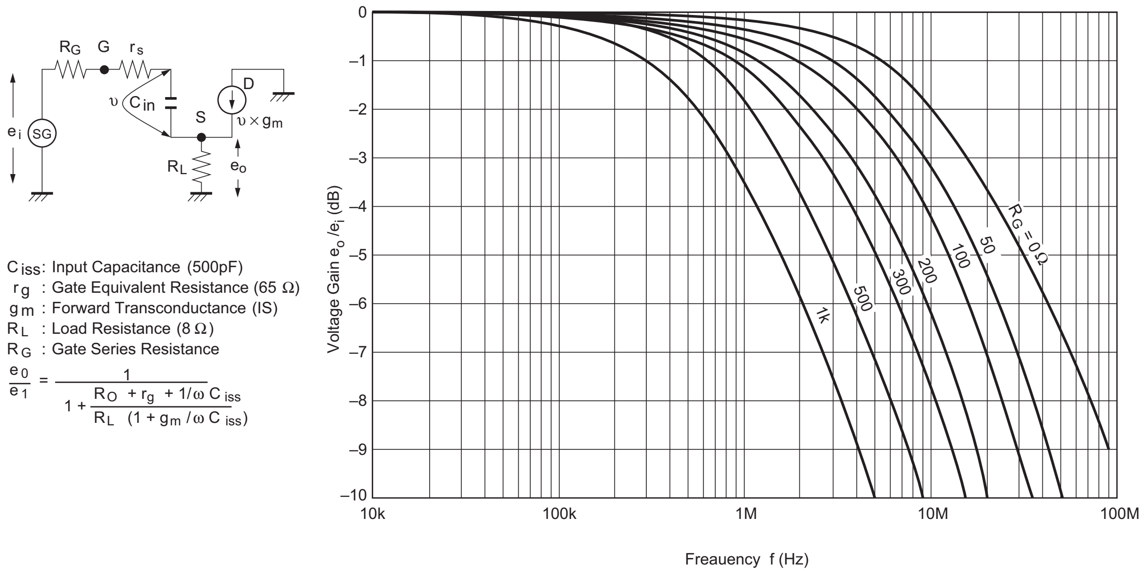
moreover, approximately,

$$R_S + r_g + R_L - \frac{C_L R_L{}^2 g_m}{Ciss} < 0 \quad \cdots\cdots (4)$$

Therefore, to prevent oscillation, external gate resistor R_G should be inserted. Then the following equation can be obtained.

$$R_G + R_S + r_g + R_L - \frac{C_L R_L{}^2 g_m}{Ciss} \geq 0$$

However, the insertion of external R_G makes Power MOS FETs frequency response worse. Therefore, when selecting R_G, a compromise between stability against oscillation and amplifier's frequency response should be considered. Voltage gain vs. frequency vs. R_G is shown in Figure 53.

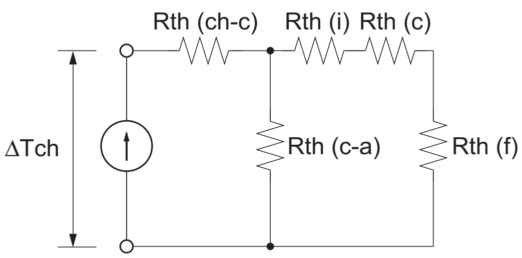


$$\frac{e_0}{e_1} = \frac{1}{1 + \frac{R_O + r_g + 1/\omega C_{iss}}{R_L \ (1 + g_m/\omega C_{iss})}}$$

Figure 53 Frequency Characteristics of Source Follower (Calculated Value)

11. Thermal Design

1. Channel, Package and Surrounding Air Thermal Resistances
   The total thermal resistance up to the surrounding air as seen from the channel is expressed by formula (1), which is derived from the equivalent circuit shown in figure 54.



Rth (ch-c): Thermal resistance from the channel to the package case
Rth (c-a) : Thermal resistance from the case to the immediate exterior atmosphere
Rth (i) : Thermal resistance of insulating layer
Rth (c) : Thermal resistance of contacts
Rth (f) : Thermal resistance of heat sink
Rth : Total thermal resistance

Figure 54 Equivalent Circuit

$$\mathrm{Rth} = \mathrm{Rth(ch-c)} + \frac{\mathrm{Rth(ch-a)} \cdot (\mathrm{Rth(i)} + \mathrm{Rth(c)} + \mathrm{Rth(f)})}{\mathrm{Rth(ch-a)} + \mathrm{Rth(i)} + \mathrm{Rth(c)} + \mathrm{Rth(f)}} \quad \cdots\cdots (1)$$

Table 3 lists the thermal resistance items for each package. (Provided as reference values.)
While the thermal resistance from the case to the surrounding air (Rth(c-a)) is determined by the transistor case materials and shape, as can been seen in table 6-3, its value is relatively large as compared to the values for Rth(i), Rth(c), and Rth(f). As a result it is possible to approximate formula (1) by formula (2) for practical application.

$$\mathrm{Rth} = \mathrm{Rth(ch-c)} + \mathrm{Rth(i)} + \mathrm{Rth(c)} + \mathrm{Rth(f)} \cdots\cdots (2)$$

Table 3 Thermal Resistance

Thermal resistance term			Package						
			DPAK	**TO-220AB**	**LDPAK**	**TO-220FM**	**TO-3P**	**TO-3PFM**	**TO-3PL**
Rth(ch-c)	(°C/W)		$Rth(ch-c) = \frac{Tj\ \ max - Tc}{Pch}$			(The Pch (W) ratings are listed in the individual product catalogues.)			
(Note 1) Rth(c-a)	(°C/W)		178	80	80	62.5	55	42	45
(Rth(i) + Rth(c)) (°C/W)	No insulating layer used	Silicon grease used	0.3 to 0.6	0.3 to 0.5	0.3 to 0.5	0.4 to 0.6	0.1 to 0.2	0.3 to 0.5	0.1 to 0.2
		Silicon grease not used	2.0 to 2.5	1.5 to 2.0	1.5 to 2.0	1.5 to 2.0	0.5 to 0.9	1.0 to 1.5	0.4 to 0.5
	Mica sheet inserted. (t = 50 to 100 µm)	Silicon grease used	—	2.0 to 2.5	—	—	0.5 to 0.8	—	0.5 to 0.7
		Silicon grease not used	—	4.0 to 6.0	—	—	2.0 to 3.0	—	1.2 to 1.5

Notes: 1. Reference values

2. Calculating the Channel Temperature, Tch

   a. When a heat sink is used and the transistor case temperature is not known

$$Tch = Ta + P_D \bullet (Rth(ch\text{-}c) + Rth(i) + Rth(c) + Rth(f)) \quad \cdots\cdots (3)$$

   b. When a heat sink is used and the transistor case temperature is known (thermal equilibrium state)

$$Tch = Tc + P_D \bullet Rth(ch\text{-}c) \quad \cdots\cdots (4)$$

   c. When no heat sink is used (independent device)

$$Tch = Ta + P_D \bullet (Rth(ch\text{-}c) + Rth(c\text{-}a)) \quad (5)$$

1) Rth(ch-c) is computed using formula (6) from the allowable channel power (Pch) rating listed in the product catalog.

$$Rth(ch-c) = \frac{Tch\ \ max - Tc}{Pch} \quad \cdots\cdots (6)$$

<Example>

Since the Pch from the catalog is 120 W, the Rth(ch-c) for the 2SK1170 (TO-3P) is calculated as follows.

$$Rth(ch-c) = \frac{150 - 25}{120} \cong 1.04°C / W$$

2) When the drain power dissipation is a pulse state dissipation, the historical thermal resistance, Rth(ch-c)(t), is used. In general, the time required for Rth(ch-c) to reach steady state (the thermal equilibrium state) is 1 to 10 seconds, while that for Rth(c-a) is on the order of a few minutes. Therefore, the temperature rise for narrow width pulse power dissipations is limited to the vicinity of the channel. Pulse widths of less than 100 ms (one shot pulses) have essentially no effect on transistor thermal states and temperature increases.

<Example>

Consider the 2SK1170 (TO-3P). Derive the transient thermal resistance Rth(ch-c)(t)1 for a one shot pulse with a pulse width (PW) of 10 µs, and the transient thermal resistance Rth(ch-c)(t)2 for continuous operation with a 20% duty cycle and a PW of 10 µs.

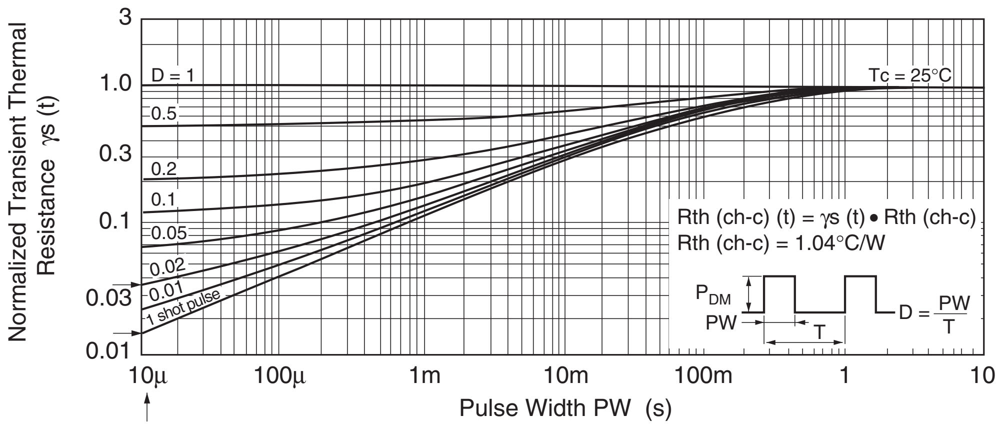


Figure 55 2SK1170 Transient Thermal Resistance Characteristics (from the separate catalog)

According to the transient thermal resistance characteristics listed in the separate catalog for the 2SK1170, these thermal resistances have the following values.

$$Tch(ch\text{-}c)(t)1 = \gamma s(t) \bullet Rth(ch\text{-}c) = 0.015 \times 1.04 = 0.0156°C/W$$

$$Tch(ch\text{-}c)(t)2 = \gamma s(t) \bullet Rth(ch\text{-}c) = 0.034 \times 1.04 = 0.035°C/W$$

d. Channel Temperature Tch Calculation Example

1) Mounting and operating conditions
   - a) The chip used in the 2SK1170 (TO-3P)
   - b) I_D = 8 A, PW = 10 μs, duty = 50% (f = 50 kHz)
     Switching power $P(t_f)$ = 500 W (t_f = 0.2 μs)
     (Here we only consider the power during the falling period t_f. Other losses are ignored.)
   - c) Heat sink thermal resistance Rth(f): 1°C/W (natural air cooling)
   - d) Ambient temperature Ta: 50°C atmosphere
   - e) Mounting method: Mica sheet and silicon grease

2) Method for calculating the channel temperature Tch
   - a) The total thermal resistance Rth is derived as follows by substituting the thermal resistances from table 6-3 into formula (2).

$$\begin{aligned} Rth &= Rth(ch\text{-}c) + Rth(i) + Rth(c) + Rth(f) \\ &= 1.04 + 0.8 + 1 \\ &= 2.84°C/W \end{aligned}$$

   - b) The power MOS FET power dissipation P_D is derived by substituting the required values into formula (9).

$$\begin{aligned} P_D &= \frac{1}{T}(t_{ON} \cdot I_D{}^2 \cdot R_{DS(on)}\max \cdot \alpha + P(t_f) \cdot t_f) \\ &= \frac{1}{20}(10 \times 8^2 \times 0.27 \times 2.41 + 500 \times 0.2) \\ &= \underline{25.8W} \end{aligned}$$

   - c) The channel temperature Tch is derived by substituting the Rth and P_D values calculated above into formula (3).

$$\begin{aligned} Tch &= Ta + P_D \bullet Rth \\ &= 50 + 25.8 \times 2.84 \\ &\cong 123°C \end{aligned}$$

Assuming that a power pulse $P_D(t)$ of 500 W is applied for a time (pulse width) of PW = 50 μs (one shot pulse) in these operating conditions, the additional temperature increase ΔTch can be derived using the transient thermal resistance Rth(ch-c) from figure 55 as follows.

$$\begin{aligned} \Delta Tch &= \Delta P_D \bullet Rth(ch\text{-}c)(t) \\ &= (500 - 25.8) \times (1.04 \times 0.032) \\ &\cong 15.8°C \end{aligned}$$

Therefore, the temperature will rise an addition 15.8°C, and become about 140°C.

3. Thermal Design Technique
   a. This section describes thermal design for applications using the 2SK1170 (TO-3P) power MOS FET. Here, we design for a Tch of 120°C or less under the mounting conditions described in items (1) through (4) below.
      (1) Operating conditions: I_D = 8 A, 10 A, PW = 10 µs (t_{ON}), duty = 50% (f = 50 kHz)
      Switching loss $P(t_f)$ = 500 W (t_f = 0.2 µs)
      (Here we only consider the power during the falling period tf. Other losses are ignored.)
      (2) Heat sinks used: Here we investigate three different heat sinks, with thermal resistances Rth(f) of 0.5°C/W, 1.0°C/W, and 1.5°C/W.
      (3) Mounting method: Mica sheet and silicon grease
      (4) Ambient temperature: Ta = 50°C

   b. Allowable power dissipation and power MOS FET power dissipation characteristics due to the total thermal resistance Rth when a heat sink is used.
      (1) The power MOS FET channel temperature Tch is given by formula (7).

$$\begin{aligned} Tch &= Ta + \Delta Tch \\ &= Ta + P_D \bullet Rth \quad \cdots\cdots (7) \end{aligned}$$

$$\therefore P_D = \frac{Tch - Ta}{Rth} \quad \cdots\cdots (8)$$

Formula (8) can be used to derive the allowable power dissipation line (Tch dependency) for the total thermal resistance Rth for the 2SK1170 under the mounting conditions specified above at Ta = 50°C for Tch values up to a maximum of about 150°C.

(2) Next we derive the power MOS FET power dissipation characteristic (Tch dependency)
Since the on resistance $R_{DS(on)}$ has a positive temperature dependency, the power dissipation P_D of a power MOS FET increases with increases in the channel temperature Tch.
The power dissipation P_D can be derived using formula (9).

$$P_D = \frac{1}{T}(ton \cdot I_D{}^2 \cdot R_{DS(on)}max \cdot \alpha + P(t_f) \cdot t_f) \quad \cdots\cdots (9)$$

Where a is the temperature coefficient for Tch(n) with respect to 25°C.
Figure 56 shows the relationship between channel temperature (Tch) and power dissipation (P_D) as derived from formulas (8) and (9).

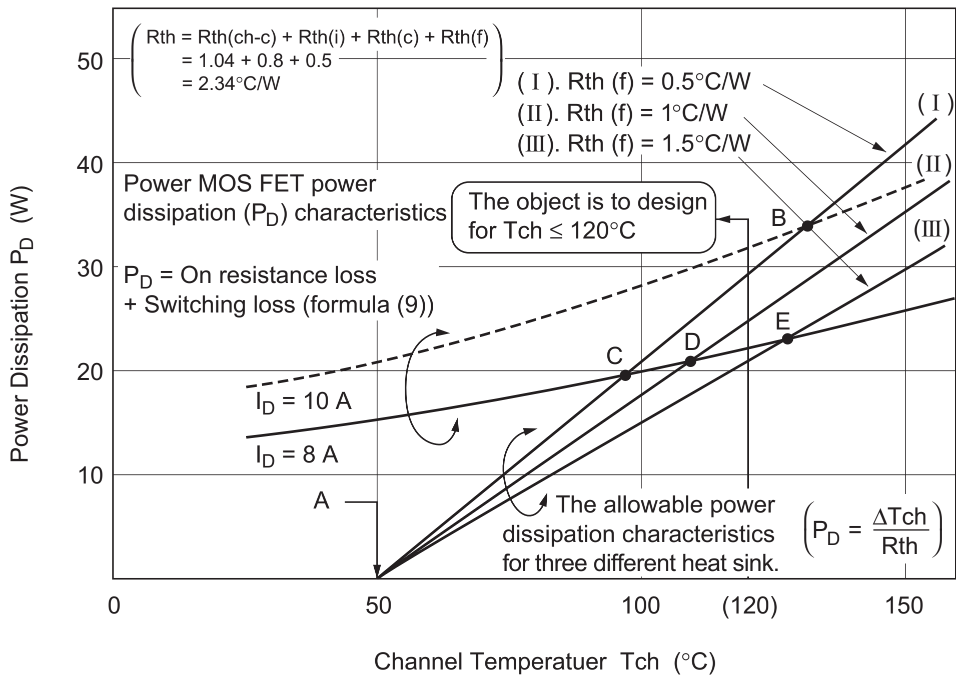


Figure 56 Channel Temperature (Tch) vs. Power Dissipation (P_D) Relationship

Table 4 Power MOS FET Power Dissipation (P_D) Calculations (for the 2SK1170)

Item		Tch (°C)							
		25	40	60	80	100	120	140	150
$R_{DS(on)}$ temperature coefficient α, with respect to Tch = 25°C		1.0	1.09	1.27	1.5	1.73	2.0	2.27	2.41
On resistance power dissipation P_{ON} $P_{ON} = \frac{t_{ON}}{T} \cdot I_D{}^2 \cdot R_{DS(on)}\ \mathrm{max} \cdot \alpha$	I_D = 8 A	8.64	9.4	11.0	13.0	14.9	17.3	19.6	20.8
	I_D = 10 A	13.5	14.7	17.1	20.3	23.4	27	30.6	32.5
Switching loss $Ps = \frac{t_f}{T} \cdot P(t_f)$		5	5	5	5	5	5	5	5
Total power dissipation	I_D = 8 A	13.6	14.4	16.0	18.0	19.9	22.3	24.6	25.8
$P_D = P_{ON} + P_S$	I_D = 10 A	18.5	19.7	22.1	25.5	28.4	32.0	35.6	37.5

Notes: 1. For simplification, the same values of P_S are used for both values of I_D, 8 A and 10 A.

c. The following can be said based on the relationship between the channel temperature and the power dissipation shown in figure 6-56.
   1) The point marked A is the point where the ambient temperature Ta is 50°C. That is, since the power dissipation is "zero", the values of Tch and Ta will be identical, i.e., 50°C.
   2) The points B, C, D, and E are intersections between the total thermal resistance characteristics for the different heat sinks and the power MOS FET power dissipation characteristics. They indicate the channel temperature (Tch) under a state of thermal equilibrium.
      Therefore, the following techniques and methods should be discussed as thermal designs and operating conditions to fulfill the condition that Ta be less than or equal to 120°C.
      (a) The heat sink used must meet either specification (I) or (II). However, the I_D must be 8 A.
      (b) Consider the operating conditions with an I_D of 10 A. Since there is no intersection between the total thermal resistance and the power dissipation curves for heat sinks II and III, this means that these conditions can result in thermal runaway leading to destruction of the device. Also, since the Tch under thermal equilibrium conditions for the type I heat sink is about 130°C, although this heat sink meets the device rating (Tch max ≤ 150°C), it does not meet the design target of a Tch less than or equal to 120°C.
      (c) Therefore, to operate at conditions up to an I_D of 10 A and to fulfill the design target (Tch ≤ 120°C) either the heat dissipation conditions must be improved, or a device with a one rank smaller on resistance must be used.

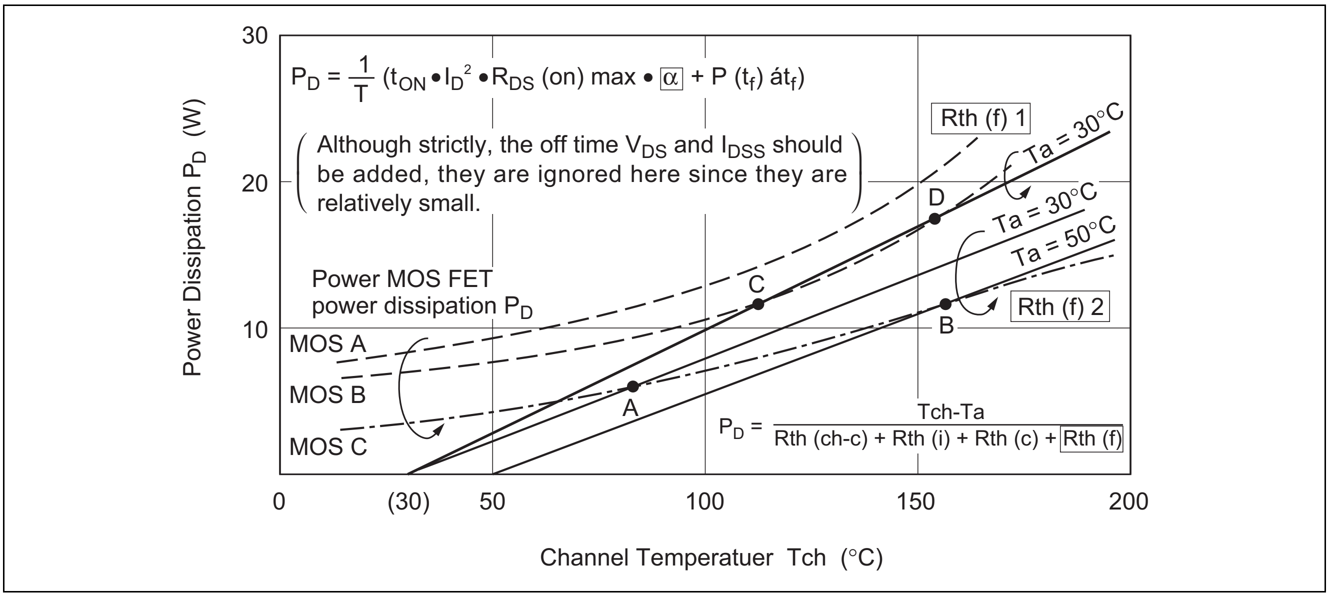


Figure 57 Channel Temperature (Tch) vs. Power Dissipation (P_D) Relationship

d. This section describes examples based on figure 57.

1) When MOS A or MOS B is used with the heat sink with thermal resistance Rth(f)1:

a) Since there is no intersection between the total thermal resistance and power dissipation curves when MOS A is used, there is no thermal equilibrium state, and thermal runaway can lead to destruction of the device.

b) When MOS B is used, although the channel temperature rises to the thermal equilibrium point at C (about 110°C) when power is applied, there is still significant danger of thermal runaway. This is because the influence of an unstable external environment (an unstable ambient temperature Ta or another heat source in the vicinity) can cause the channel temperature Tch to reach point D (about 150°C), where thermal runaway can occur.

2) Using the heat sink with thermal resistance Rth(f)2 and operating at ambient temperatures of 30 and 50°C.

a) When operating at a Ta of 30°C the system will be in thermal equilibrium at point A (Tch = 83°C) and there will be no problems.

b) When operating at a Ta of 50°C the system will be in thermal equilibrium at point B (Tch = 154°C). This temperature exceeds the rated allowable channel temperature (150°C). Although this will not immediately destroy the device, it will reduce its life and make the various failure modes more likely to occur.

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Revision History

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		Page	Summary
1.00	Jul.18.04	-	First edition issued
2.00	Dec.25.08	19	Amended
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