EFT Immunity for the RAA78817x Family of 3.3V RS-485/RS-422 Transceivers

This application note discusses the immunity for the RAA78817x family (RAA788170, RAA788172, RAA788173, RAA788175, RAA788176, RAA788178) of RS-485/RS-422 transceivers to repetitive Electrical Fast Transients (EFT) as defined in IEC61000-4-4. It describes the EFT test setup and the transceiver performance under the application of EFT pulses. Subsequent ATE tests confirm an EFT immunity of 3kV at 5kHz and 100kHz repetition rates for all RAA78817x transceivers, which places them into the test level 4 category of IEC61000-4-4.

Contents

1. EFT Test according to IEC61000-4-4

The EFT test applies a burst of 75 fast transients that are coupled into the data lines of an RS-485 data link. Significant for the test pulses are the high amplitude, the short rise time, the high repetition rate, and the low energy of the transients. This test checks the immunity of RS-485 transceivers when subjected to fast transients, such as those generated by the switching of inductive loads and relay contact bounce. The preferred test levels for the electrical fast transient test, applicable to data ports are listed in Table 1.

Table 1. EFT Test Levels

Test Level	Test Voltage (kV)	Repetition Frequency (kHz)[1]
1	0.25	5 or 100
2	0.5	5 or 100
3	1	5 or 100
4	2	5 or 100
X[2]	Special	Special

1. The use of 5kHz repetition rates is traditional, however, 100kHz is closer to reality.
2. X is an open level. The level has to be specified in the dedicated equipment specification.

An EFT transient has a rise time of 5ns and a pulse width (where V_{Test} is > 50% $V_{Test-PK}$) of 50ns (Figure 1). The burst period is 300ms and consists of 75 EFT pulses (t_{Burst}) followed by a break interval. Depending on the repetition frequency, t_{Burst} is 15ms at f_{Rep} = 5kHz, or 0.75ms at f_{Rep} = 100kHz. The total test time, comprising multiple burst periods, must be at least one minute (Figure 2).

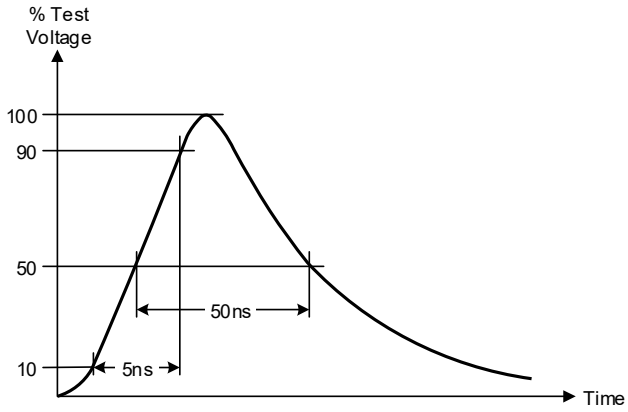

Figure 1. EFT Pulse Waveform

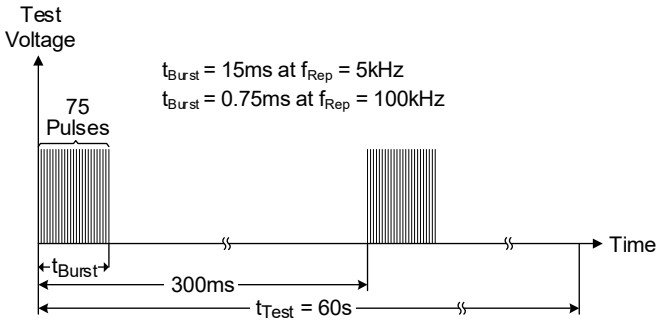

Figure 2. EFT Test Timing

Figure 3 depicts the principle test set-up for the application of the test voltage by a capacitive coupling clamp for laboratory test purposes.

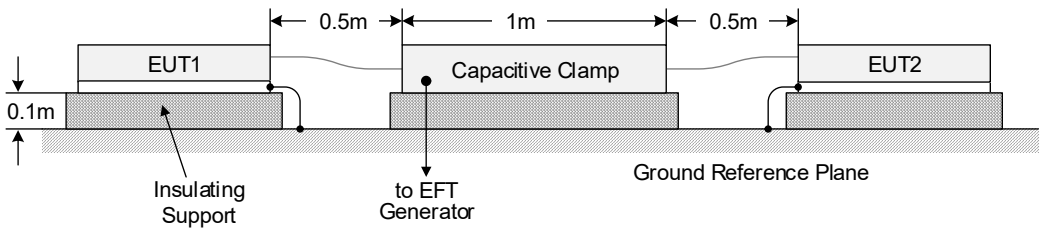

Figure 3. Test Setup with a Capacitive Clamp for Laboratory Tests

In this setup, two equipment under test (EUTs) are tested simultaneously. With both EUTs being equally distanced from the clamp by 0.5m, and a capacitive clamp length of 1m, the total test cable length is 2m (6ft). The entire setup is placed on top of a ground reference plane, with the EUTs and the clamp being isolated from the reference plane by an insulating support material of 0.1m height.

2. Actual Test Setup

Figure 4 show the schematic of test setup for testing the EFT immunity of RS-485 transceivers. A data signal in form of a square wave is applied to the data input (DI) of the left node. This node is configured as a driver whose output is looped back to the receiver output (RO1), which is captured with the oscilloscope. The driver transmits data to the receiving node on the right, whose output (RO2) is also captured with the scope. During transmission, the EFT test voltage is raised until one of the transceivers latches up first.

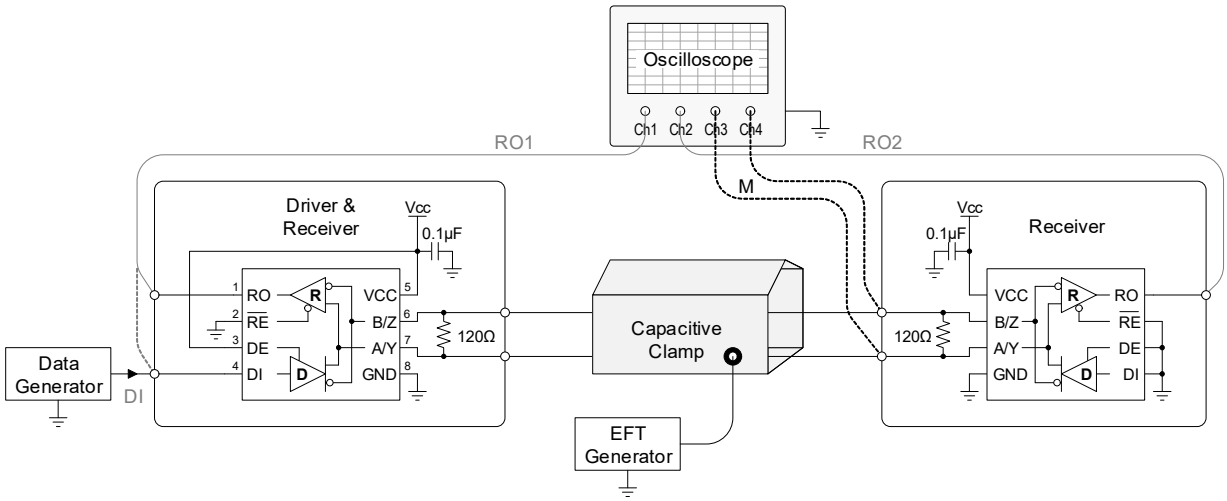

Figure 4. Schematic of Laboratory Test Setup

A second measurement (dotted lines) is performed that captures the differential bus signal (M) and compares it with the data input (DI). M is the math-function of the scope that calculates the difference of the individually measured signals on the A and B bus lines.

Figure 5 shows a picture of the actual test setup using the AXOS-5 test system.

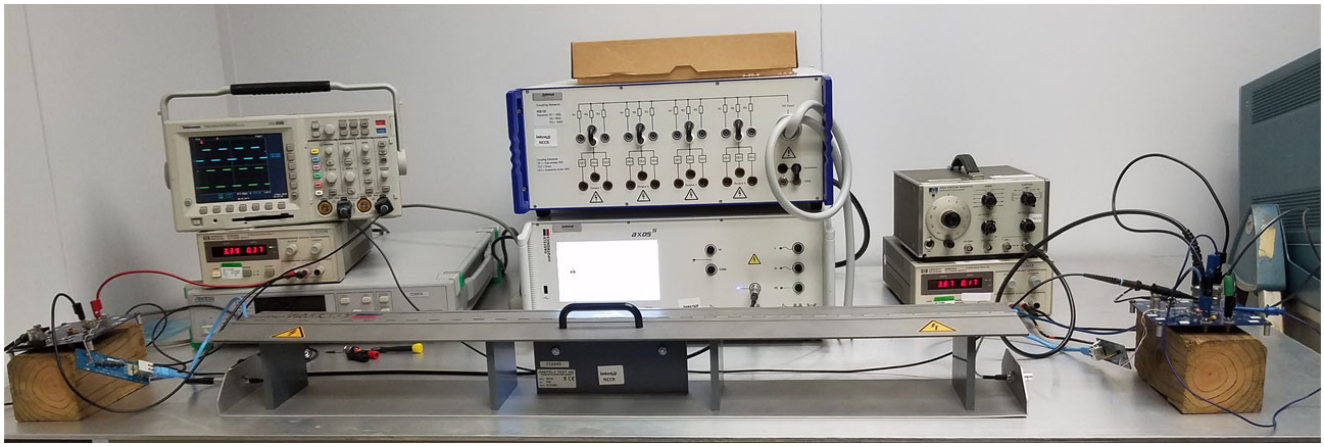

Figure 5. Photograph of Laboratory Test Setup

3. Test Performance

Figure 6 depicts the receiver output signals before and after the EFT test (DR = 250kbps, f_{REP} = 5kHz). Figure 7 shows the same outputs during the EFT test at a ten-times larger time base. It can be seen that a single EFT pulse corrupts several data bits. Also, the EFT transients on the bus traverse through the unprotected transceiver devices and appear at both receiver outputs.

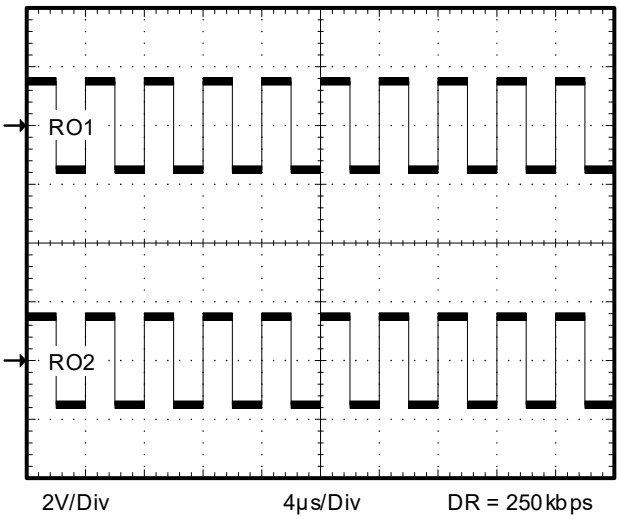

Figure 6. RO1 and RO2 before and after the EFT Test

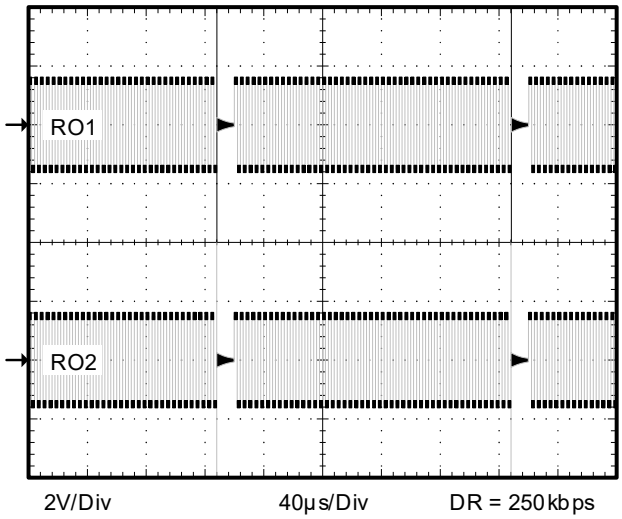

Figure 7. RO1 and RO2 during the EFT Test

The differential bus voltage during an EFT application is shown in Figure 8. *Note:* The applied transient is also observable at the driver input.

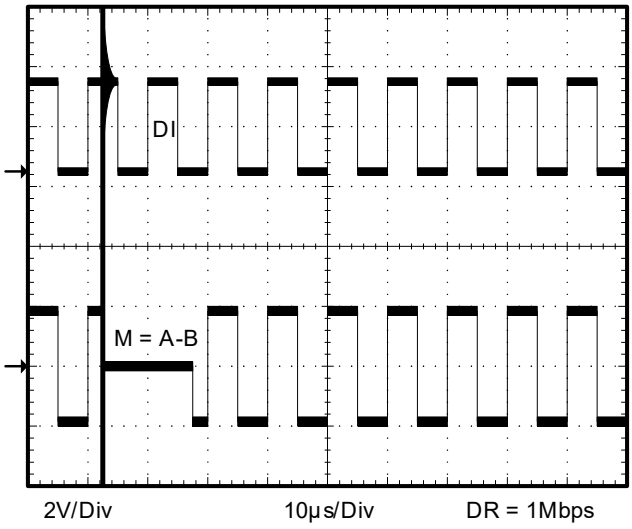

Figure 8. Data Input and Differential Bus Voltage during EFT Test

Figure 6 to Figure 8 show that the voltages on the logic control side of the transceivers can be significantly higher than the transceiver supply voltages if the transceivers are not sufficiently protected by transient voltage suppressors (TVS) and bypass capacitors.

4. EFT Test Datasheet

All transceivers were tested with positive and negative EFT transients. If latch-up occurred, the test voltage was reduced to the point where no latch-up occurred to determine the minimum pass-voltage. The devices were then tested on an automatic test system (ATE) for parametric performance. The pass criterion required that a device did not show any parametric shift. The results of the EFT and ATE tests have been recorded in the EFT Test Datasheet, shown in Figure 9.

TEST DATASHEET

Product Type	RAA78817x		
Date	08/19/2021		
Type of Test	EFT Immunity per IEC61000-4-4	**Recorded by**	Alan E.
Board Used / Equip.	Burst Period 300ms, Rep. Freq. = 5kHz/100kHz, Burst Length = 15ms/0.75ms		
Other special setup	DR = 250kbps, Test time = 60s		

Mode	Parameter	Half-Duplex Transceivers						Full-Duplex Transceivers					
	VCC = 3.3V	**RAA788172**		**RAA788175**		**RAA788178**		**RAA788170**		**RAA788173**		**RAA788176**	
	Rep. Freq. (kHz)	5	100	5	100	5	100	5	100	5	100	5	100
	Burst (ms)	15	0.75	15	0.75	15	0.75	15	0.75	15	0.75	15	0.75
	EFT (kV)												
TX	+5	OK	OK	OK	OK	OK	OK						
	-5	OK	OK	OK	OK	OK	OK						
RX	+5	OK	OK	OK	OK	OK	OK						
	-5	OK	OK	–	L	–	L						
	-4	–	–	–	L	–	OK						
	-3.9	–	–	–	L	–	–						
	-3.8	–	–	–	OK	–	–						
TX/RX	+5							–	OK	–	OK	–	OK
	-5							–	L	–	OK	–	L
	-4							–	L	–	OK	–	L
	-3.9							–	L	–		–	OK
	-3.8							–	L	–		–	OK
	-3.7							–	L	–		–	OK
	-3.6							–	L	–	OK	–	
	-3.5	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK
	ATE-Test	Pass		Pass		Pass		Pass		Pass		Pass	

* L = Latch-Up

* Rated EFT immunity is 500V below lowest EFT pass level

→ Rated EFT immunity for RAA78817xE family = 3.0kV

Figure 9. EFT Test Datasheet

5. Conclusion

The RAA78817x family of 3.3V RS-485 transceivers passed all EFT tests with 3.5kV test voltage. To account for temperature and humidity effects, the rated EFT immunity is specified with 500V below the lowest pass-level. Therefore, the rated EFT immunity for the RAA78817x family is 3.0kV, which places this transceiver family into the highest special test level category (level X) of the IEC61000-4-4 standard (Table 2).

Table 2. EFT Test Level Category for RAA78817x Transceivers

Test Level	Test Voltage (kV)	Repetition Frequency (kHz)	Components
1	0.25	5 or 100	RAA788170, RAA788172, RAA788173, RAA788175, RAA788176, RAA788178
2	0.5	5 or 100	
3	1	5 or 100	
4	2	5 or 100	
X	3	5 or 100	

Although the tested Renesas RS-485 transceivers possess high EFT immunity, the remaining components of a bus node design, such as UART, MCU, LDO, usually have less EFT immunity. As the transient immunity of a bus node is only as high as its weakest component, Renesas highly recommends protecting a bus node with external transient suppressor devices. The design, functional principle, and application of these devices in combination with Renesas transceivers is discussed and explained in the application notes listed in the reference section.

6. References

- AN1976: Important Transient Immunity Tests for RS-485 Networks
- AN1977: Transient Voltage Suppressors: Operation and Features
- AN1978: Surge Protection for Renesas' Standard RS-485 Transceivers
- AN1979: Surge Protection simplified with Renesas' Overvoltage Protected (OVP) Transceivers
- R15AN0002: RS-485 Transient Protection in Industrial DC-Supply Buses

7. Revision History

Revision	Date	Description
1.00	Aug 24, 2022	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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