R2A20133D

Application Note

R03AN0008EJ0300
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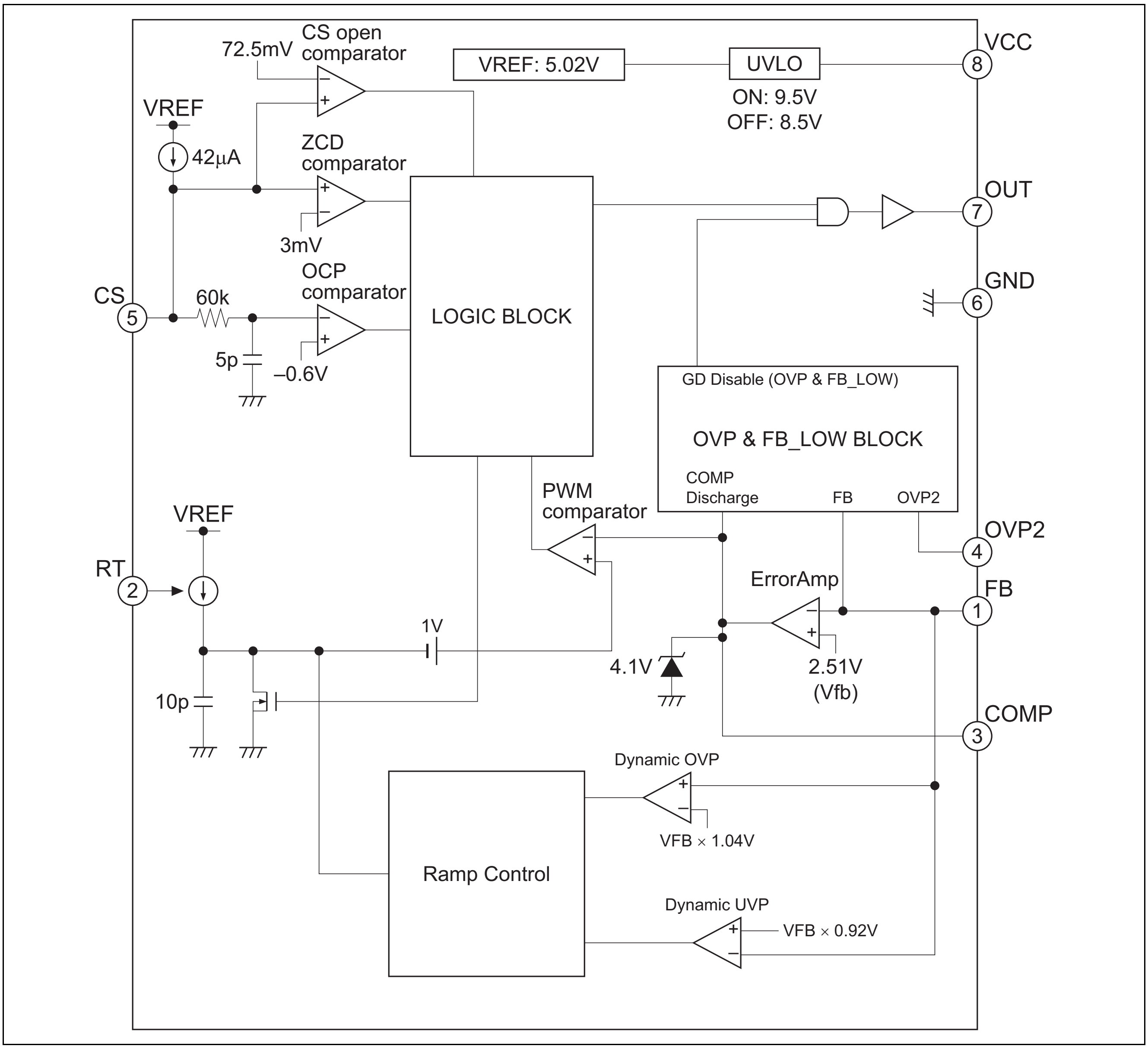
1. Outline

The R2A20133D is the active power factor correction controller that operates in the critical conduction mode (CRM).

The R2A20133D is the voltage mode CRM, such that the Power MOSFET controlled by this IC is turned on when the current of the boost inductor reaches zero and also controlled to keep ON time of the Power MOSFET constant. So, the peak current of the boost inductor follows the input voltage waveform.

The voltage mode CRM PFC controller does not need the input voltage sense line. So, the power loss of the system can be reduced.

2. Block Diagram



3. Descriptions of the R2A20133D Functional Blocks

3.1 Zero-Current Detection

The Zero-Current Detection (ZCD) detects the zero-current of the inductor, and the Power MOSFET is turned on at that time. After being converted from the GND-current to the voltage by the sensing resistor Rcs, the ZCD signal is supplied to the CS-pin.

The threshold voltage for ZCD is 3 mV (typ.). IC has the delay time (ZCD_delay), in which the drain voltage of the MOSFET decreases after the threshold voltage is detected. And ZCD_delay can be adjusted by RT pin resistor (R_{RT}).

Due to the offset of the zero-current, it is advised to tune the threshold voltage for ZCD to the negative side by using the bias current (Ics) in the CS pin and inputting the resistor for the filtering between Rcs and the CS-pin. (Example: 3 mV – 42 µA × 180 Ω = –4.56 mV)

Furthermore, as the threshold voltage of the ZCD is small, such as several mV, R2A20133D has the 0.2 µs mask function to prevent erroneous operations due to noises. By the 0.2 µs mask function, the output signal of the ZCD would be sent to the latter part, only when the zero current continues over the 0.2 µs mask period. The ZCD_delay time in figure 2 includes 0.2 µs of the mask function.

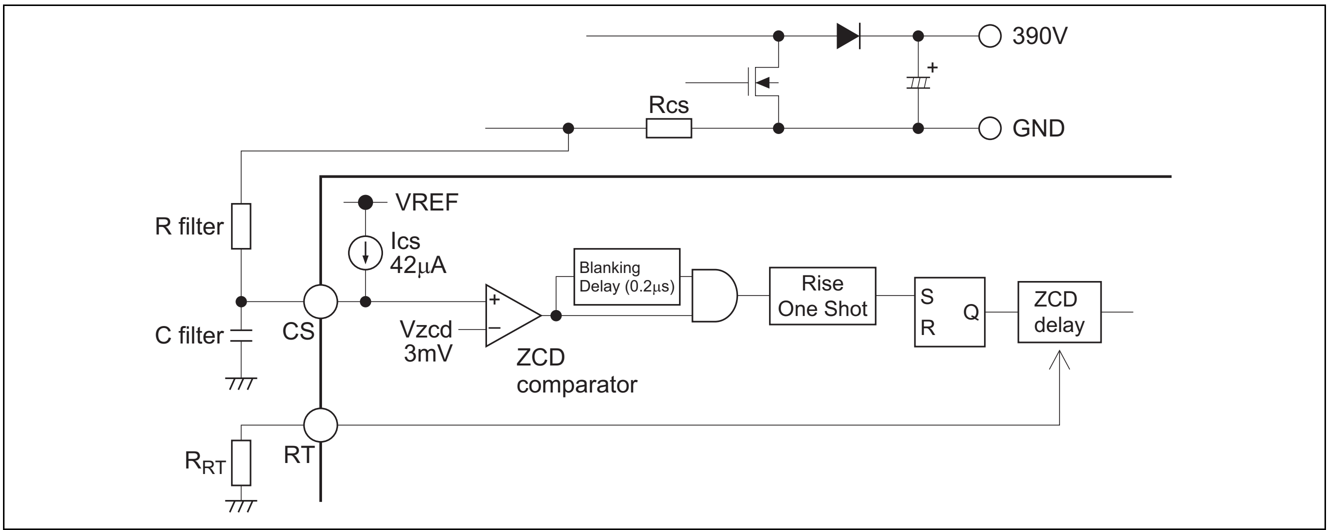


Figure 1

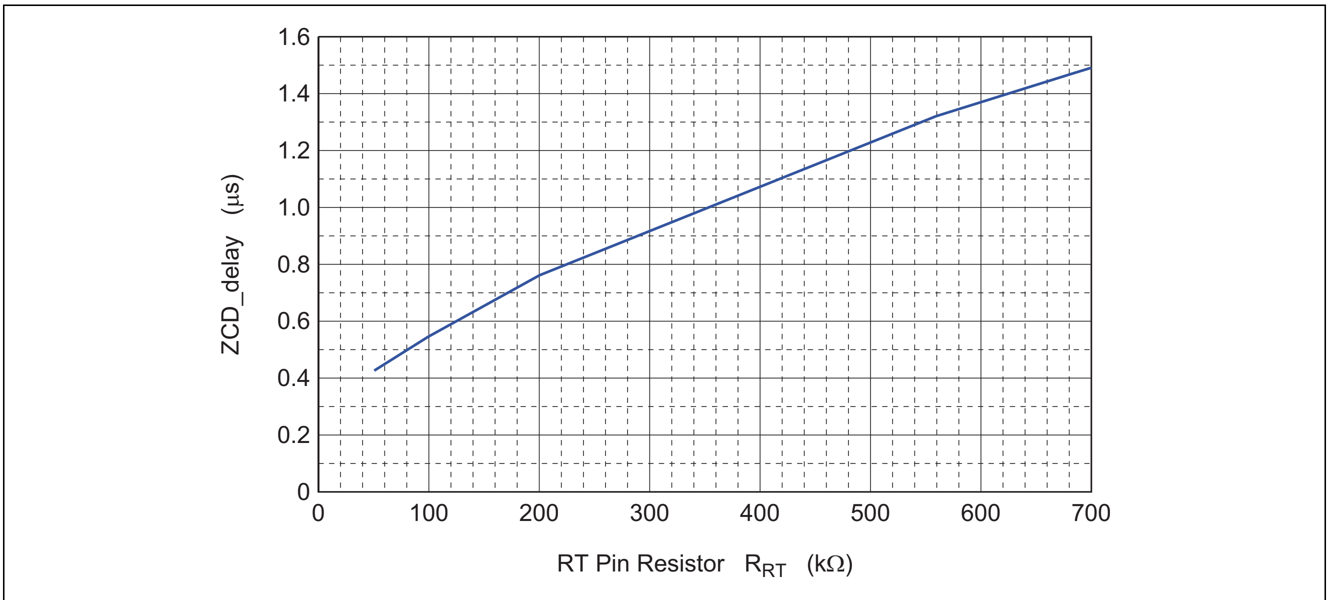


Figure 2 RT Pin Resistor vs. ZCD_dealy Time

3.2 Error Amplifier

The error amplifier of PFC control is a trance conductance amplifier.

The output current changes according to a voltage difference between FB pin voltage and the internal reference voltage.

COMP pin which is output of error amplifier is clamped by 4.1 V (typ).

3.3 RAMP Slope (IC-Internal)

The slope at point RAMP within the chip depends on the current determined by the external resistor R_{RT} on the RT pin and on-chip 10-pF capacitor.

The resistor R_{RT} is connected between the RT pin and the GND level.

The maximum ON time, tonmax, is determined when the output voltage of the error amplifier is 4.1 V (typ.). The RAMP circuit starts charging the RAMP capacitor when the ZCD circuit detects inductor zero current.

The RAMP circuit starts discharging the "RAMP portion" when the RAMP slope reaches COMP voltage.

And when the output voltage of the error amplifier is smaller than 1 V, the Power MOSFET ON time is zero, due to the built-in level shift voltage of 1 V.

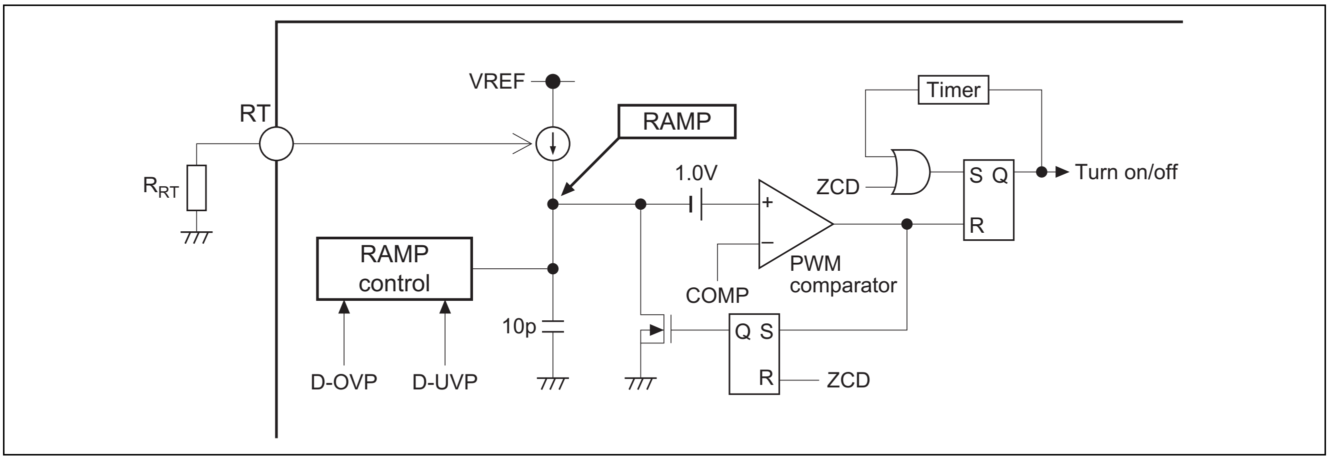


Figure 3

3.4 Output Stage

R2A20133D contains the single totem-pole output stage.

The drivability is +900 mA/–500 mA (peak). "+" means that the current flows into the IC.

Basically, direct driving of the power MOSFET is possible. However, please adjust drivability of the driver circuit on the board by selecting the appropriate parameters of the circuit according to the characteristics of the Power MOSFET to be used.

Due to zero-current switching, the speed of turning-off affects power loss more strongly than the speed of turning-on. The following figures show examples of driver circuits.

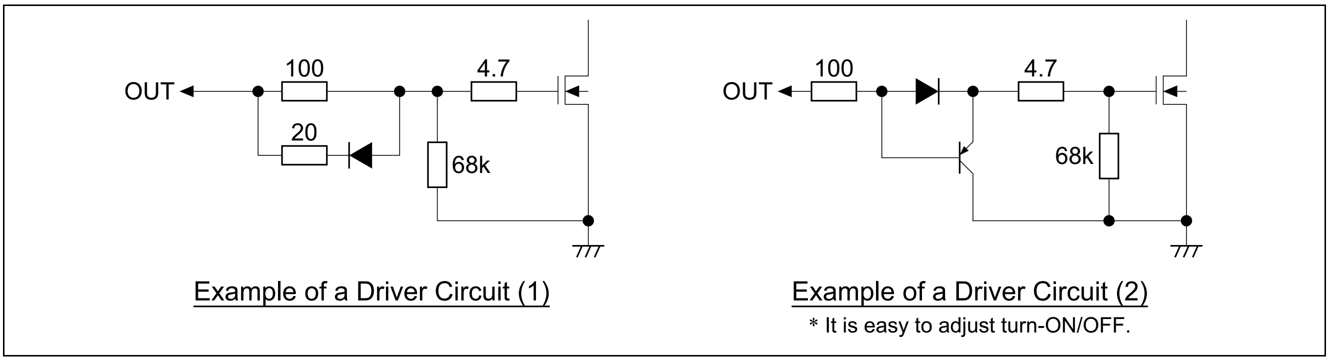


Figure 4

3.5 Protection

R2A20133D has the over voltage protection for PFC output voltage, feedback open loop protection, the over current protection, off time control function and so on.

[Protections at FB Pin]

3.5.1 Static Over Voltage Protection (S-OVP)

Static Over Voltage Protection stops an OUT signal when FB pin voltage reaches 1.09 × Vfb (2.51 V typ).
A Power MOSFET turns off quickly and S-OVP keeps stopping a GD signal till FB pin voltage reaches 1.09 × Vfb (2.51 V typ) – 100 mV.

3.5.2 Feedback Low Detection (FB-LOW)

The FeedBack LOW protection discharges COMP pin voltage during FB pin voltage is under 0.3 V.
Therefore a GD signal does not appears in this case.

3.5.3 Dynamic Over Voltage Function (D-OVP)

Dynamic Over Voltage Protection Function starts to decrease the On time of the MOSFET when FB pin voltage reaches 1.04 × Vfb (2.51 V typ).
The Power MOSFET ON time is decreased gradually, so that, the audio noise, that occurs when the current of inductor stops suddenly, can be avoided.

3.5.4 Dynamic Under Voltage Function (D-UVP)

When the voltage of the FP-pin is less than 0.92 × Vfb, R2A20133D starts to increase the On time of the MOSFET regardless of the COMP voltage. The maximum On time while D-UVP is working is twice as long as the On time at steady state.
This function is active when once the voltage of the FB-pin is more than 0.92 × Vfb after the IC starts.

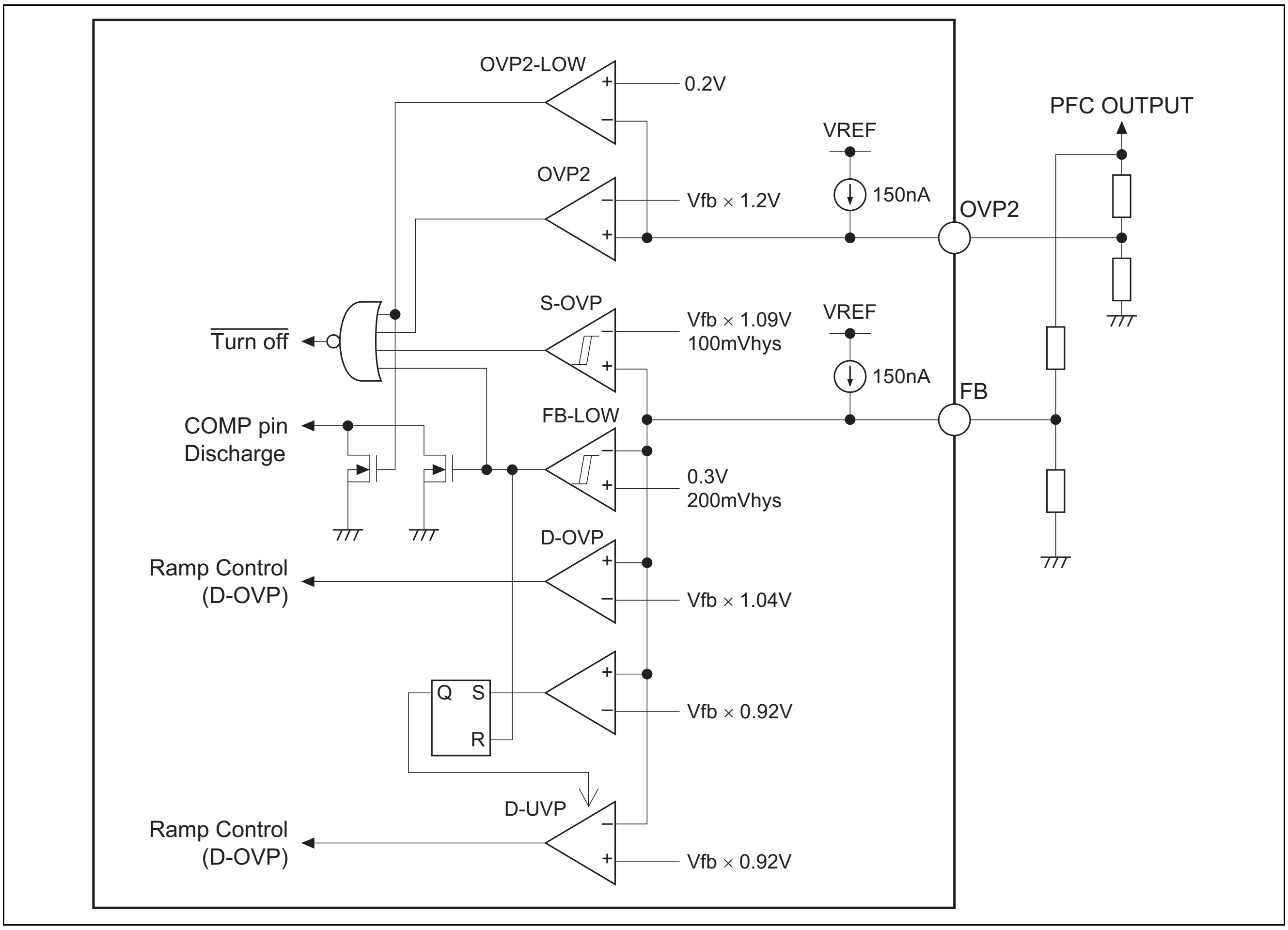


Figure 5

[Protections at OVP2 Pin]

3.5.5 Additional Over Voltage Protect Function (OVP2)

When OVP2 pin voltage reaches 1.2 × Vfb (Vfb = 2.51 V typ), a GD signal stops.
R2A20133D has an "auto recovery type" OVP function. A switching starts again when OVP2 pin voltage becomes under 1.2 × Vfb.

3.5.6 OVP2 Loop Low Detection (OVP2-Low)

When OVP2 pin voltage becomes under 0.2 V, a GD signal stops, and COMP voltage is discharged.

[Protections at CS Pin]

3.5.7 Over Current Protection (OCP)

This function defend Power MOSFET, boost inductor and boost Diode from over current.
OCP pin senses the each Power MOSFET source current by using an external sense resistor.
When OCP pin reaches –0.6V, an output is stopped with pulse-by-pulse.

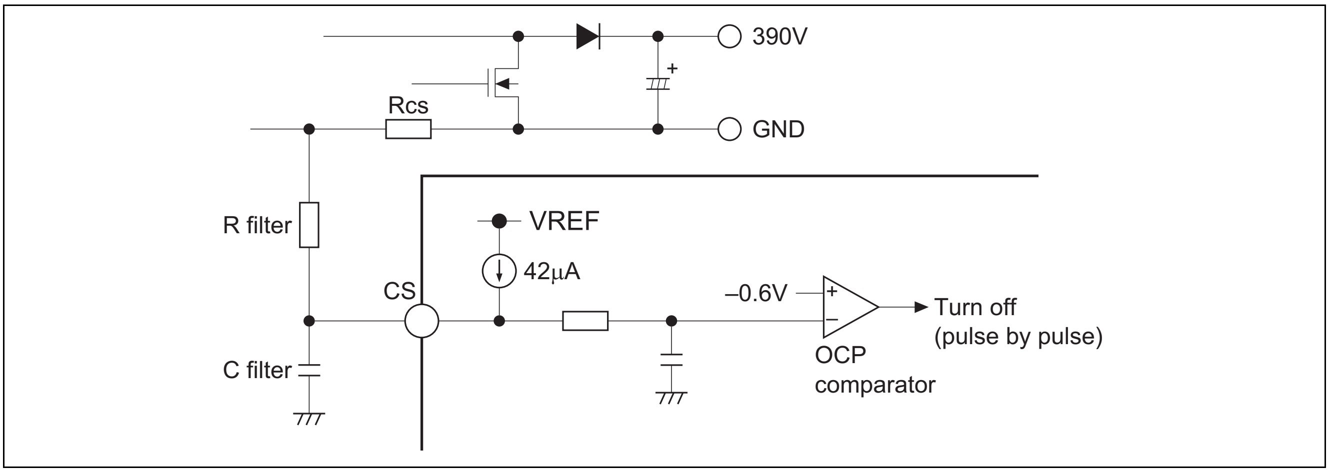


Figure 6

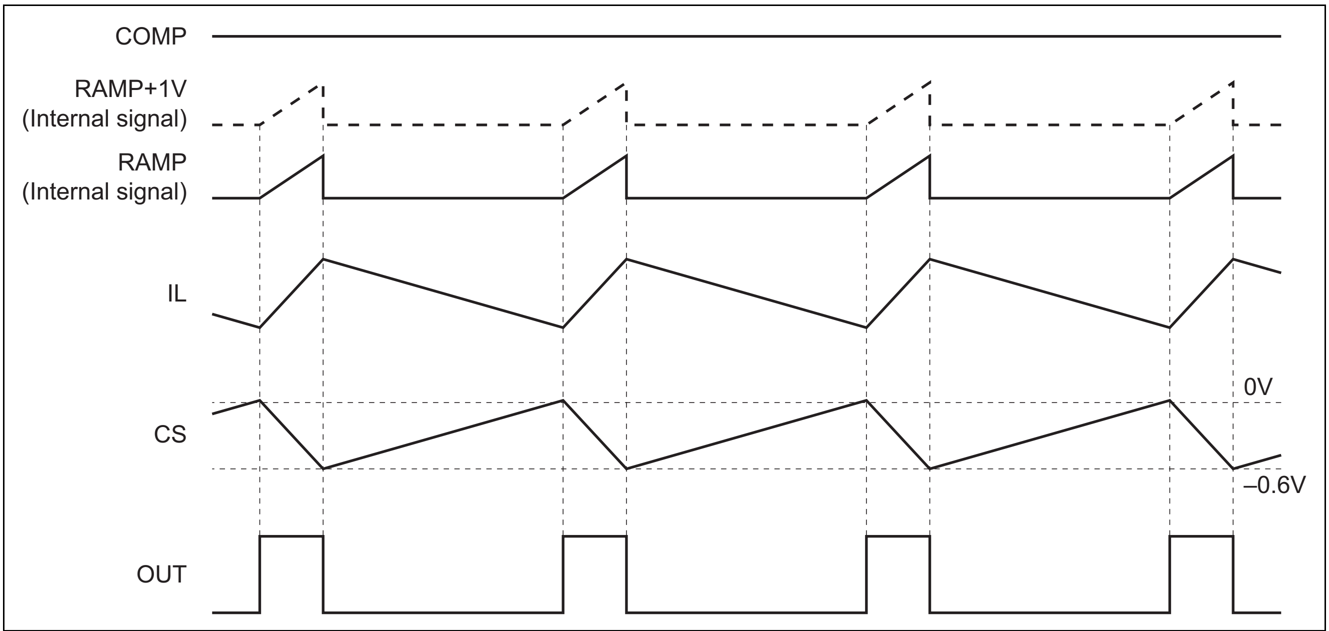


Figure 7 Waveform at the Over Current Detection

3.5.8 Switching Frequency Limiter

In CRM operation, the efficiency falls at the light load because the switching frequency becomes very high.
R2A20133D has the switching frequency limiter function so that it may not output the GD signal above a setting value.
The switching frequency is determined by the combination of below functions.

— ON Time Control

  There is time that R2A20133D does not output the GD signal even getting the ZCD signal after MOSFET turns on. Its period is 1.13 μs typ.

— ZCD detection delay time adjustable function

  As shown in section 3.1, R2A20133D has the ZCD_delay time after getting ZCD threshold voltage.
  It is possible to adjust an optimal value with the setting of R_{RT} value.

The limited maximum frequency is determined by the combination of the above functions.
Therefore limited maximum frequency can also be adjusted.

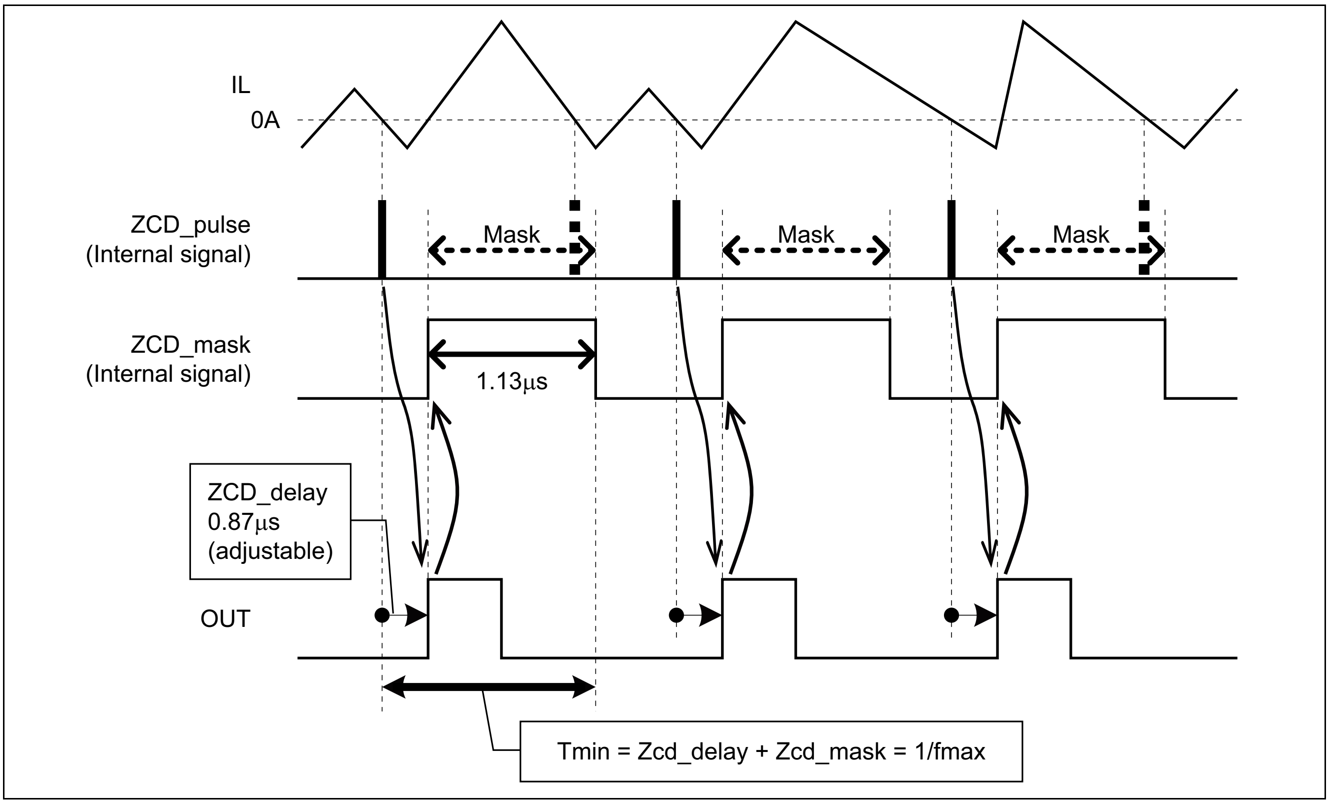


Figure 8 Waveform at Limited Maximum Switching Frequency Operation

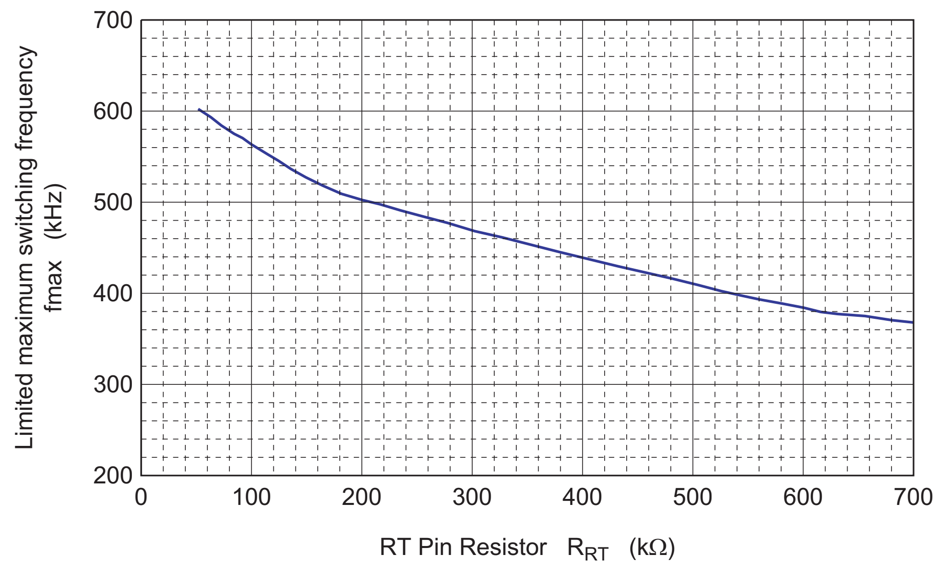


Figure 9 RT Pin Resistor vs. Limited Maximum Switching Frequency

3.5.9 Restriction Function at Restart Mode

Although R2A20133D contains the function which turns on the MOSFET forcedly when there is no ZCD signal in a certain period, 150 µs (typ.), the IC stops the Restart mode in order to prevent the high current from flowing into the MOSFET under the situations as follows:

(Example 1) The case when the inrush current flows into the output capacitor through the boost inductor at the instance of turning on the AC input voltage.

(Example 2) The case when the peaks of the AC input voltage rectified by the diode bridge are larger than the total voltage of the PFC output voltage and the forward voltage of the boost diode.

In both examples, because the currents continue to flow into the boost inductors, the voltage of the CS-pin is negative. Under these situations like two examples above, R2A20133D stops the Restart mode.

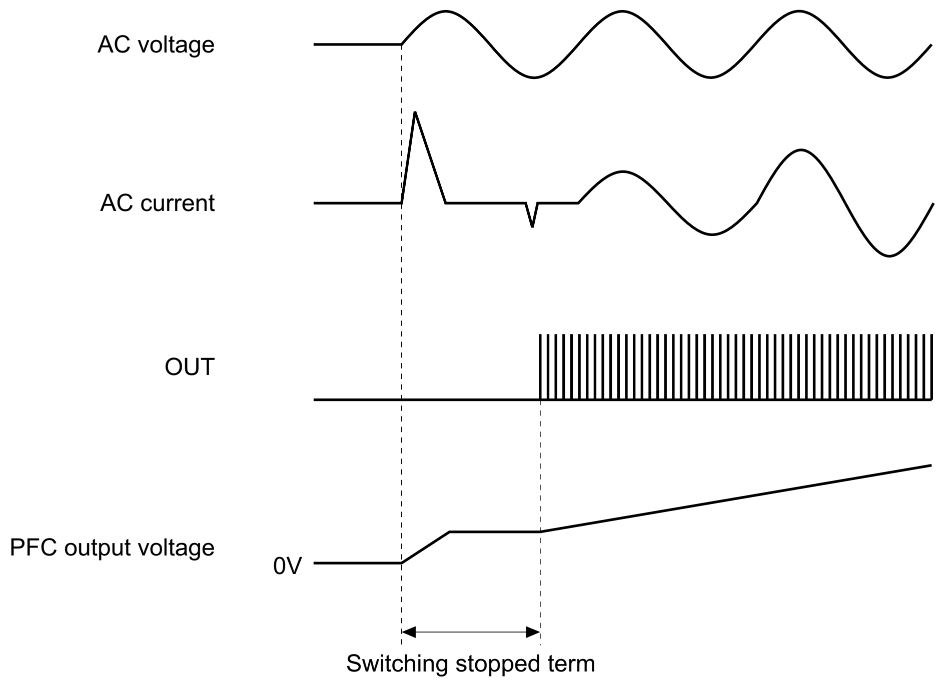


Figure 10 Example(1) Stop of the Switching Operation

3.6 PFC OFF

The operation of the PFC is stopped when the switch Q2 turns on and the COMP pin voltage becomes smaller than 1V (typ).

3.7 How to Stop OVP2 Function

If the OVP2 function is not used, the OVP2 pin should be connected to the RT pin.

4. Design Guide

4.1 Boost Inductor

It is necessary to set the inductance of boost inductor that a minimum switching frequency may not go into audio frequency. It is also possible to set a minimum switching frequency highly. However, the efficiency gets worse in that case. Thus, we don't recommend that it sets highly.
The minimum switching frequency must be higher than 20 kHz which is audio frequency to avoid audio noise of the inductor or the input capacitor. The frequency is generally set to the frequency higher than 50 kHz.
The boost inductor is obtained by Equation (1). Use the value around 0.9 as the conversion efficiency η.

$$f_{SW} = \frac{V_{AC}^2 \times (V_o - \sqrt{2} \times V_{AC}) \times \eta}{2 \times L \times V_o^2 \times I_{omax}} \quad \cdots (1)$$

f_{SW} [Hz]: Switching frequency
V_{AC} [V]: Effective value of AC input voltage
V_O [V]: PFC output voltage
I_{omax} [A]: Maximum output current
L [H]: Boost inductance

When the electric power is constant, the switching frequency depends on the AC input voltage range and the PFC output voltage.
Therefore an inductance of the boost inductor that satisfies a target minimum frequency is obtained by the Equation (2) and (3) which are transformed from the Equation (1).
The small value of the calculation result by the Equation (2) and (3) become as a minimum inductance value.
Use the value around 0.9 as the conversion efficiency η.

$$L_{ACLow}\,[H] = \frac{V_{ACLow}^2 \times (V_o - \sqrt{2} \times V_{ACLow}) \times \eta}{2 \times f_{SWLow} \times V_o^2 \times I_{omax}} \quad \cdots (2)$$

$$L_{ACHi}\,[H] = \frac{V_{ACHi}^2 \times (V_o - \sqrt{2} \times V_{ACHi}) \times \eta}{2 \times f_{SWLow} \times V_o^2 \times I_{omax}} \quad \cdots (3)$$

L_{ACLow}/L_{ACHi} [H]: Boost inductance
V_{ACLow} [V]: Effective value of minimum input voltage
V_{ACHi} [V]: Effective value of maximum input voltage
V_O [V]: PFC output voltage
I_{omax} [A]: Maximum output current
f_{SWLow} [Hz]: Minimum switching frequency

4.2 Output Capacitance

The capacitance of the output capacitor for arbitrary hold-up time is expressed in the next equation.

$$C_o\,[F] \geq \frac{2 \times P_o \times t_{hold}}{V_o^2 - V_{omin}} \quad \cdots (4)$$

t_{hold} [s]: Hold-up time
V_{omin} [V]: Minimum output voltage
P_O [W]: Maximum output power

4.3 Power MOS FET and Boost Diode

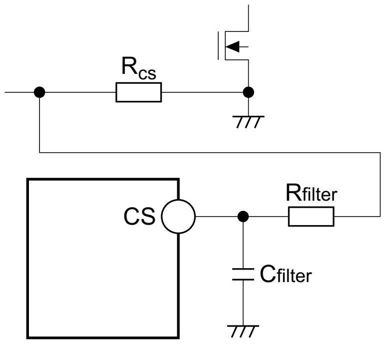
A peak current flowing on the Power MOSFET or the boost diode is expressed in the next equation. Use the value around 0.9 as the conversion efficiency η.

$$I_{Lpk}\ [\mathrm{A}] = \frac{2\sqrt{2} \times P_o}{V_{ACLow} \times \eta} \qquad \cdots (5)$$

4.4 Overcurrent-Detecting Resistor (Rcs)

Rcs is obtained by Equation (6). Use the value around 0.9 as the conduction loss η.
Rcs might be very small, so that care should be taken in the PCB pattern impedance.
And it is suggested that a CR filter of around 1 MHz is put on the OCP pin to avoid a switching noise.
Also, use the value of 1.2 as the current-limiting factor β to allow a margin of 20% in the normal value of ILpk.

$$R_{cs}\ [\Omega] = \frac{0.6 \times V_{ACLow} \times \eta}{2\sqrt{2} \times P_o \times \beta} \qquad \cdots (6)$$



Note: When Rcs becomes smaller, the voltage that is impressed to the terminal of CS becomes smaller. And then, it becomes easy for the restart operation to start at a high AC input voltage, and it causes the "sound bark", the audio noise of the inductor. This should be noted, when small value of Rcs is utilized to improve efficiency.
If you change the cutoff frequency of the filter, please set the resistance of Rfilter as a fixed value and adjust the capacitance of Cfilter. When the resistance of Rfilter is enlarged, it becomes easy for the restart operation to start.
If the setting of the OCP (over current protection) is smaller than ILpk, PFC output voltage falls by OCP function at maximum power.

4.5 The Resistance of RT

The ON time which is required at maximum output power at least (Ton_need) is obtained from the following equation. Use the value of around 0.9 as the conversion efficiency η.

$$T_{on\_need}\,[\mathrm{s}] = \frac{2 \times L \times P_o}{V_{ACLow}^{\,2} \times \eta} \qquad \cdots (7)$$

The maximum ON time (Ton_max) in which an output is possible is adjusted by resistance of RT pin (R_{RT}).
As shown in figure 11, please select the R_{RT} value which can be achieved over the calculated Ton_need by Equation (7).

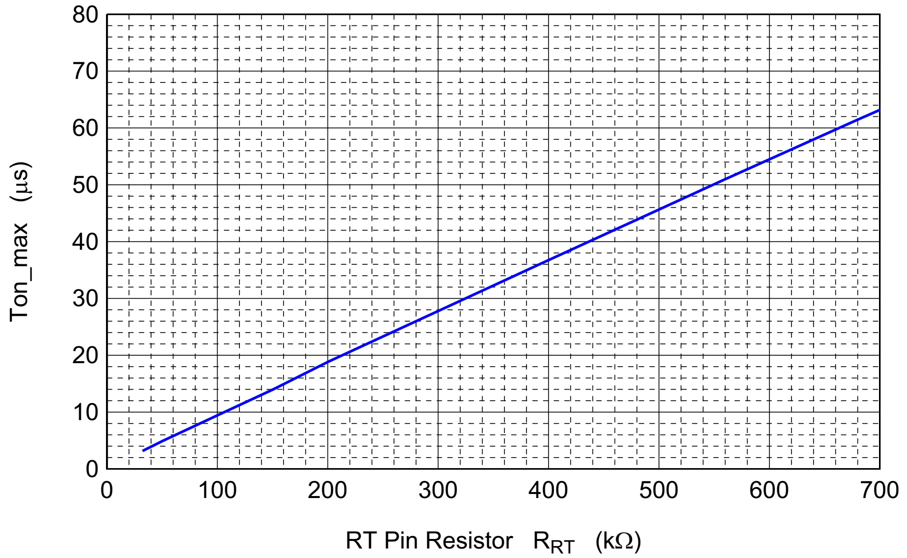
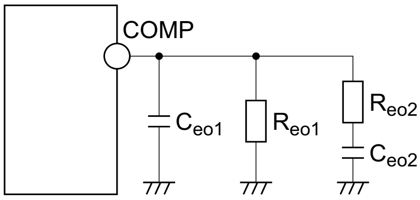


Figure 11 RT Pin Resistor (R_{RT}) vs. Ton_max

4.6 Frequency Characteristics of the Error Amplifier (gm Amplifier)

The error amplifier is a transconductance amplifier (gm amplifier). It does not need a feedback on input side. Therefore, it is possible to minimize influence on input circuit by a feedback circuit.
Gain of gm amplifier is calculated by product of transconductance and output impedance.
It is obtained by Equation (8), where Gm-v is tranceconductance of the gm amplifier and Rvo is an output resistor of the gm amplifier itself.
The overview of Gain-Frequency characteristics is shown in figure 12, in which the tendencies of the characteristics variation are illustrated when each parameter changes. The example of Frequency characteristics of the Error Amplifier is shown in figure 13.

$$G_V = G_{m-v} \times \frac{1}{\frac{1}{R_{vo}} + \frac{1}{R_{eo1}} + j\omega C_{eo1} + \frac{1}{R_{eo2} + \frac{1}{j\omega C_{eo2}}}} \quad \cdots (8)$$



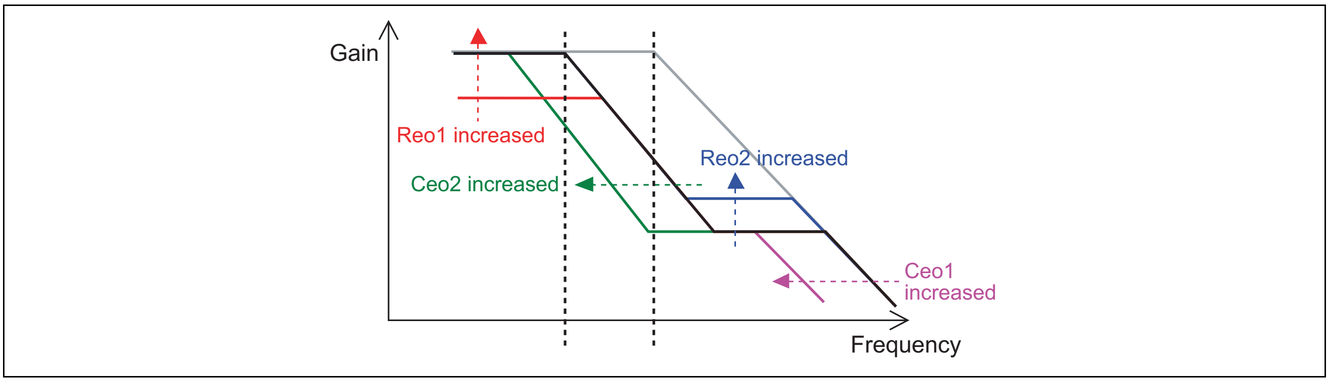


Figure 12 Overview of Gain–Frequency Characteristics

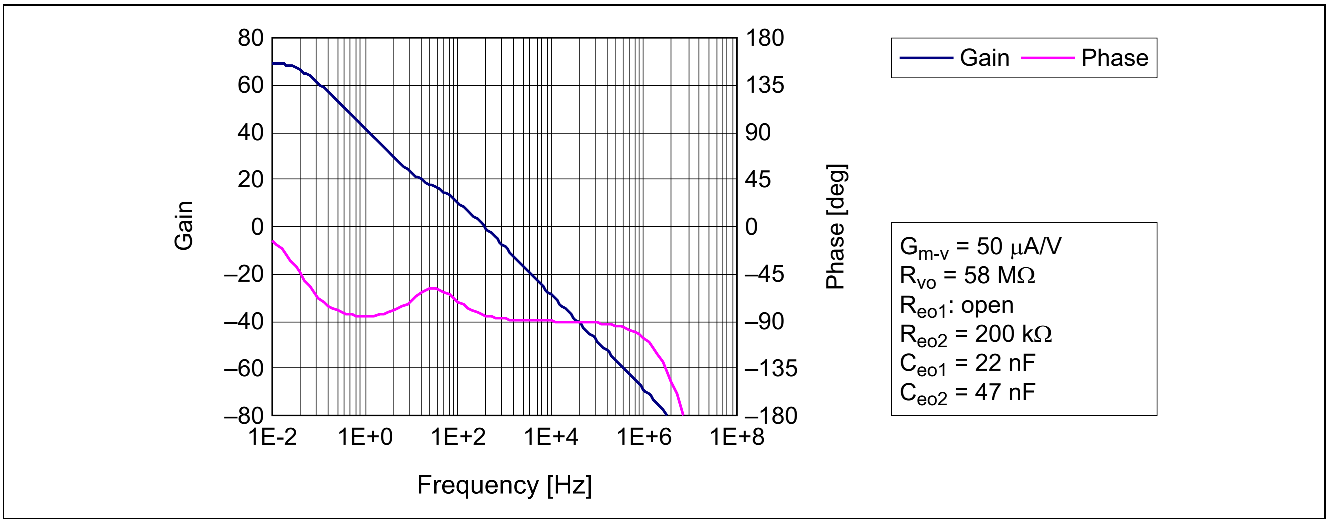


Figure 13 Frequency Characteristics of the Error Amplifier

5. Layout Pattern Guide

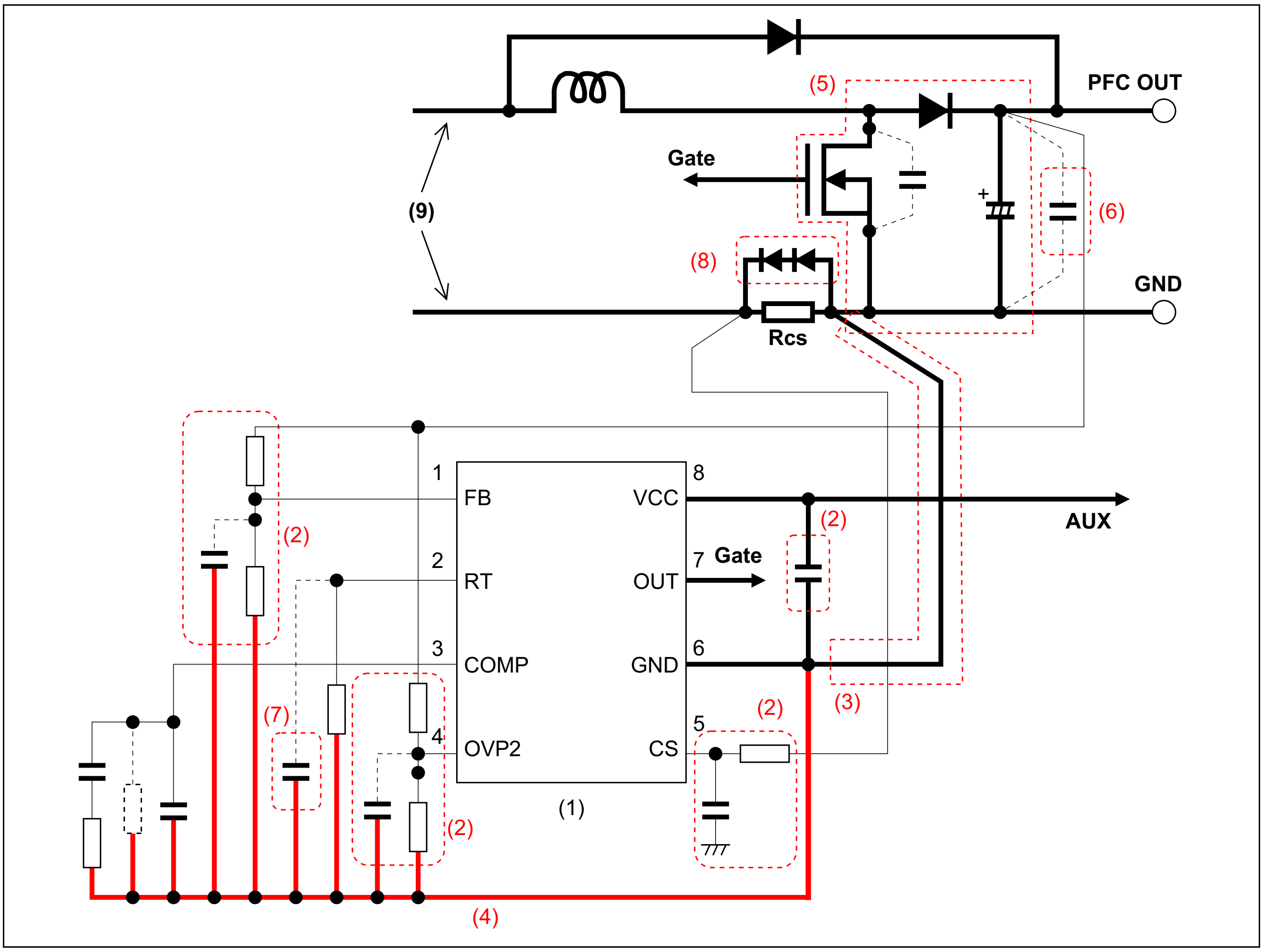


Figure 14

(1) Avoid switching noise by keeping the PFC IC as far as possible from high-voltage switching parts (power MOS FET, diode, and boost coil).
Take particular care to prevent noise radiation from the drain of the power MOSFET.

(2) To avoid the effects of radiated noise (to the extent this), place the filter on the CS pin, resistor on the FB and OVP2 line as close to the IC as possible.
Also place the bypass capacitors for VCC as close to the IC as possible.
When the large value of the resistance, such as over 1MΩ, is used in the FB and OVP2 line the capacitor about 1000 pF should be used between FP pin and GND.

(3) Wire the GND line of the IC with a single thick pattern to near the Rcs Resistor (Output side).

(4) Connect external components, the COMP, RT, FB and OVP2 pins to a common GND, and connect it to the GND pin of the IC with a single wiring.

(5) Keep pattern runs, on which current is discontinuous, as short as possible. In particular, it is effective to suppress overshooting of the drain voltage when the power MOSFET is turned off by ensuring a short distance between the drain and the anode of the boost diode.

(6) If a film capacitor is to be mounted to reduce switching ripple in the output voltage, insert it close to the diode. Use a film capacitor that has good high-frequency characteristics.

(7) Add a capacitor around 1000 pF between the RT pin and GND in case that the resistor value in RT pin is over 400 kΩ.

(8) Insert a cramp circuit (exp. diode x 2) close to the Rcs resistor to prevent over the CS pin maximum rating (–5 V) when inrush current happened such as start-up and power brownout.

(9) Avoid a pattern in which PFC power line and IC signal line become parallel and close.

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Revision Record

Rev.	Date	Description Page	Summary
1.00	Jan 17, 2012	—	First edition issued
2.00	Feb 07, 2012	P11	Replace the figure 11
3.00	Jul 05, 2013	P9	“4.1 Boost Inductor” is corrected

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