ISL73847x 4-Phase Design Example with Calculations

The purpose of this document is to provide an example of how to calculate supporting components for the ISL73847x 4-phase applications. This document also introduces an Excel design calculator that automatically calculates all these values.

Contents

1. 4-Phase Design

1.1 Initial Design Values

List out all the initial design values and any ISL73847x required parameters.

- V_{IN} = 5V
- V_{OUT} = 0.8V
- V_{REF} = 0.6V
- $I_{OUT(MAX)}$ = 100A
- n = 4 (number of phases)
- f_{SW} = 1000kHz
- A_{CSA} = 8mV/mV
- I_{STEP} = 50A
- $tran_{percent}$ = 2%
- $g_{m(EA)}$ = 4mA/V
- $DRP_{percent}$ = 4%
- I_{DROOP} = 19.9µA
- t_{SS} = 1ms
- I_{SS} = 10µA

1.2 Determining the Frequency Select Resistor

In this 4-phase calculation, use an external 1000kHz clock on SYNC-I. The datasheet recommends setting the internal oscillator to 85% of the external clock using the R_{FS} resistor so if the external clock stops, the converter continues running by switching to the ISL73847x internal oscillator. The 15% margin prevents the oscillator from switching randomly between the external and internal clock. The required internal clock is 85%×1000kHz = 850kHz.

Refer to the EC table in the datasheet for the recommended R_{FS} resistor values for 250kHz, 500kHz, 1MHz, and 1.5MHz switching frequencies, as these are tested. Use Equation 1 for other frequencies to calculate R_{FS} with less than 10%.

(EQ. 1) $$R_{FS}[k\Omega] = \left(\frac{56497}{f_{SW}[kHz]}\right) - 20.96$$

$$R_{FS} = \left(\frac{56497}{850}\right) - 20.96$$

$$\therefore R_{FS} = 45.51k\Omega$$

The equation suggests using a 45.51kΩ R_{FS} resistor. A good option is 43.2kΩ which would provide more margin..

1.3 Determining the Output Voltage Feedback Resistors

The required output voltage is 0.8V, the internal voltage reference is 0.6V typical, and as a starting point Renesas suggests making R_1 4.99kΩ.

(EQ. 2)

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_2}{R_1}\right)$$

Rearrange the equation:

(EQ. 3)

$$R_2 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_1$$

$$R_2 = \left(\frac{0.8}{0.6} - 1\right) \times 4.99k\Omega$$

$$\therefore R_2 = 1.663k\Omega$$

A good option for R_2 is a 1.67kΩ resistor with ±0.1% tolerance. Calculating the output voltage with this value gives an output voltage of 0.801V.

1.4 Determining the Current-Sense Resistor

The target current-sense amplifier input voltage is 50mV, maximum output current is 100A, the number of phases is four, and the OCP1 sense voltage is 75mV.

(EQ. 4)

$$R_{SEN}[\Omega] = \frac{V_{SEN}[V] \times n}{I_{OUT(MAX)}[A]}$$

$$R_{SEN} = \frac{50 \times 10^{-3} \times 4}{100}$$

$$\therefore R_{SEN} = 2m\Omega$$

(EQ. 5)

$$P_{RSEN}[W] = \frac{V_{OCP1}[V]^2}{R_{SEN}[\Omega]}$$

$$P_{RSEN} = \frac{(75 \times 10^{-3})^2}{2 \times 10^{-3}}$$

$$\therefore P_{RSEN} = 2.813W$$

1.5 Determining the Output Inductor

Use Equation 6 to calculate a good estimate for the output inductor based on a required ripple current, where $I_{OUT} = n \times I_{PHASE}$.

(EQ. 6)

$$L_{REC}[H] = \frac{(V_{IN} - V_{OUT})[V] \times D \times n}{k \times f_{SW}[Hz] \times I_{OUT(MAX)}[A]}$$

The input voltage is 5V, the calculated output voltage is 0.801V, the duty cycle is D = 0.8V/5V = 0.16, the output switching frequency is 1000kHz, the number of phases is 4, the required ripple current (k) is 30% and the max output current is 100A (4x25A).

$$\therefore L_{REC} = \frac{(5 - 0.801) \times 0.16 \times 4}{0.3 \times (1000 \times 10^3) \times 100} = 89.6\text{nH}$$

An available option for the inductor is L_{SEL} = 100nH. Use Equation 7 to calculate the actual inductor ripple percentage for the chosen inductor.

(EQ. 7)

$$\text{ripple}[\%] = \frac{(V_{IN} - V_{OUT})[V] \times D \times n}{f_{SW}[Hz] \times I_{OUT(MAX)}[A] \times L_{SEL}[H]}$$

$$\therefore \text{ripple} = \frac{(5 - 0.801) \times 0.16 \times 4}{(1000 \times 10^3) \times 100 \times (100 \times 10^{-9})} = 26.9\%$$

1.6 Determining the Current-Sense Filter

The current-sense ISEN signal must be filtered before going to the ISL73847x ISENx pins to eliminate high-frequency switching noise and extract the current signal information. In addition, the parasitic ESL of the current-sense resistor creates an inductive divider with the output inductor and adds a square wave component to the current-sense signal, which could prematurely trip overcurrent. To fix this issue, an RC filter must be placed across the ISENx traces and as close as possible to the ISL73847x device. Use Equation 12 to calculate the zero formed by the R_{SENSE} parasitic ESL and L_{OUT}. R_{SENSE} is the current-sense resistance of 2mΩ, V_{IN} is the buck input voltage of 5V, L_{OUT} is the output inductor of 220nH, and V_{ESL} is the voltage amplitude of the parasitic square wave component created by the parasitic inductance of the R_{SENSE} and L_{OUT}, which is 50mV. V_{ESL} is determined by the specific components used on the board and can be measured with oscilloscope captures of the current-sense signal without filtering.

(EQ. 8)

$$f_{ZERO}[Hz] = \frac{R_{SENSE}[\Omega] \times V_{IN}}{2\pi \times L_{OUT}[H] \times V_{ESL}}$$

(EQ. 9)

$$f_{ZERO}[Hz] = \frac{(2 \times 10^{-3}) \times 5V}{2\pi \times (220 \times 10^{-9}) \times (50 \times 10^{-3})} = 144.69\text{kHz}$$

For the ISL73847x, a bit of the ESL square-wave signal must be left to achieve short T_{ON} because the bandwidth of the current-sense amplifier itself creates filtering of the current-sense signal. Therefore, to achieve a triangular signal at the PWM input, the user must relax filtering on the CSA input. Use Equation 10 to calculate the filter resistor, so the corner-frequency of the RC filter is seven times higher than the ESL zero, where C_F is the filter capacitor of 680pF.

(EQ. 10)

$$R_F[\Omega] = \frac{1}{2\pi \times 7 \times f_{ZERO} \times C_F}$$

(EQ. 11)

$$R_F[\Omega] = \frac{1}{2\pi \times 7 \times (144.69 \times 10^3) \times (680 \times 10^{-12})} = 231\Omega$$

For the full possible range of VIN on the ISL73847x buck supply, an R_F of 30.1Ω and C_F of 680pF are good choices for the RC filter.

1.7 Determining the Slope Compensation Resistor

Use Equation 12 to calculate the slope compensation resistor. R_{SEN} is 2mΩ, R_{FS} is 43.2kΩ, V_{OUT} is 0.801V, k is 25kV/s, L_{SEL} is 100nH.

(EQ. 12) $$R_{SLOPE}[\Omega] = \frac{R_{SEN}[\Omega] \times R_{FS}[\Omega] \times V_{OUT}[V]}{k \times L_{SEL}}$$

$$\therefore R_{SLOPE} = \frac{(2 \times 10^{-3}) \times (43.2 \times 10^{3}) \times 0.801}{(25 \times 10^{3}) \times (100 \times 100^{-9})} = 27.683\text{k}\Omega$$

The equation gives a 27.683kΩ R_{SLOPE} value, which is between 25kΩ and 100kΩ. A good option is 30.1kΩ.

1.8 Determining the Error-Amplifier Compensation Resistor

To calculate the output capacitor and compensation values, ΔV_{OUT} and ΔI_{OUT} must be known. ΔV_{OUT} is the amount of output voltage deviation during a load step, in this example it is 2%×0.801V = 16mV, and ΔI_{OUT} is the load step which is 50A. With these two known values, use Equation 13 to calculate the equivalent load-line output impedance R_{LL}.

(EQ. 13) $$R_{LL} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}}$$

$$\therefore R_{LL} = \frac{16 \times 10^{-3}}{50} = 0.32\text{m}\Omega$$

With the load-line impedance, use Equation 14 to calculate RCOMP, where V_{OUT} is 0.801V, R_{SEN} is 2mΩ, A_{CSA} is 8mV/mV, n is 4, V_{REF} is 0.6V, $g_{m(EA)}$ is 4mS, and R_{LL} is 0.32mΩ.

(EQ. 14) $$R_{COMP} = \frac{V_{OUT}[V] \times R_{SEN}[\Omega] \times A_{CSA}[mV/mV]}{n \times V_{REF}[V] \times g_{m(EA)}[A/V] \times R_{LL}[\Omega]}$$

(EQ. 15) $$R_{COMP} = \frac{0.801 \times (2 \times 10^{-3}) \times 8}{4 \times 0.6 \times (4 \times 10^{-3}) \times (0.32 \times 10^{-3})} = 4.171\text{k}\Omega$$

A good compensation resistor is a 4.22kΩ.

1.9 Determining the Output Capacitance

Use Equation 16 to determine the minimum output capacitance. The compensation resistor is 4.22kΩ, the error amplifier transconductance is 4mA/V or 4mS, the internal voltage reference is 0.6V, f_T is the converter unity-gain frequency, which Renesas recommends setting a decade below the switching frequency ($f_T = f_{SW}/10 = 1000kHz/10 = 100kHz$), A_{CSA} is 8mV/mV, and the calculated output voltage is 0.801V.

(EQ. 16) $$C_{OUT(MIN)} = \frac{n \times R_{COMP}[\Omega] \times g_{m(EA)}[V/A] \times V_{REF}[V]}{2\pi \times f_T[Hz] \times A_{CSA}[mV/mV] \times R_{SEN}[\Omega] \times V_{OUT}[V]}$$

$$\therefore C_{OUT(MIN)} = \frac{4 \times (4.22 \times 10^3) \times (4 \times 10^{-3}) \times 0.6}{2\pi \times (100 \times 10^3) \times 8 \times (2 \times 10^{-3}) \times 0.801} = 5031\mu F$$

A good option is paralleling twenty-four 220µF capacitors, or twelve per phase, which gives 5280µF of bulk output capacitance.

With the actual output capacitor value chosen, recalculate f_T by rearranging Equation 16 to create Equation 17.

(EQ. 17) $$f_T[Hz] = \frac{n \times R_{COMP}[\Omega] \times g_{m(EA)}[V/A] \times V_{REF}[V]}{2\pi \times C_{OUT}[F] \times A_{CSA}[mV/mV] \times R_{SEN}[\Omega] \times V_{OUT}[V]}$$

$$\therefore f_T[Hz] = \frac{4 \times (4.22 \times 10^3) \times (4 \times 10^{-3}) \times 0.6}{2\pi \times (5280 \times 10^{-6}) \times 8 \times (2 \times 10^{-3}) \times 0.801} = 95.28kHz$$

1.10 Determining the Error-Amplifier Compensation Capacitor

Use Equation 18 to determine the error-amplifier compensation capacitor. f_Z is the zero frequency of the error amplifier. Renesas recommends setting the zero formed by R_{COMP} and C_{COMP} a decade smaller than the f_T ($f_Z = f_T/10 = 95.28kHz/10 = 9.528kHz$), where R_{COMP} is 4.22kΩ.

(EQ. 18) $$C_{COMP}[F] = \frac{1}{2\pi \times f_Z[Hz] \times R_{COMP}[\Omega]}$$

$$\therefore C_{COMP} = \frac{1}{2\pi \times (9.528 \times 10^3) \times (4.22 \times 10^3)} = 3.96nF$$

A good option for the compensation capacitor is 3.9nF.

1.11 Determining the Pole Capacitor

Adding a pole capacitor is recommended to cancel out the zero formed by the equivalent bulk output capacitance and ESR. To determine the pole capacitor, first determine the equivalent total ESR of the parallel combination of output capacitors. The 220µF output capacitors chosen have 6mΩ of ESR individually, so the parallel combination of twenty-four of these output capacitors have an equivalent total ESR of 6mΩ/24 = 0.250mΩ, as shown in Equation 19.

Note: This equation and the ones that follow apply only if all capacitors in parallel are identical with equal capacitance and ESR values.

(EQ. 19) $$ESR_{TOTAL}[\Omega] = \frac{ESR[\Omega]}{\#\text{ of capacitors}}$$

$$\therefore ESR_{TOTAL} = \frac{6 \times 10^{-3}}{24} = 0.250m\Omega$$

Lastly, add a pole to the controller loop at the same frequency as the zero formed by the equivalent C_{OUT} and ESR, using Equation 20.

(EQ. 20) $$C_{POLE}[F] = \frac{C_{OUT}[F] \times ESR[\Omega]}{R_{COMP}[\Omega]}$$

$$\therefore C_{POLE} = \frac{(5280 \times 10^{-6}) \times (0.25 \times 10^{-3})}{4.22 \times 10^{3}} = 313pF$$

A good option for the pole capacitor is 330pF.

1.12 Determining the Droop Regulation Resistor and Capacitor

Use Equation 21 to determine the droop resistor. The required percentage of droop regulation at full load is 4%, the internal voltage reference is 0.6V, the droop current at full-load is 19.9µA, the number of phases for this design is 4, and two ISL73847x Controllers.

(EQ. 21) $$R_{DROOP}[\Omega] = \frac{DRP_{percent} \times V_{REF}[V]}{I_{DROOP}[\mu A] \times n} \times \#\text{ of Controllers}$$

$$\therefore R_{DROOP} = \frac{4\% \times 0.6}{(19.9 \times 10^{-6}) \times 4} \times 2 = 603\Omega$$

A good option for R_{DROOP} is 604Ω. Use Equation 22 to determine the droop capacitor. The compensation resistor is 4.22kΩ, and the compensation capacitor is 4.3nF.

(EQ. 22) $$C_{DROOP}[F] = \frac{R_{COMP}[\Omega] \times C_{COMP}[F]}{R_{DROOP}[\Omega]}$$

$$\therefore C_{DROOP} = \frac{4.22 \times 10^{3} \times 3.9 \times 10^{-9}}{604} = 27.25nF$$

A good option for C_{DROOP} is 27nF.

1.13 Determining the Soft-Start Capacitor and In-Rush Current

Use Equation 23 to determine the soft-start capacitor. The required soft-start time is 1ms, the soft-start current is 10µA and the voltage reference is 0.6V.

(EQ. 23) $$C_{SS}[F] = \frac{t_{SS}[s] \times I_{SS}[A]}{V_{REF}[V]}$$

$$\therefore C_{SS} = \frac{0.001 \times (10 \times 10^{-6})}{0.6} = 16.78\text{nF}$$

A good option for C_{SS} is 22nF.

Use Equation 23 to calculate the expected soft-start time with this C_{SS} value.

(EQ. 24) $$t_{SS}[s] = \frac{(22 \times 10^{-9}) \times 0.6}{10 \times 10^{-6}}$$

$$\therefore t_{SS} = 1.32\text{ms}$$

Use Equation 25 to calculate the in-rush current. The output capacitance is 5280µF, the calculated output voltage is 0.801V, and the duty cycle is 0.16.

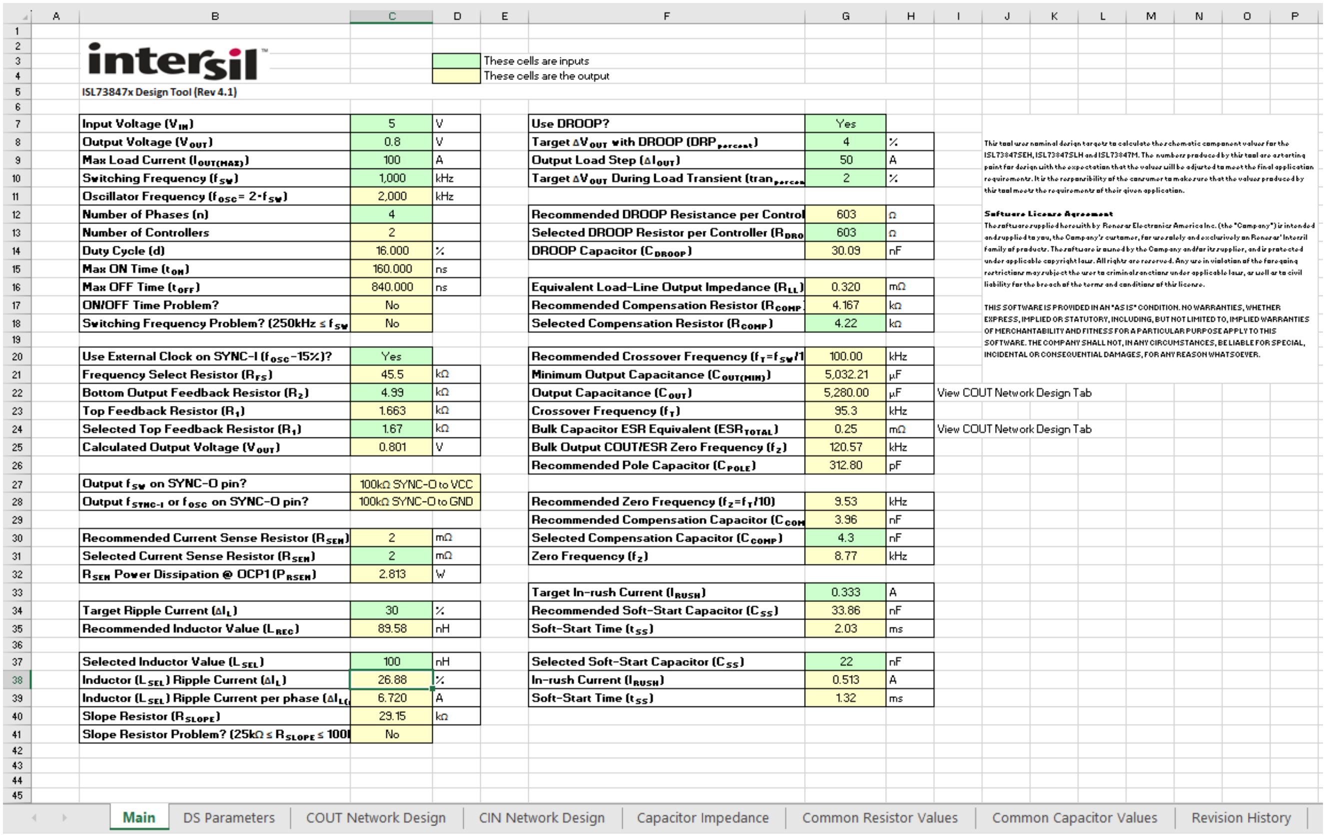
(EQ. 25) $$I_{RUSH}[A] = \frac{D \times V_{OUT}[V] \times C_{OUT}[F]}{t_{SS}[s]}$$

$$\therefore I_{RUSH}[A] = \frac{0.16 \times 0.801 \times 5280 \times 10^{-6}}{0.00132} = 0.513\text{A}$$

1.14 Summary of all the Calculated Component Values

- R_{FS} = 45.5kΩ ≈ 43.2kΩ
- R_1 = 1.66kΩ ≈ 1.67kΩ, with ±0.1% tolerance
- R_2 = 4.99kΩ
- V_{OUT} = 0.801V
- R_{SEN} = 2mΩ
- R_{FIL} = 30.1Ω
- C_{FIL} = 680pF
- L_{OUT} = 100nH/phase
- R_{SLOPE} = 29.15kΩ ≈ 30.1kΩ
- R_{COMP} = 4.17kΩ ≈ 4.22kΩ
- C_{OUT} = 220µF×24 = 5280µF (2640µF/phase)
- C_{COMP} = 3.96nF ≈ 3.9nF
- R_{DROOP} = 603Ω ≈ 604Ω
- C_{DROOP} = 27nF
- C_{SS} = 17nF ≈ 22nF
- C_{POLE} = 330pF

Figure 1 shows an image of the ISL73847x Design Tool (Excel file) that automatically calculates all of these values for the 4-phase application design.



ISL73847x Design Tool (Rev 4.1)

These cells are inputs
These cells are the output

7	Input Voltage (V_{IN})	5	V
8	Output Voltage (V_{OUT})	0.8	V
9	Max Load Current ($I_{OUT(MAX)}$)	100	A
10	Switching Frequency (f_{SW})	1,000	kHz
11	Oscillator Frequency (f_{OSC}= 2·f_{SW})	2,000	kHz
12	Number of Phases (n)	4	
13	Number of Controllers	2	
14	Duty Cycle (d)	16.000	%
15	Max ON Time (t_{ON})	160.000	ns
16	Max OFF Time (t_{OFF})	840.000	ns
17	ON/OFF Time Problem?	No	
18	Switching Frequency Problem? (250kHz ≤ f_{SW}	No	
20	Use External Clock on SYNC-I (f_{OSC}-15%)?	Yes	
21	Frequency Select Resistor (R_{FS})	45.5	kΩ
22	Bottom Output Feedback Resistor (R_2)	4.99	kΩ
23	Top Feedback Resistor (R_1)	1.663	kΩ
24	Selected Top Feedback Resistor (R_1)	1.67	kΩ
25	Calculated Output Voltage (V_{OUT})	0.801	V
27	Output f_{SW} on SYNC-O pin?	100kΩ SYNC-O to VCC	
28	Output f_{SYNC-I} or f_{OSC} on SYNC-O pin?	100kΩ SYNC-O to GND	
30	Recommended Current Sense Resistor (R_{SEN})	2	mΩ
31	Selected Current Sense Resistor (R_{SEN})	2	mΩ
32	R_{SEN} Power Dissipation @ OCP1 (P_{RSEN})	2.813	W
34	Target Ripple Current (ΔI_L)	30	%
35	Recommended Inductor Value (L_{REC})	89.58	nH
37	Selected Inductor Value (L_{SEL})	100	nH
38	Inductor (L_{SEL}) Ripple Current (ΔI_L)	26.88	%
39	Inductor (L_{SEL}) Ripple Current per phase ($\Delta I_{L(}$	6.720	A
40	Slope Resistor (R_{SLOPE})	29.15	kΩ
41	Slope Resistor Problem? (25kΩ ≤ R_{SLOPE} ≤ 100	No	

7	Use DROOP?	Yes		
8	Target ΔV_{OUT} with DROOP ($DRP_{percent}$)	4	%	
9	Output Load Step (ΔI_{OUT})	50	A	
10	Target ΔV_{OUT} During Load Transient ($tran_{percen}$	2	%	
12	Recommended DROOP Resistance per Control	603	Ω	
13	Selected DROOP Resistor per Controller (R_{DRO}	603	Ω	
14	DROOP Capacitor (C_{DROOP})	30.09	nF	
16	Equivalent Load-Line Output Impedance (R_{LL})	0.320	mΩ	
17	Recommended Compensation Resistor (R_{COMP}	4.167	kΩ	
18	Selected Compensation Resistor (R_{COMP})	4.22	kΩ	
20	Recommended Crossover Frequency (f_T=f_{SW}/1	100.00	kHz	
21	Minimum Output Capacitance ($C_{OUT(MIN)}$)	5,032.21	µF	
22	Output Capacitance (C_{OUT})	5,280.00	µF	View COUT Network Design Tab
23	Crossover Frequency (f_T)	95.3	kHz	
24	Bulk Capacitor ESR Equivalent (ESR_{TOTAL})	0.25	mΩ	View COUT Network Design Tab
25	Bulk Output COUT/ESR Zero Frequency (f_Z)	120.57	kHz	
26	Recommended Pole Capacitor (C_{POLE})	312.80	pF	
28	Recommended Zero Frequency (f_Z=f_T/10)	9.53	kHz	
29	Recommended Compensation Capacitor (C_{COM}	3.96	nF	
30	Selected Compensation Capacitor (C_{COMP})	4.3	nF	
31	Zero Frequency (f_Z)	8.77	kHz	
33	Target In-rush Current (I_{RUSH})	0.333	A	
34	Recommended Soft-Start Capacitor (C_{SS})	33.86	nF	
35	Soft-Start Time (t_{SS})	2.03	ms	
37	Selected Soft-Start Capacitor (C_{SS})	22	nF	
38	In-rush Current (I_{RUSH})	0.513	A	
39	Soft-Start Time (t_{SS})	1.32	ms	

Main | DS Parameters | COUT Network Design | CIN Network Design | Capacitor Impedance | Common Resistor Values | Common Capacitor Values | Revision History

Figure 1. Automatic Design Results for a 4-Phase ISL73847x Application Design

2. Conclusion

An Excel ISL73847x Design Tool that automatically calculates all the values derived in this document and more is available. However, it is beneficial to know how they were derived and to hand calculate some of the values.

3. Revision History

Revision	Date	Description
1.01	Jun 5, 2025	Added Determining the Current-Sense Filter section. Minor text updates throughout.
1.00	Dec 18, 2023	Initial release.

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