Working with the Radiation Hardened Instrumentation Amplifier ISL70617SEH

Introduction

The ISL70617SEH is a high-performance, differential input, differential output instrumentation amplifier (INA) designed for precision analog signal conditioning. It offers a wide supply range from 8V (±4V) to 36V (±18V), and provides a differential input voltage range of up to ±30V. The output stage, powered by separate supplies, has rail-to-rail drive capability optimized for driving differential ADC inputs. This feature allows the output stage of the INA to be powered by the ADC supplies, ensuring that the ADC input is not overdriven.

Several features not commonly found in other instrumentation amplifiers make this device suitable for a wide variety of signal conditioning applications that require high levels of DC precision and excellent AC performance.

This application note gives a quick overview of the device features and benefits, discusses its principle of operation, and provides a quick-start design procedure.

Contents

1. General Description

The ISL70617SEH is an enhanced radiation hardened instrumentation amplifier using transconductance amplifiers in a current feedback topology. This design approach provides the following features and benefits:

- Any gain setting including attenuation
- High gain accuracy through matched on-chip components
- High bandwidth at high gains
- Kelvin connections eliminating parasitic resistance of PCB traces
- High CMRR (>100dB) at any gain setting and without sensitivity to gain resistor tolerance
- User control of precision by choice of external resistor tolerance
- Separate supplies for input and output stages swing to prevent output overdrive
- Fully differential, rail-to-rail output for optimal ADC drive with output dynamic range set by feedback resistor
- Level-shifting interface from bipolar analog input signals to unipolar and bipolar output signal

The transconductance stages (GMs) are implemented with very high-gain (>140dB) amplifiers and transconductance drive transistors that impose input and feedback voltages on the gain and feedback resistors, R_{FB} and R_{IN}. With very high gain in the GMs, the transistor errors are linearized well below 10ppm. Therefore, the entire circuit adds little gain error and only the matching of the external R_{FB} and R_{IN} resistors determine the overall gain error.

Note: The separate output supply leaves the input stage completely unaffected by output biasing, which is ideal for level-shifting a bipolar input signal into a single-supplied output dynamic range.

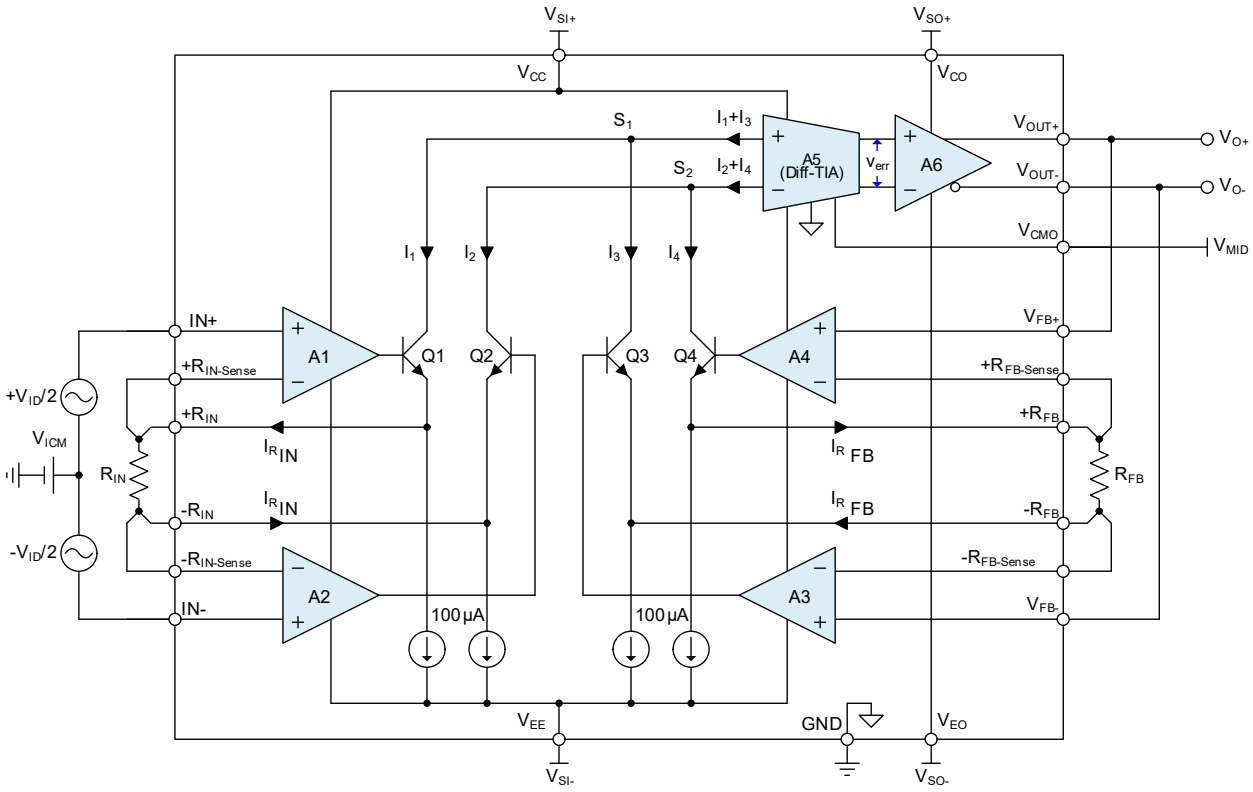

Figure 1. Functional Block Diagram

2. Functional Principle

Referring to Figure 1, the input stage consists of high performance, wideband amplifiers (A1, A2), transconductance drive transistors, Q1 and Q2, and input gain resistor, R_{IN}. Current drive for Q1 and Q2 emitters are provided by a matched pair of 100µA current sinks. A unity gain buffer from each input (IN+, IN-) to the terminals of the input resistor, R_{IN}, is formed by the connection of the Kelvin resistor sense pins ($+R_{IN\text{-}Sense}$, $-R_{IN\text{-}Sense}$) and drive pins ($+R_{IN}$, $-R_{IN}$) to the terminals of the input resistor, as shown in Figure 1.

In this configuration, the voltage across R_{IN} is equal to the input differential voltage across IN+ and IN-, therefore making the current through R_{IN}:

(EQ. 1) $$I_{R_{IN}} = \frac{V_{IN+} - V_{IN-}}{R_{IN}} = \frac{V_{ID}}{R_{IN}}$$

The input stage operates by creating a current difference in the collector currents Q1 and Q2 in response to the voltage difference between the IN+ and IN- pins. When the input voltage at IN+ and IN- pins is zero, the voltage across R_{IN}, is zero. Without current flowing through R_{IN}, the collector currents of Q1 and Q2 are equal: $I_1 = I_2$.

A change in the input differential voltage causes an equivalent voltage drop across the input gain resistor R_{IN}, and the resulting current flow through R_{IN} causes an imbalance in the collector currents, I_1 and I_2:

(EQ. 2) $$I_1 = 100\mu A + I_{R_{IN}} = 100\mu A + \frac{V_{ID}}{R_{IN}}$$

(EQ. 3) $$I_2 = 100\mu A - I_{R_{IN}} = 100\mu A - \frac{V_{ID}}{R_{IN}}$$

2.1 Feedback Transconductance Amplifier

The feedback amplifiers A3 and A4 form a differential transconductance amplifier identical to the one in the input stage. Their input terminals, VFB+ and VFB-, connect to the differential output terminals, +VOUT and -VOUT, so that the output voltage also appears across the feedback gain resistor R_{FB}, making the current through R_{FB}:

(EQ. 4) $$I_{R_{FB}} = \frac{V_{OUT+} - V_{OUT-}}{R_{FB}} = \frac{V_{OD}}{R_{FB}}$$

The operation is the same as for the input stage, therefore, creating the differential feedback currents, I_3 and I_4.

(EQ. 5) $$I_3 = 100\mu A - I_{R_{FB}} = 100\mu A - \frac{V_{OD}}{R_{FB}}$$

(EQ. 6) $$I_4 = 100\mu A + I_{R_{FB}} = 100\mu A + \frac{V_{OD}}{R_{FB}}$$

2.2 Error Amplifier A5 and Output Amplifier A6

Amplifiers A5 and A6 act together to form a high-gain, differential trans-impedance amplifier. The differential current amplifier A5 detects the difference between the current summing nodes, S_1 and S_2. This difference in current creates a differential error voltage at the input of A6, which generates a differential rail-to-rail output drive at the +VOUT and -VOUT pins.

The differential output voltage of A6 is fed into the differential input of the feedback stage (A3 and A4), which creates the compensation currents I_3 and I_4 that counteract I_1 and I_2 at the summing points S_1 and S_2.

Therefore, the differential output voltage of A6 becomes stable when current balance is restored, which is the difference in current between S_1 and S_2 is zero and $I_1 + I_3 = I_2 + I_4$.

This equilibrium is reached when $I_1 = I_4$ and $I_2 = I_3$, which makes

(EQ. 7) $$I_{R_{IN}} = I_{R_{FB}}$$

Substituting the currents in Equation 5 with Equation 1 and Equation 4 and solving for the circuit gain, V_{OD}/V_{ID}, yields:

(EQ. 8) $$\text{Gain} = \frac{V_{OD}}{V_{ID}} = \frac{R_{FB}}{R_{IN}}$$

3. Power Supply Settings

The input common-mode voltage range of the input and feedback amplifiers (A1 to A4) is limited to $V_{EE} + 3V \le V_{ICM} \le V_{CC} - 3V$. The direct connection between the output stage and the feedback input stage limits VOUT+ and VOUT- to the same common-mode range: $V_{EE} + 3V \le V_{OUT} \le V_{CC} - 3V$ (Figure 2).

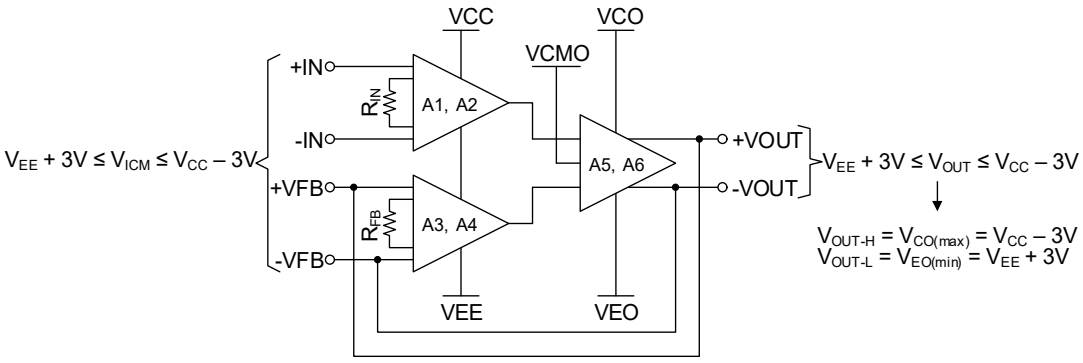

Figure 2. Power Supply Requirements

Due to the rail-to-rail capability of the output stage, this output common-range demands the following.

- The maximum positive output supply is $V_{CO(max)} \le V_{CC} - 3V$.
- The minimum negative output supply is $V_{EO(min)} \le V_{EE} + 3V$.

Note: Due to the V_{EO} requirement, a single-supply operation of the output does not allow the input and feedback amplifiers to operate from a single supply. Also, the minimum power supply of the output stage is 3V, that is $V_{CO} - V_{EO} = 3V$ (±1.5V).

4. Design Procedure

For a fast and successful design of a signal conditioning stage using the ISL70617SEH, complete the following recommended design procedure.

1. Define the output differential voltage swing based on your load or ADC input requirements.
2. To ensure output signal linearity, limit the current through the feedback resistor to 80% of the on-chip current sinks, calculating $R_{FB} = V_{OD}/\pm 80\mu A$.
3. For a required gain, calculate the input gain resistor with $R_{IN} = R_{FB}/Gain$.
4. Set the V_{CO} and V_{EO} output power supply voltages to $V_{CO} \geq VOUT_{High}$ and $V_{EO} \leq VOUT_{Low}$.
5. Set the V_{CC} and V_{EE} supply voltages to $V_{CC} \geq V_{CO} + 3V$ and $V_{EE} \leq V_{EO} - 3V$.
6. Set V_{CMO} to the mid-level of the output supplies: $(V_{CO} - V_{EO})/2$

Figure 3 shows a typical signal conditioner converting a bipolar ±15V input signal into a ±2.0V output signal that swings around a 2.5V dc common-mode voltage to match the input range of a single-ended 5V SAR ADC.

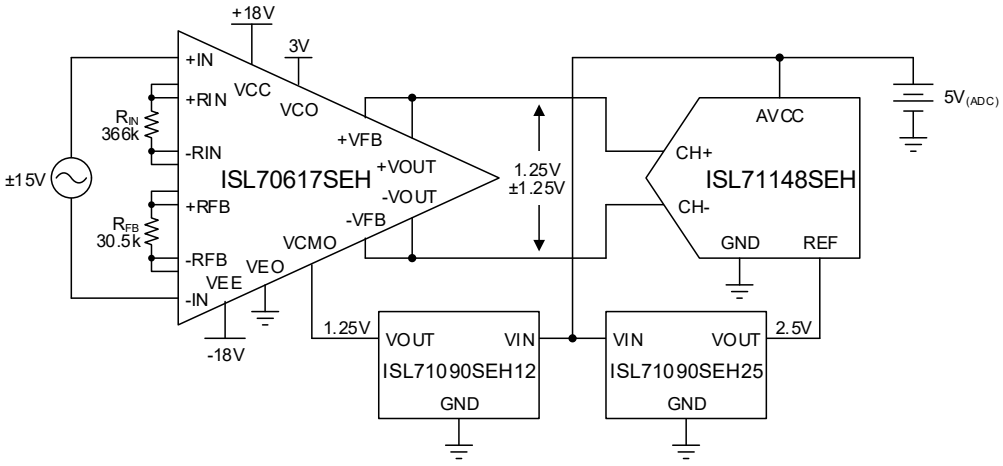

Figure 3. Space Grade Analog Signal Conditioner with ADC and VREFs

5. Conclusion

The ISL70617SEH has several advantages over the typical three op amp INAs. Its differential output enables high levels of DC precision and excellent AC performance and has features not found in other instrumentation amps. The ISL70617SEH features a wide range of gain including attenuation, gain error down to 10ppm, typical CMRR of >100dB at unity gain and a rail-to-rail output stage that can be powered from the same supplies as the ADC. This preserves the ADC maximum input dynamic range and eliminates ADC input overdrive.

Its precision and radiation hardened performance makes this amplifier ideal in analog sensor front ends, shunt current sensing, and instrumentation and data acquisition applications that require very low noise and high dynamic range in the space environment.

6. Revision History

Revision	Date	Description
1.00	Oct 13, 2025	Initial release.

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