R8A66593 / R8A66597

Guidelines for Hi-Speed USB 2.0 Board Design

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Summary

This document describes the guidelines for Hi-Speed USB 2.0 board design.

Operation Check Devices

The application explained in this document applies to the following ASSP.

- R8A66593 USB Peripheral Controller
- R8A66597 USB Host & Peripheral Controller

This document is described as “R8A66593 / 7” about “R8A66593” and “R8A66597”.

Note: The contents in this document are provided as a reference example based on USB specification, and the signal system quality is not guaranteed. When implementing this example into an existing system, the overall system should be thoroughly evaluated, and the user should integrate at their own discretion.

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1. Introduction

This document is described by using the pin names of R8A66593/ 7 . Table 1.1 lists the outline of R8A66593 USB2.0 module pin and Table 1.2 lists the outline of R8A66597 USB 2.0 module pin.

Table1.1 Outline of R8A66593 USB2.0 Module Pin

Pin number	Pin Name	I/O	Name	Function
40(J9)	DP0	I/O	USB D+ data	Connect to D+ pin of USB bus.
39(J8)	DM0	I/O	USB D- data	Connect to D- pin of USB bus.
41(H9)	VBUS	I	VBUS input	Connect directly to Vbus of USB bus. Can detect Vbus connection/disconnection. Connect to 5V when not connecting to Vbus.
27(J4)	REFRIN	I	Reference input	Connect to AGND pin through 5.6kΩ±1% resistor.
23(H3)	XIN	I	USB crystal resonator/ External clock	Connect crystal oscillator between XIN and XOUT. Connect external clock signal to XIN in order to input external clock, and leave open XOUT.
24(J3)	XOUT	O		
25(G3)	AVCC	I	Transceiver analog pin power supply	3.3V analog power supply for pins.
26(H4)	AGND	I	Transceiver analog pin ground	3.3V analog ground for pins.
22,35,43 (G9),(H5),(J2)	VCC	I	Transceiver digital pin power supply	3.3V digital power supply for pins.
11,21,29,32, 33,34,38,42, 45,50,61,71, 80 (A1),(A5),(A9), (E1),(E5),(E9), (F7),(G5),(G7), (H6),(H7),(H8), (J1),(J7)	GND	I	Transceiver digital pin ground	3.3V digital ground for pins.
1,20,60,70 (B1),(B5), (B9),(H1)	VIF	I	Power supply for I/O circuit	3.3V or 1.8V power supply for I/O pin.
10,51 (E2),(E8)	VDD	O	Core power	Connect the 4.7uF and 0.1uF capacitor between GND.

Note: In ( ) of the pin number, the pin number for the R8A66593BG package.

Table1.2 Outline of R8A66597 USB2.0 Module Pin

Pin number	Pin Name	I/O	Name	Function
40(J9)	DP0	I/O	USB D+ data	Connect to D+ pin of USB bus.
37(J6)	DP1			
39(J8)	DM0	I/O	USB D- data	Connect to D- pin of USB bus.
36(J5)	DM1			
41(H9)	VBUS	I	VBUS input	<Host Controller> Leave open or connect directly to Vbus of USB bus. *This pin cannot supply Vbus to the connected device. <Peripheral Controller>

Pin number	Pin Name	I/O	Name	Function
				Connect directly to Vbus of USB bus. Can detect Vbus connection/disconnection. Connect to 5V when not connecting to Vbus.
27(J4)	REFRIN	I	Reference input	Connect to AGND pin through 5.6kΩ±1% resistor.
23(H3)	XIN	I	USB crystal resonator/ External clock	Connect crystal oscillator between XIN and XOUT. Connect external clock signal to XIN in order to input external clock, and leave open XOUT.
24(J3)	XOUT	O		
25(G3)	AVCC	I	Transceiver analog pin power supply	3.3V analog power supply for pins.
26(H4)	AGND	I	Transceiver analog pin ground	3.3V analog ground for pins.
22,35,43 (G9),(H5),(J2)	VCC	I	Transceiver digital pin power supply	3.3V digital power supply for pins.
11,21,38,42, 45,50,61,71, 80 (A1),(A5),(A9), (E1),(E5),(E9), (F7),(H8),(J1), (J7)	GND	I	Transceiver digital pin ground	3.3V digital ground for pins.
1,20,60,70 (B1),(B5), (B9),(H1)	VIF	I	Power supply for I/O circuit	3.3V or 1.8V power supply for I/O pin.
10,51 (E2),(E8)	VDD	O	Core power	Connect the 4.7uF and 0.1uF capacitor between GND.
30(F5)	VBOUT0	O	External power on	Used for ON/OFF output to external power supply circuit. Connect to external power supply circuit for Vbus supply. VBOUT1 pin cannot be used when using DP0, DM0 as OTG.
28(G4)	VBOUT1	O		
33(H7)	OVCUR0A	I	Overcurrent input for Port0	Used for input of over-current detection from external power supply circuit. Connect to PORT0 external power supply circuit. When input for over-current detection from external power supply circuit is one pin, connect to OVCUR0A and fix OVCUR0B to High or Low.
34(H6)	OVCUR0B	I		
29(G5)	OVCUR1	I	Overcurrent input for Port1	Used for input of over-current detection from external power supply circuit. Connect to PORT1 external power supply circuit. OVCUR1 pin cannot be used when using DP0, DM0 as OTG.
31(G6)	EXTLP0	O	Control of external power for low power consumption	Used for low-power consumption mode ON/OFF switch when external power supply circuit has low-consumption mode. Connect to PORT0 external power supply circuit.
32(G7)	ID0	I	ID input	When using USB Micro-AB receptacle, connect to ID pin.

Note: In ( ) of the pin number, the pin number for the R8A66597BG package.

2. USB Transmission Line

The USB transmission line indicates the wiring pattern that connects the USB connector and the R8A66593 / 7 embedded USB transceiver.
USB 2.0 has three communication modes: Hi-Speed, Full-Speed and Low-Speed modes. The Hi-Speed mode has a 480Mbps communication speed. Therefore, the USB transmission lines must be designed as a high-frequency circuit. Impedance control is required for the USB transmission lines.
Notes on designing the wiring pattern of USB transmission lines are described below.

- The characteristic impedance required for the USB transmission lines is the differential impedance 90Ω ±15%.
- The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more details.
- The wiring pattern length of USB transmission lines from the R8A66593 / 7 to the USB connector must be designed not to exceed the maximum delay time which is regulated by the USB specification. Table 2 lists the recommended values for the wiring pattern length of USB transmission lines for host and Peripheral.

Table 2 Recommended Value for the Wiring Pattern Length of USB Transmission Line

	Maximum Delay Time (USB Specification)	Wiring Length	D+ and D- Wiring Length Differential
Host Controller	3ns	300mm or less	2.5mm or less
Peripheral Controller	1ns	100mm or less	2.5mm or less

- The lower layer of the USB transmission lines must be a ground plane. The ground plane must be at least 2mm wider than the USB transmission lines. The power supply for the ground plane is GND
- Do not allocate other signal lines near the USB transmission lines. Particularly lines of heavily fluctuating signals, such as clock and data bus lines, must be allocated far from the USB transmission lines. Moreover, the USB transmission lines and other lines must not cross.
- The same layer (surface layer) as the USB transmission lines should be allocated 1mm from the USB transmission lines, and grounded with a guard ring.
- USB transmission lines should be allocated on the same layer without passing through a hole. In addition, wiring should not be divaricated.
- The USB transmission lines should be wired with uniform spaces.
- The USB transmission lines should be allocated far from the oscillator, power supply circuit, and other I/O connectors.
- The USB transmission lines should be wired with straight lines. If they are bent, they should be bent gently in an arc or up to 135 degrees, and not bent at acute angles (right angles).
- It is recommended that the clock, reset, read, write and chip select signals should be grounded with a guard ring.

Figure 1 shows a design example of a Host controller USB transmission line pattern, and figure 2 shows a design example of a Peripheral controller USB transmission line pattern.

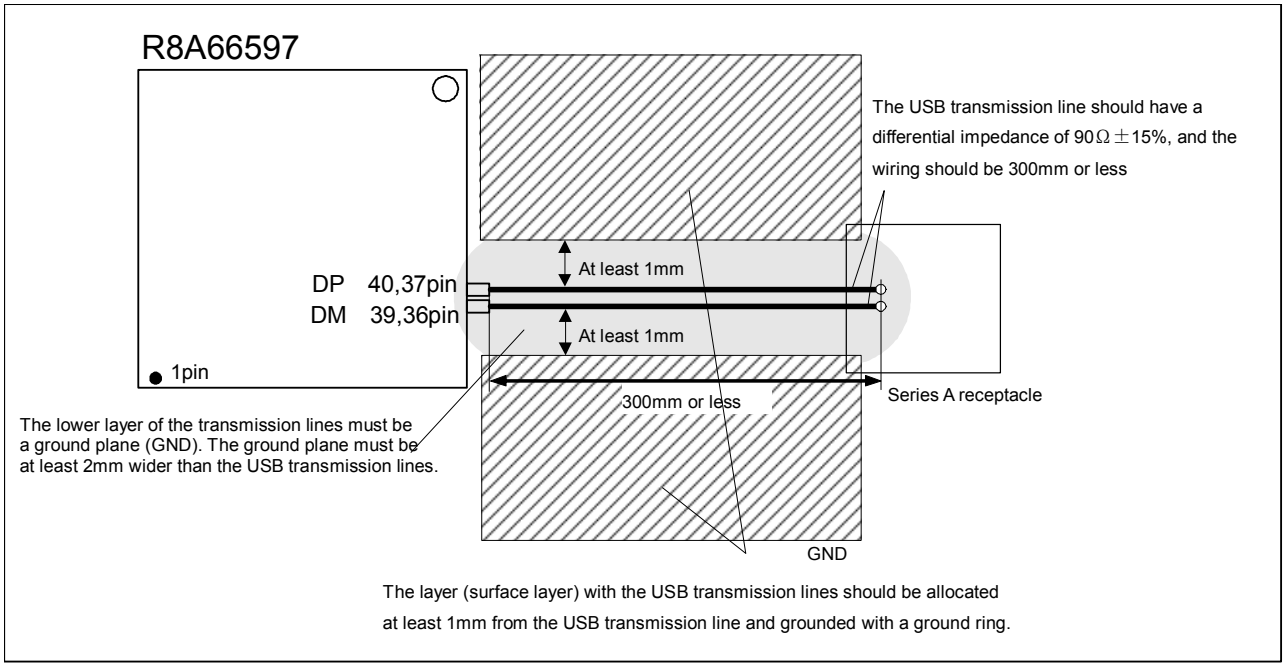

Figure 1 Design Example of a Host Controller USB Transmission Line Pattern

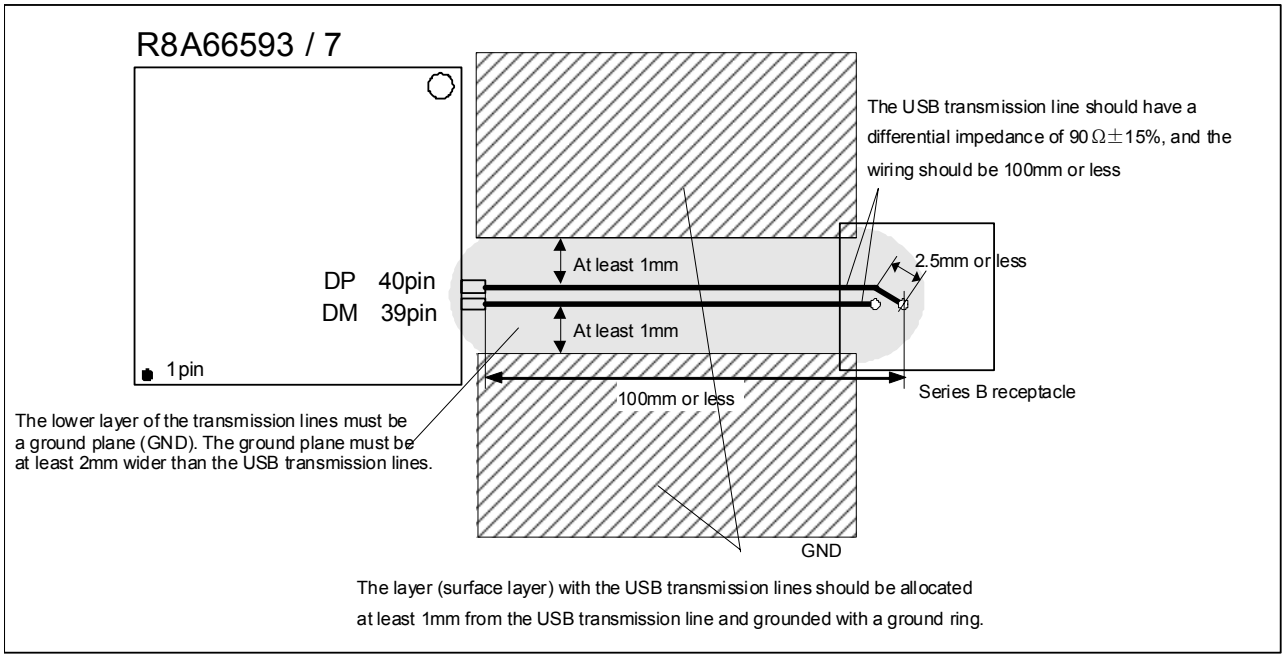

Figure 2 Design Example of a Peripheral Controller USB Transmission Line Pattern

3. Power Supply and Ground Pattern

Notes on designing a power supply/ground pattern are described below.

- Power supplies and ground patterns should be separated into digital and analog. Table 3 and Table 4 list the power supply and ground classifications.

Table 3 USB Power Supply Classifications

R8A66593 / 7 Pin Name	Power Supply Classifications			
	Analog Power Supply (3.3V)	Digital Power Supply (3.3V)	Digital Power Supply (1.8V)	Digital Core Power Supply
AVCC	○			
VCC		○		
VIF		○	○	

○: Indicates power used.

Table 4 USB Ground Classifications

R8A66593 / 7 Pin Name/ USB Connector	Ground Classifications	
	Analog Ground (AGND)	Digital Ground (GND)
AGND	○	
GND		○
USB Connector Ground (Including Frame Ground)		○

○: Indicates the ground used.

- The patterns of power supplies and grounds should be designed with as wide a surface layer as possible.
- Tantalum capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as power supply capacitors.
- Aluminum electrolytic capacitors affect the jitter value when measuring the EYE pattern. The capacitors should be thoroughly designed and tested before use.
- As the capacitance value of decoupling capacitor, it is recommended that the capacities for 0.001uF, 0.01uF, 0.1uF, and 10uF are allocated closest to the USB power supply pin. Figure 3 shows an example of decoupling capacitor allocation.
- Please connect digital ground and analog ground by one point near R8A66593 / 7.

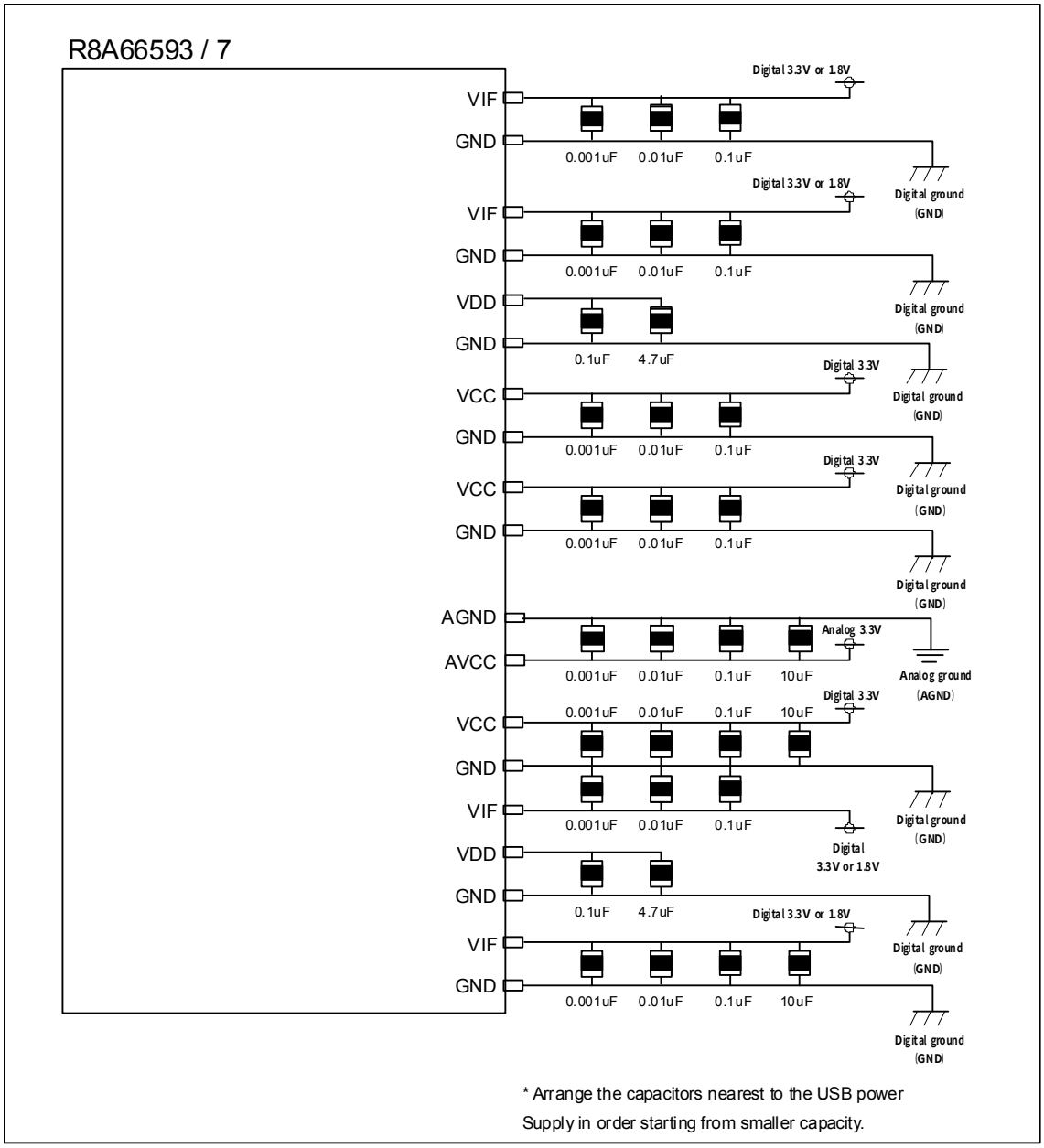

Figure 3 Example of Decoupling Capacitor Allocation

4. Oscillation Circuit

Notes on designing an oscillation circuit are described below.

- The oscillation circuit should be allocated near the XIN clock input pin. Grounding the XIN with a guard ring is recommended.
- Oscillation components that fulfill a 12, 24, 48 MHz ± 100ppm frequency specification should be used.
- When using a crystal resonator, the manufacturer should be consulted before deciding the circuit constant.

Figure 4 shows a connection example when the crystal resonator is used, and Figure 5 shows a connection example when an oscillator is used.

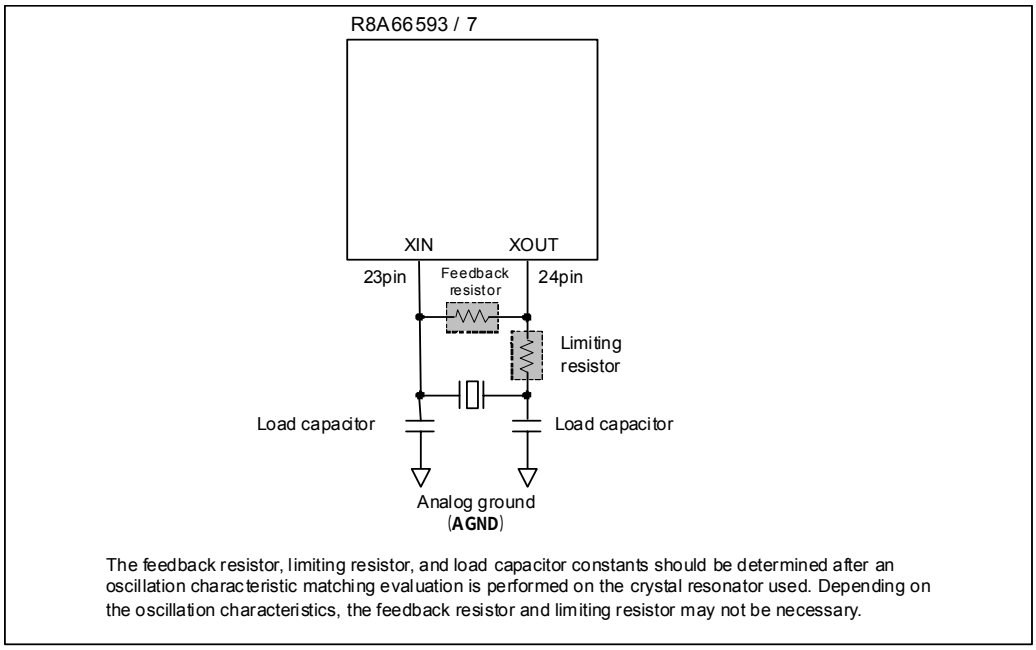

Figure 4 Example of a Crystal Resonator Connection

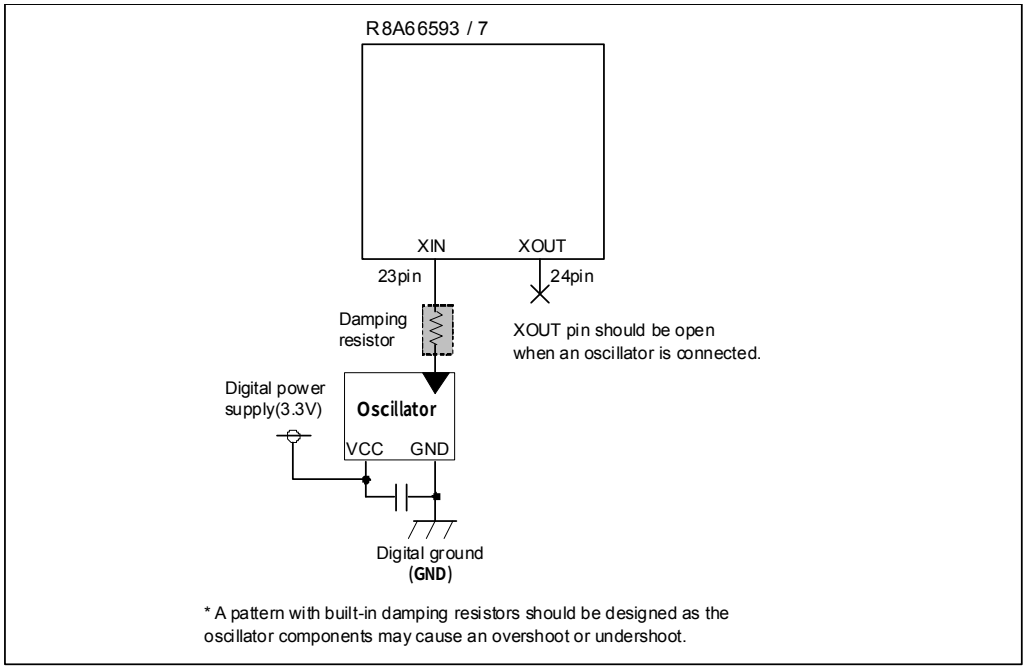

Figure 5 Example of an Oscillator Connection

5. VBUS Power Supply Circuit

Notes on designing the VBUS power supply circuit are described below.

- When the R8A66597 is used as a host controller, the additional capacity of the VBUS line should be designed to be 120uF or more.
- When the R8A66593 / 7 is used as a Peripheral controller, the additional capacity of the VBUS line should be designed to be within 1.0uF to 10uF.
- The VBUS line should include a filter circuit as an overshoot may be caused by inconsistent impedance when the USB cable is connected. The 1.0uF to 10uF capacitor and 100Ω to 1kΩ resistor should be added as a filter circuit. The constant should be defined after confirming that an overshoot has not occurred on the board. Also, a resistor of more than 1kΩ should not be added.
- When the R8A66597 is used as a host controller, the VBUS power should be supplied to the Peripheral devices. A power supply switch IC with over-current protection for the USB power bus (hereinafter called “USB power supply switch IC”) is recommended for the VBUS power supply control. Make sure to consider the limitation value of the current of VBUS power supply line based on the current value used by the system power supply applied and the USB Peripheral devices communicated. In addition, refer to the USB power supply switch IC datasheet used for VBUS power supply control circuit.

Figure 6 shows an example of the VBUS power supply circuit when it is used as a host controller, and Figure 7 shows an example of the VBUS power supply circuit when it is used as a Peripheral controller.

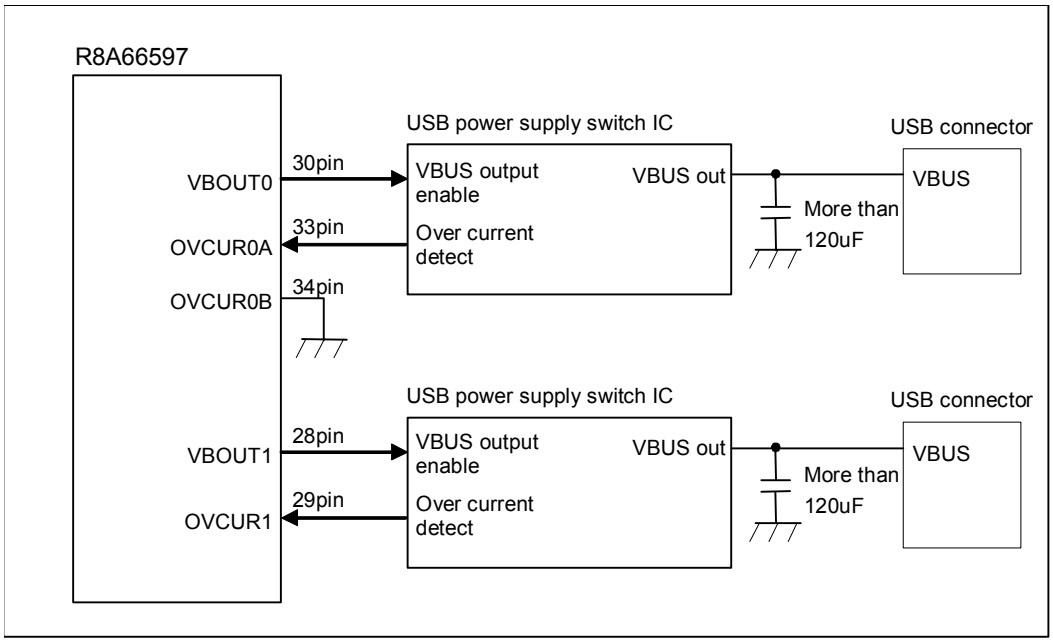

Figure 6 Example of Host Controller VBUS Power Supply Circuit

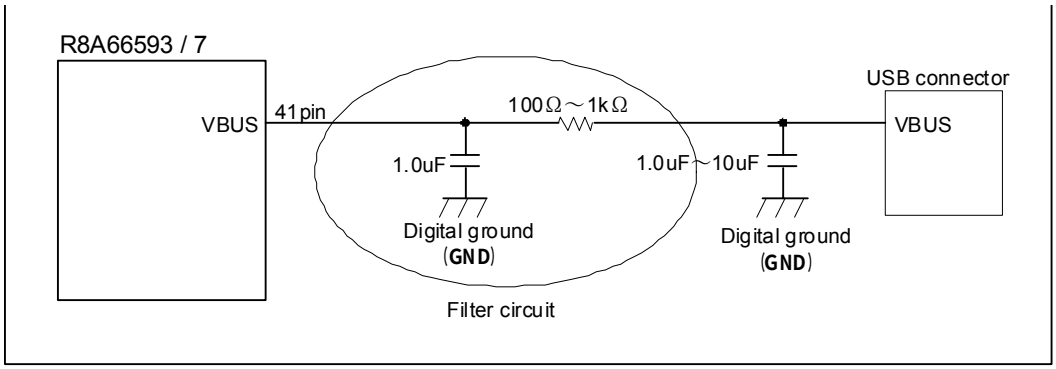

Figure 7 Example of Peripheral Controller VBUS Power Supply Circuit

6. REFRIN Pin

Notes on designing the circuit around the REFRIN pin are described below.

- A resistor of 5.6kΩ ± 1% (hereinafter called “standard resistor”) should be allocated between the REFRIN pin and AGND.
- A standard resistor should be allocated as close as possible to the R8A66593 / 7.
- The REFRIN pin, the standard resistor, and AGND should be connected with a bold, minimal pattern.
- The standard resistor and AGND should be connected in an exclusive pattern, and then connected to the analog ground. The pattern should be designed to avoid common impedance with other signals.
- To prevent cross talk, heavily fluctuating signals such as DP, DM, clocks, address data, and control signals should neither cross nor go side by side with standard resistor and patterns. It is recommended that standard resistor and patterns be grounded with a guard ring.

Figure 8 shows the block diagram of the pin connection and the design example of pattern around the REFRIN pin.

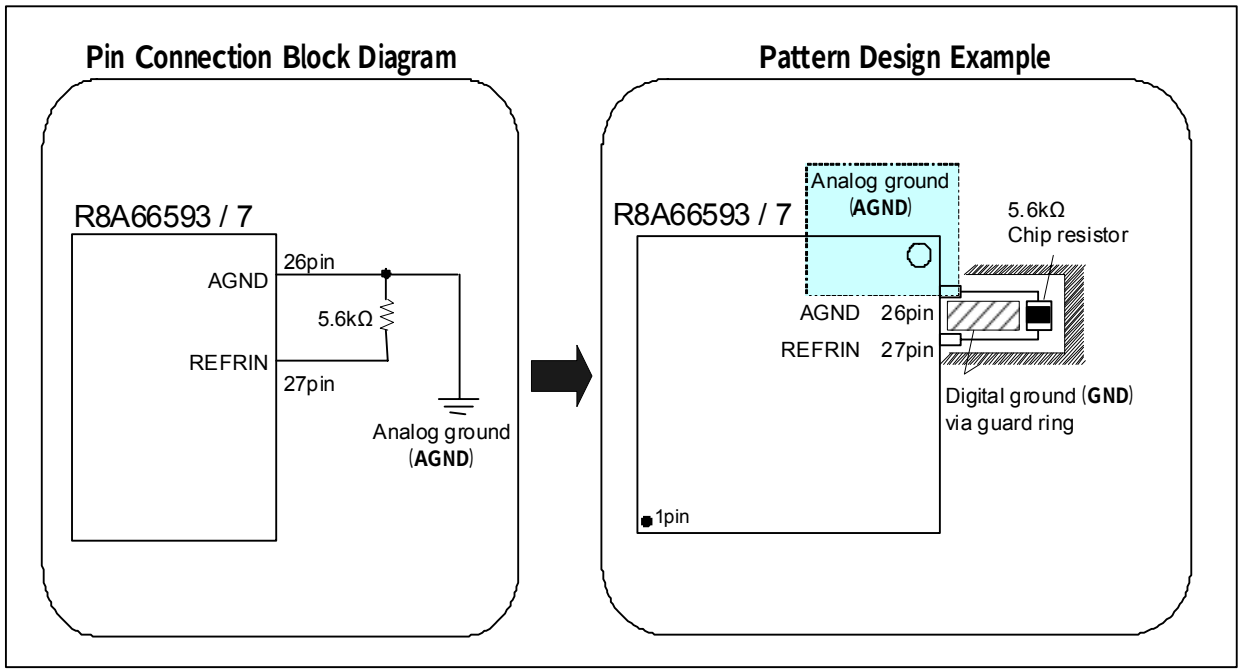

Figure 8 Pin Connection and Design Example of Pattern Around the REFRIN Pin

7. EMI/ESD Workarounds

Notes on EMI/ESD workarounds are described below.

- When components for EMI/ESD workarounds such as coils and diodes are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.
- The components for the EMI/ESD workarounds must be USB 2.0 compliant. Also, by mounting EMI/ESD workaround components, an inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.

Figure 9 shows the block diagram of a connection example when the components for EMI/ESD workarounds are used.

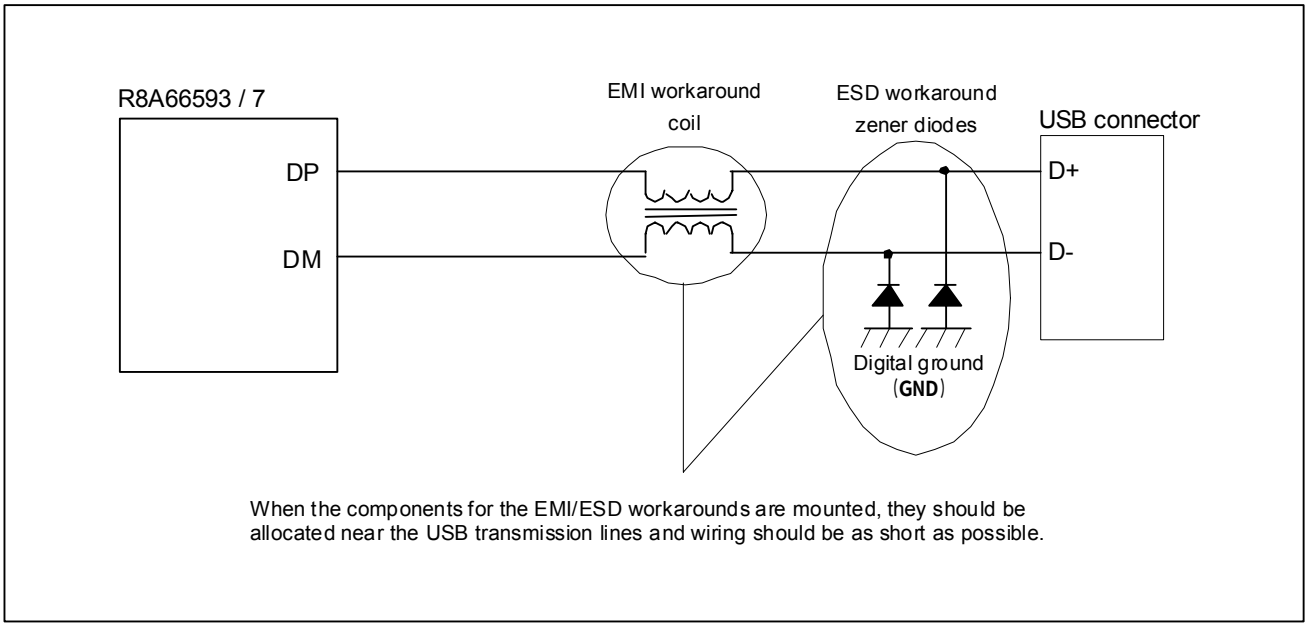

Figure 9 Connection Example When Components for EMI/ESD Workarounds are Used

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Revision History

Revision	Date	Description	
		Page	Summary
1.0RC1	July 28, 2008	-	First edition issued
1.0RC2	July 31, 2008	all	“function” -> “peripheral”
		P5	Figure1 change FONT
		P6	Table3 delete VDD
		P2	Table1 (E8) -> (H1)
		all	"USB power switch IC" -> "USB power supply switch IC"
		P12	Figure9 coil -> zener diodes
		P3	Figure1 “DP0/DM0” -> “DP0,DM0”
		P3	Figure1 “Mini-AB” -> “Micro-AB”
		all	“resistance” -> “resistor”
2.00	Dec.7 ,2012	-	Add R8A66593 information
		P.2	Add Table 1.1
		P.12	Figure7.1 delete Pin number of DP and DM.
		-	UpdateR Numder: REJ05F0024 ->R19AN0016EJ0200

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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