
R8C/27 Group

R01AN1277EJ0110

Timer RC in Input Capture Function

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1. Abstract

This document describes how to set up and use timer RC in the input capture function in the R8C/27 Group.

2. Introduction

The application example described in this document is applied to the following MCU and parameter(s):

- MCU: R8C/27 Group

This program can be used with other R8C/Tiny Series which have the same special function registers (SFRs) as the R8C/27 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

Note on oscillation stabilization wait time

In chapter 4.2.1 , select the high-speed on-chip oscillator after starting the high-speed on-chip oscillator and waiting until oscillation stabilizes.

3. Applications

3.1 Timer RC

Timer RC is a 16-bit timer with four I/O pins.

Timer RC uses either f1 or fOCO40M as its operation clock. Table 3.1 lists the Timer RC Operation Clock.

Table 3.1 Timer RC Operation Clock

Condition	Timer RC Operation Clock
Count source is f1, f2, f4, f8, f32, or TRCCLK input (bits TCK2 to TCK0 in TRCCR1 register are set to a value from 000b to 101b)	f1
Count source is fOCO40M (bits TCK2 to TCK0 in TRCCR1 register are set to 110b)	fOCO40M

Table 3.2 lists the Timer RC I/O Pins, and Figure 3.1 shows a Timer RC Block Diagram.

Timer RC has three modes:

- Timer mode
 - Input capture function The counter value is captured to a register, using an external signal as the trigger.
 - Output compare function Matches between the counter and register values are detected. (Pin output state changes when a match is detected.)

The following two modes use the output compare function:

- PWM mode Pulses of a given width are output continuously.
- PWM2 mode A one-shot waveform or PWM waveform is output following the trigger after the wait time has elapsed.

Input capture function, output compare function, and PWM mode settings may be specified independently for each pin.

In PWM2 mode, waveforms are output based on a combination of the counter and the register. Pin function is decided by the mode.

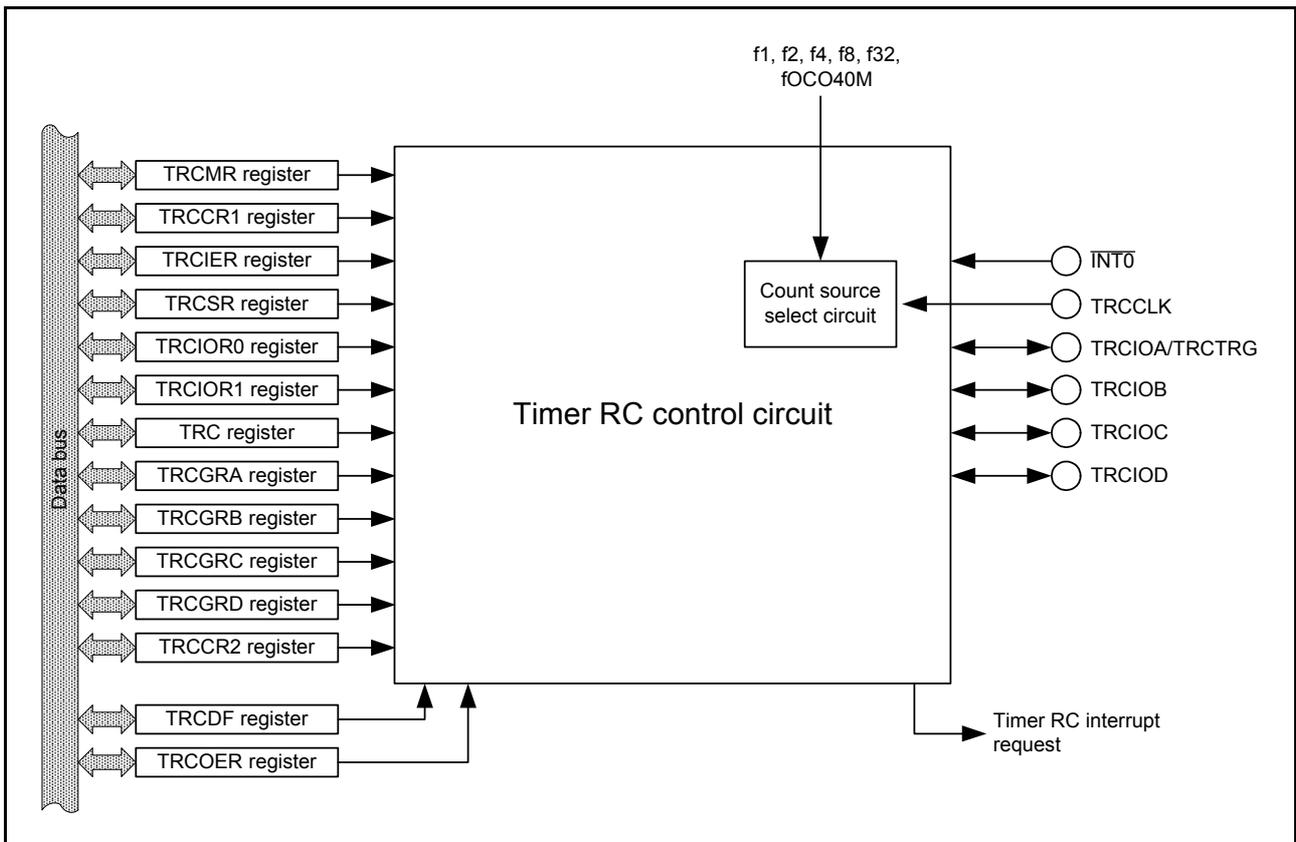


Figure 3.1 Timer RC Block Diagram

Table 3.2 Timer RC I/O Pins

Pin Name	I/O	Function
TRCIOA(P1_1) TRCIOB(P1_2) TRCIOC(P5_3 or P3_4) ⁽¹⁾ TRCIOD(P5_4 or P3_5) ⁽¹⁾	I/O	Function differs according to the mode. Refer to descriptions of individual modes for details.
TRCCLK(P3_3)	Input	External clock input
TRCTRIG(P1_1)	Input	PWM2 mode external trigger input

NOTE:

1. The pins used for TRCIOC and TRCIOD can be selected. Refer to the description of bits TRCIOCSEL and TRCIODSEL in the PINSR3 register in the **R8C/27 Group Hardware Manual** for details.

3.2 Registers Associated with Timer RC

Table 3.3 lists the Registers Associated with Timer RC. Figures 3.2 to 3.11 show details of the registers associated with timer RC.

Table 3.3 Registers Associated with Timer RC

Address	Symbol	Mode				Related Information
		Timer		PWM	PWM2	
		Input Capture Function	Output Compare Function			
0120h	TRCMR	Valid	Valid	Valid	Valid	Timer RC mode register Figure 3.2 TRCMR Register
0121h	TRCCR1	Valid	Valid	Valid	Valid	Timer RC control register 1 Figure 3.3 TRCCR1 Register
0122h	TRCIER	Valid	Valid	Valid	Valid	Timer RC interrupt enable register Figure 3.4 TRCIER Register
0123h	TRCSR	Valid	Valid	Valid	Valid	Timer RC status register Figure 3.5 TRCSR Register
0124h	TRCIOR0	Valid	Valid	-	-	Timer RC I/O control register 0, timer RC I/O control register 1 Figure 3.11 Registers TRCIOR0 and TRCIOR1 Figure 3.16 TRCIOR0 Register for Input Capture Function Figure 3.17 TRCIOR1 Register for Input Capture Function
0125h	TRCIOR1					
0126h 0127h	TRC	Valid	Valid	Valid	Valid	Timer RC counter Figure 3.6 TRC Register
0128h 0129h	TRCGRA	Valid	Valid	Valid	Valid	Timer RC general registers A, B, C, and D Figure 3.7 Registers TRCGRA, TRCGRB, TRCGRC, and TRCGRD
012Ah 012Bh	TRCGRB					
012Ch 012Dh	TRCGRC					
012Eh 012Fh	TRCGRD					
0130h	TRCCR2					
0131h	TRCDF	Valid	-	-	Valid	Timer RC digital filter function select register Figure 3.9 TRCDF Register
0132h	TRCOER	-	Valid	Valid	Valid	Timer RC output mask enable register Figure 3.10 TRCOER Register

- : Invalid

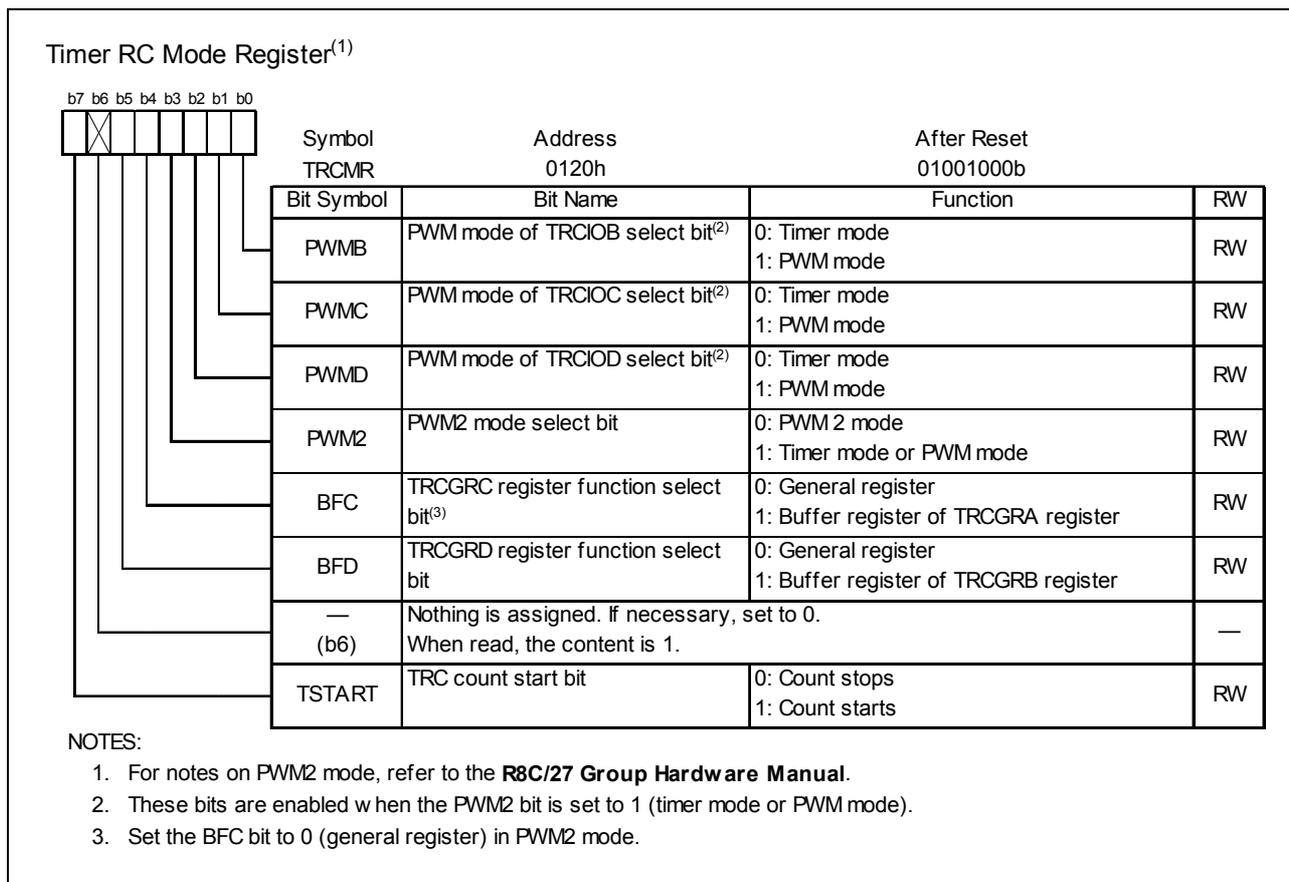


Figure 3.2 TRCMR Register

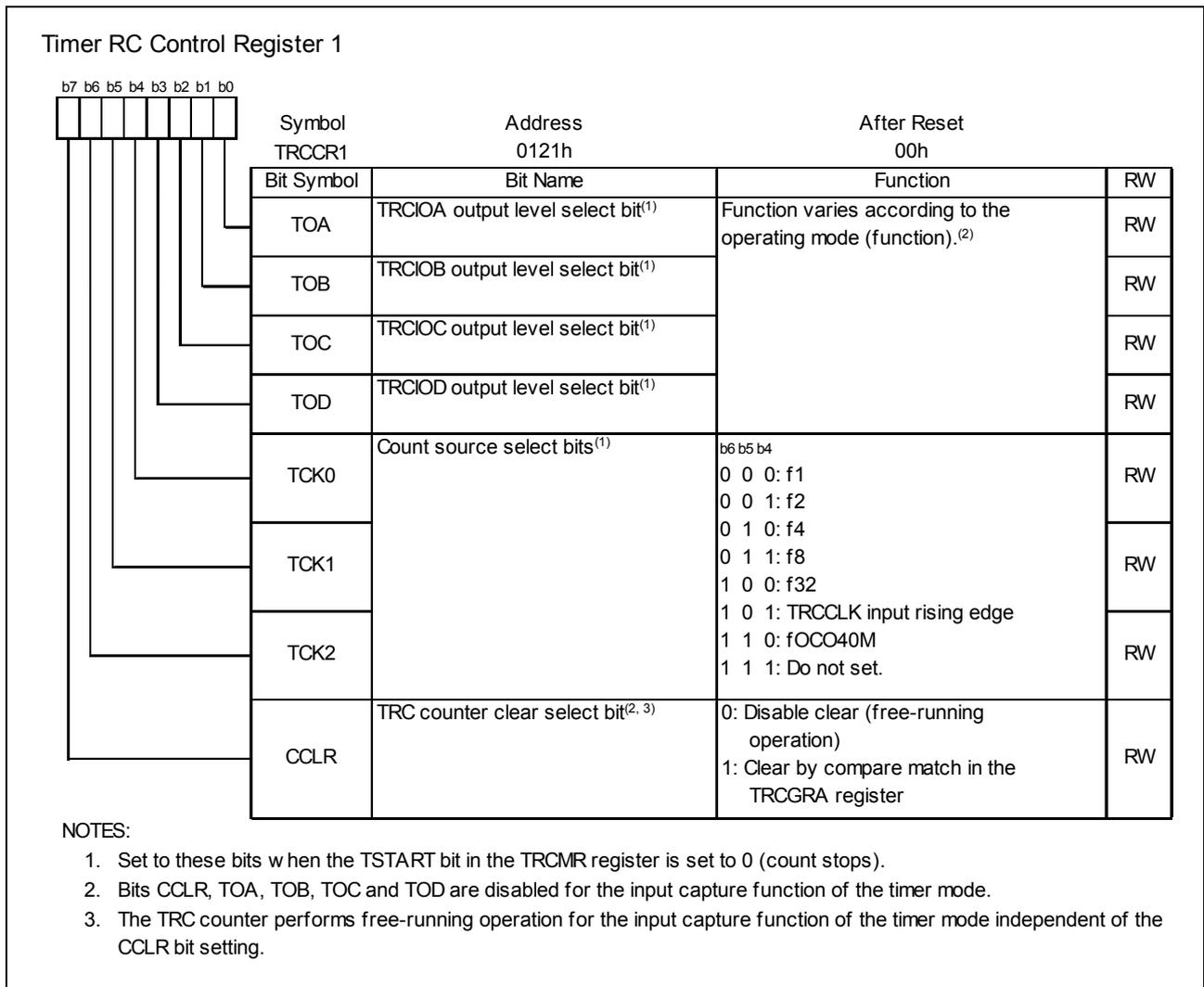


Figure 3.3 TRCCR1 Register

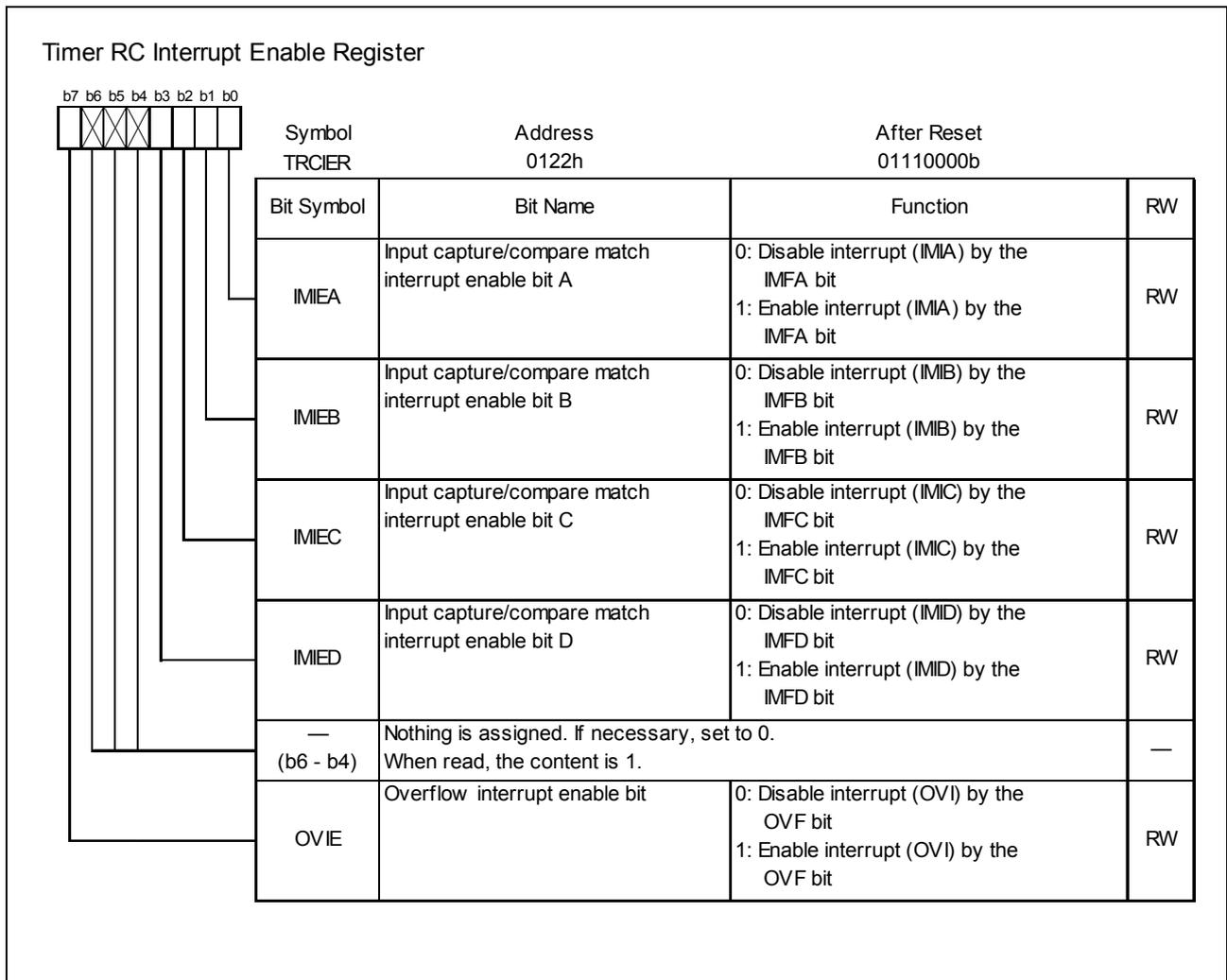


Figure 3.4 TRCIER Register

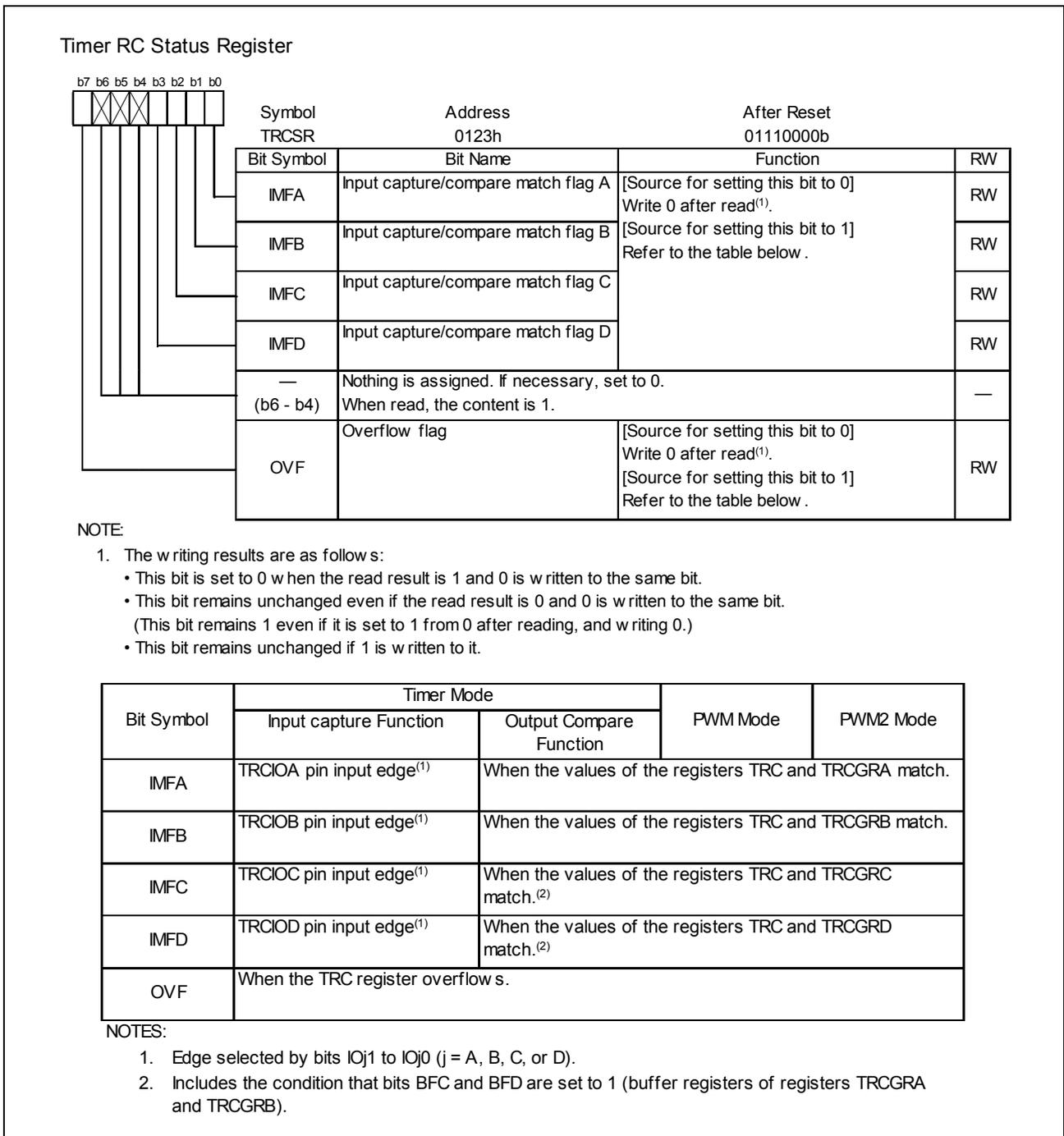


Figure 3.5 TRCSR Register

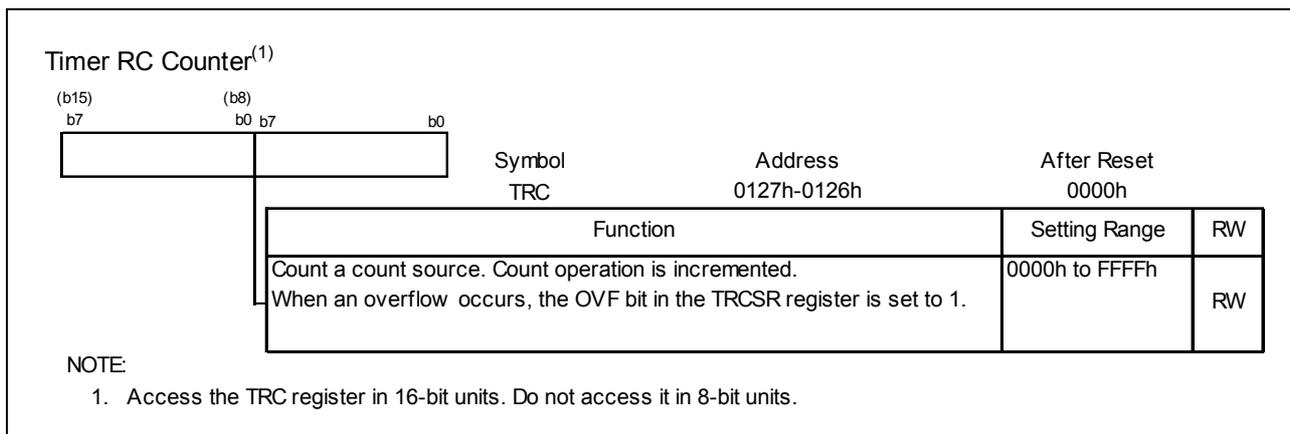


Figure 3.6 TRC Register

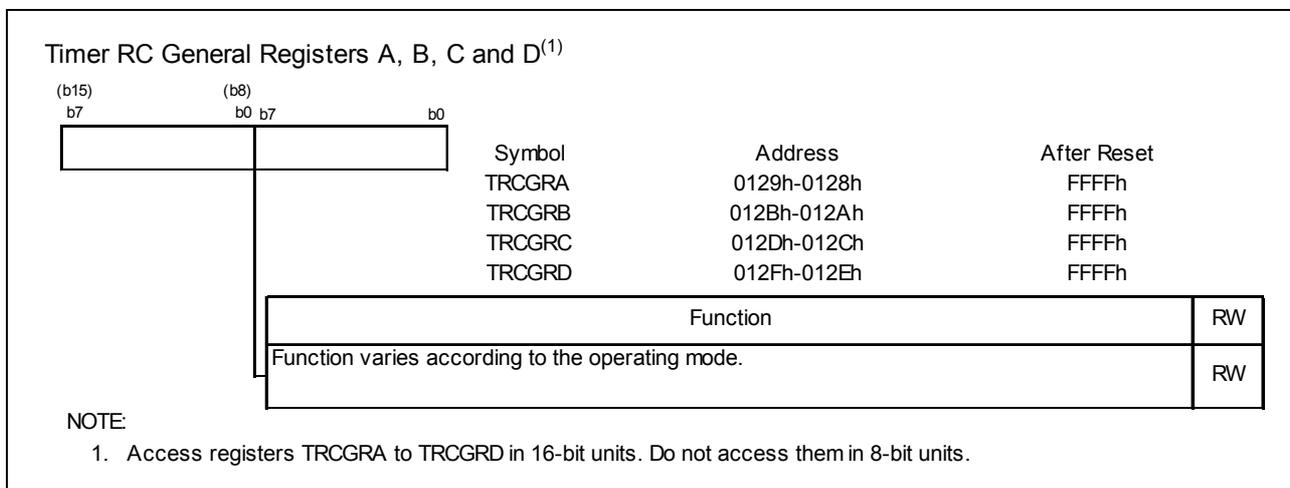


Figure 3.7 Registers TRCGRA, TRCGRB, TRCGRC, and TRCGRD

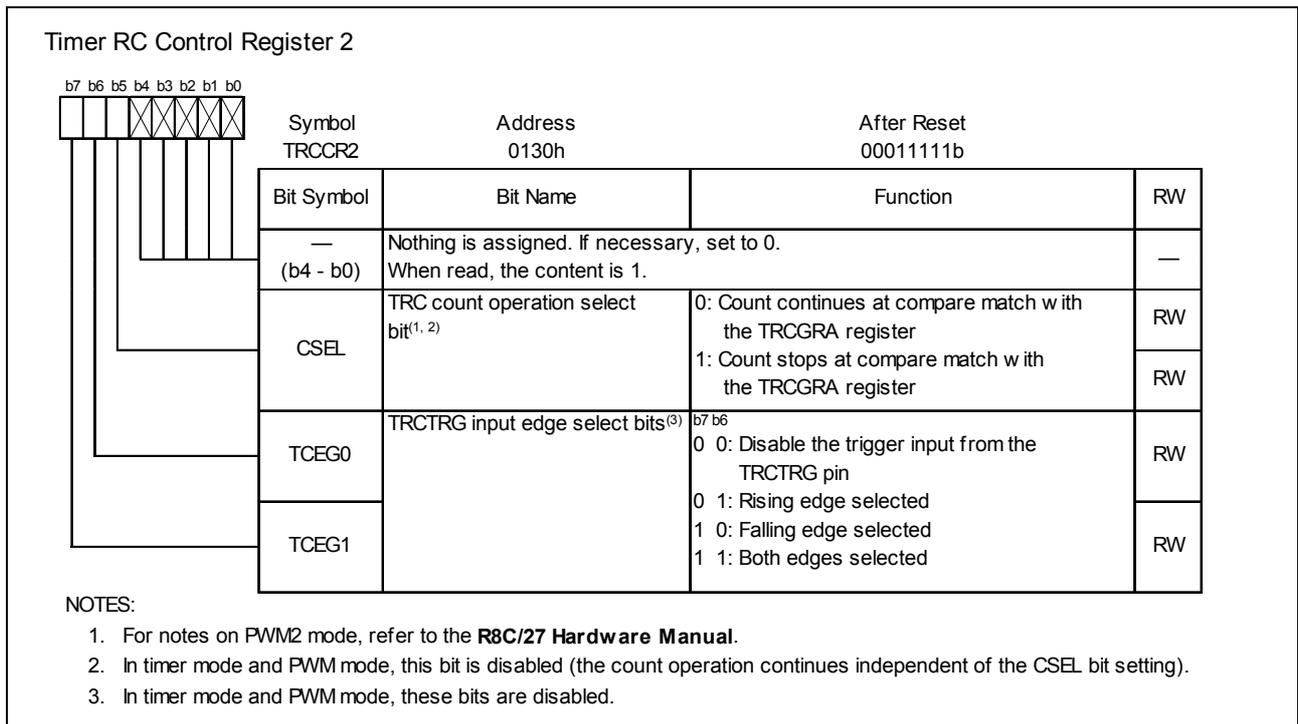


Figure 3.8 TRCCR2 Register

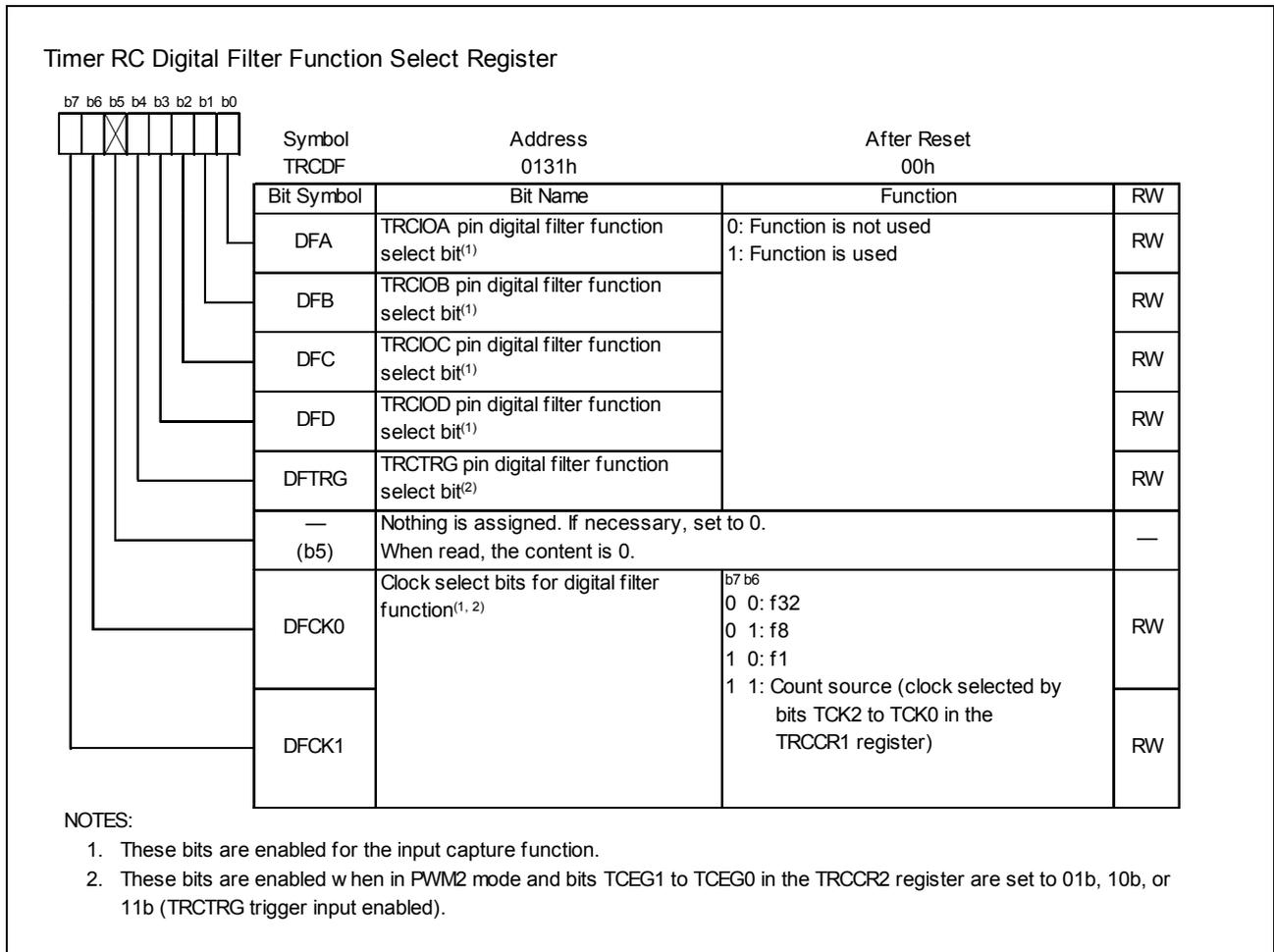


Figure 3.9 TRCDF Register

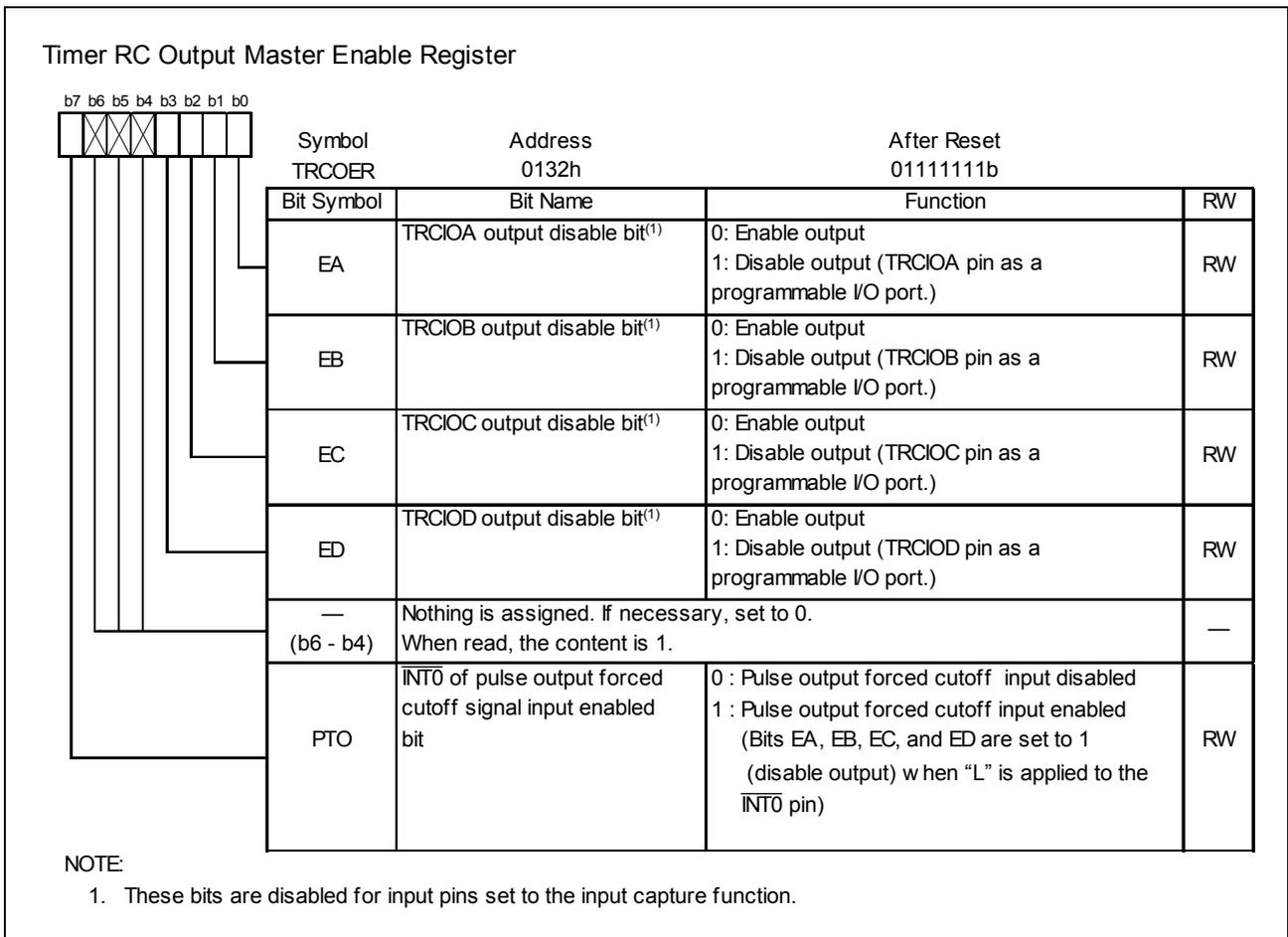


Figure 3.10 TRCOER Register

Timer RC I/O Control Register 0⁽¹⁾

Bit	Symbol	Address	After Reset
b7	TRCIOR0	0124h	10001000b
b6			
b5			
b4			
b3			
b2			
b1			
b0			

Bit Symbol	Bit Name	Function	RW
IOA0	TRCGRA control bits	Function varies according to the operating mode (function).	RW
IOA1			RW
IOA2	TRCGRA mode select bit ⁽²⁾	0: Output compare function 1: Input capture function	RW
— (b3)	Reserved bit	Set to 1.	RW
IOB0	TRCGRB control bits	Function varies according to the operating mode (function).	RW
IOB1			RW
IOB2	TRCGRB mode select bit ⁽³⁾	0: Output compare function 1: Input capture function	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:

1. The TRCIOR0 register is enabled in timer mode. It is disabled in modes PWM and PWM2.
2. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
3. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Timer RC I/O Control Register 1⁽¹⁾

Bit	Symbol	Address	After Reset
b7	TRCIOR1	0125h	10001000b
b6			
b5			
b4			
b3			
b2			
b1			
b0			

Bit Symbol	Bit Name	Function	RW
IOC0	TRCGRC control bits	Function varies according to the operating mode (function).	RW
IOC1			RW
IOC2	TRCGRC mode select bit ⁽²⁾	0: Output compare function 1: Input capture function	RW
— (b3)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—
IOD0	TRCGRD control bits	Function varies according to the operating mode (function).	RW
IOD1			RW
IOD2	TRCGRD mode select bit ⁽³⁾	0: Output compare function 1: Input capture function	RW
— (b7)	Nothing is assigned. If necessary, set to 0. When read, the content is 1.		—

NOTES:

1. The TRCIOR1 register is enabled in timer mode. It is disabled in modes PWM and PWM2.
2. When the BFC bit in the TRCMR register is set to 1 (buffer register of TRCGRA register), set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
3. When the BFD bit in the TRCMR register is set to 1 (buffer register of TRCGRB register), set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

Figure 3.11 Registers TRCIOR0 and TRCIOR1

3.3 Common Items for Multiple Modes

3.3.1 Count Source

The method of selecting the count source is common to all modes.

Table 3.4 lists the Count Source Selection, and Figure 3.12 shows a Count Source Block Diagram.

Table 3.4 Count Source Selection

Count Source	Selection Method
f1, f2, f4, f8, f32	Count source selected using bits TCK2 to TCK0 in TRCCR1 register
fOCO40M	FRA00 bit in FRA0 register set to 1 (high-speed on-chip oscillator on) and bits TCK2 to TCK0 in TRCCR1 register are set to 110b (fOCO40M)
External signal input to TRCCLK pin	Bits TCK2 to TCK0 in TRCCR1 register are set to 101b (count source is rising edge of external clock) and PD3_3 bit in PD3 register is set to 0 (input mode)

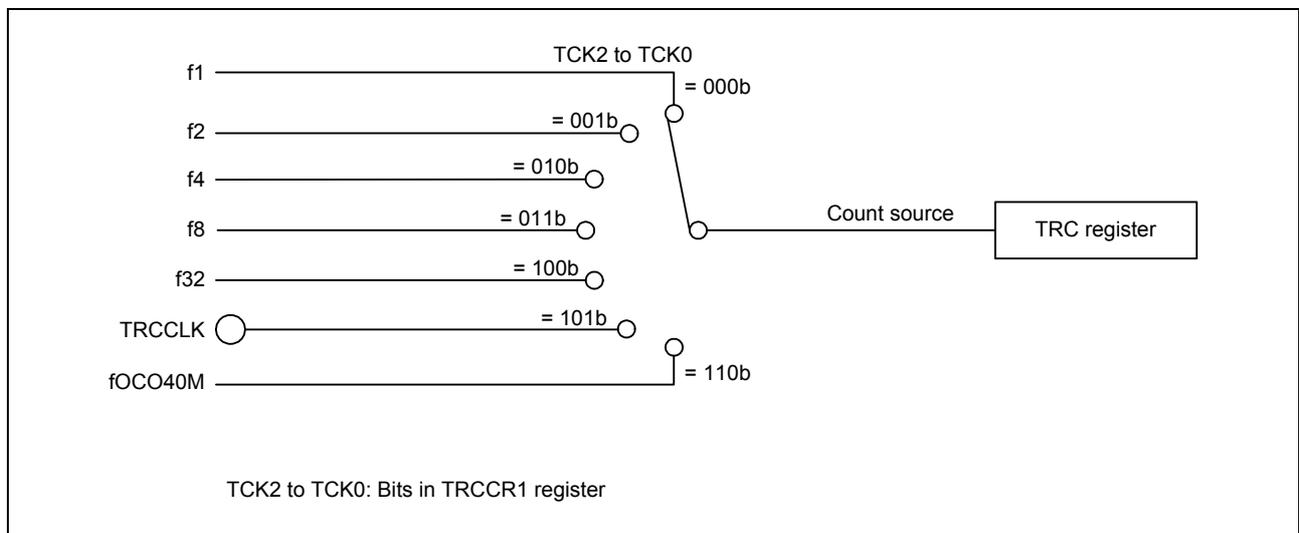


Figure 3.12 Count Source Block Diagram

The pulse width of the external clock input to the TRCCLK pin should be three cycles or more of the timer RC operation clock (see **Table 3.1 Timer RC Operation Clock**).

To select fOCO40M as the count source, set the FRA00 bit in the FRA0 register to 1 (high-speed on-chip oscillator on), and then set bits TCK2 to TCK0 in the TRCCR1 register to 110b (fOCO40M).

3.3.2 Buffer Operation

Bits BFC and BFD in the TRCMR register are used to select the TRCGRC or TRCGRD register as the buffer register for the TRCGRA or TRCGRB register.

- Buffer register for TRCGRA register: TRCGRC register
- Buffer register for TRCGRB register: TRCGRD register

Buffer operation differs depending on the mode.

Table 3.5 lists the Buffer Operation in Each Mode, and Figure 3.13 shows the Buffer Operation for Input Capture Function.

Table 3.5 Buffer Operation in Each Mode

Function, Mode	Transfer Timing	Transfer Destination Register
Input capture function	Input capture signal input	Contents of TRCGRA (TRCGRB) register are transferred to buffer register
Output compare function	Compare match between TRC register and TRCGRA (TRCGRB) register	Contents of buffer register are transferred to TRCGRA (TRCGRB) register
PWM mode		
PWM2 mode	<ul style="list-style-type: none"> • Compare match between TRC register and TRCGRA register • TRCTRIG pin trigger input 	Contents of buffer register (TRCGRD) are transferred to TRCGRB register

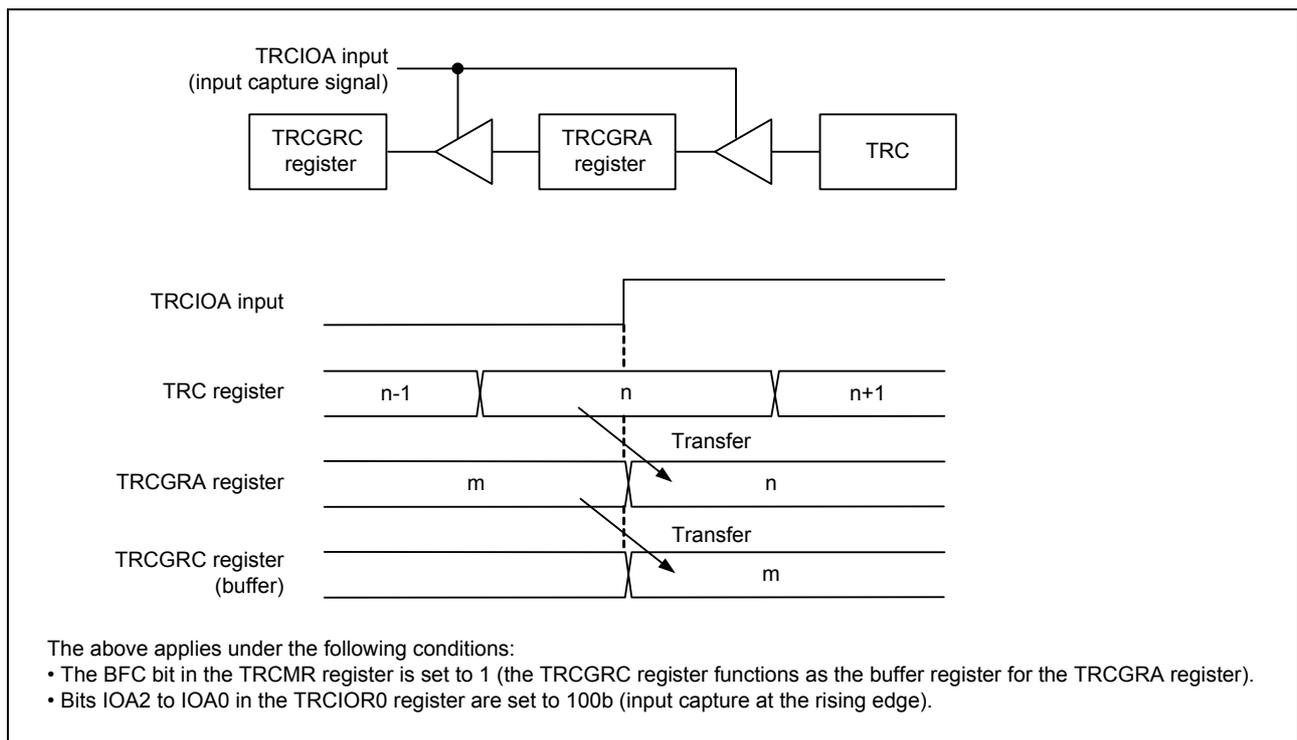


Figure 3.13 Buffer Operation for Input Capture Function

Set the following in timer mode:

- To use the TRCGRC register as the buffer register for the TRCGRA register:
Set the IOC2 bit in the TRCIOR1 register to the same value as the IOA2 bit in the TRCIOR0 register.
- To use the TRCGRD register as the buffer register for the TRCGRB register:
Set the IOD2 bit in the TRCIOR1 register to the same value as the IOB2 bit in the TRCIOR0 register.

When the input capture function and the TRCGRC register or TRCGRD register is also functioning as a buffer register, the IMFC bit or IMFD bit in the TRCSR register is set to 1 at the input edge of a signal input to the TRCIO pin or TRCIOD pin.

3.3.3 Digital Filter

The input to TRCTR_G or TRCIO_j (j = A, B, C, or D) is sampled, and the level is considered to be determined when three matches occur. The digital filter function and sampling clock are selected using the TRCDF register. Figure 3.14 shows a Block Diagram of Digital Filter.

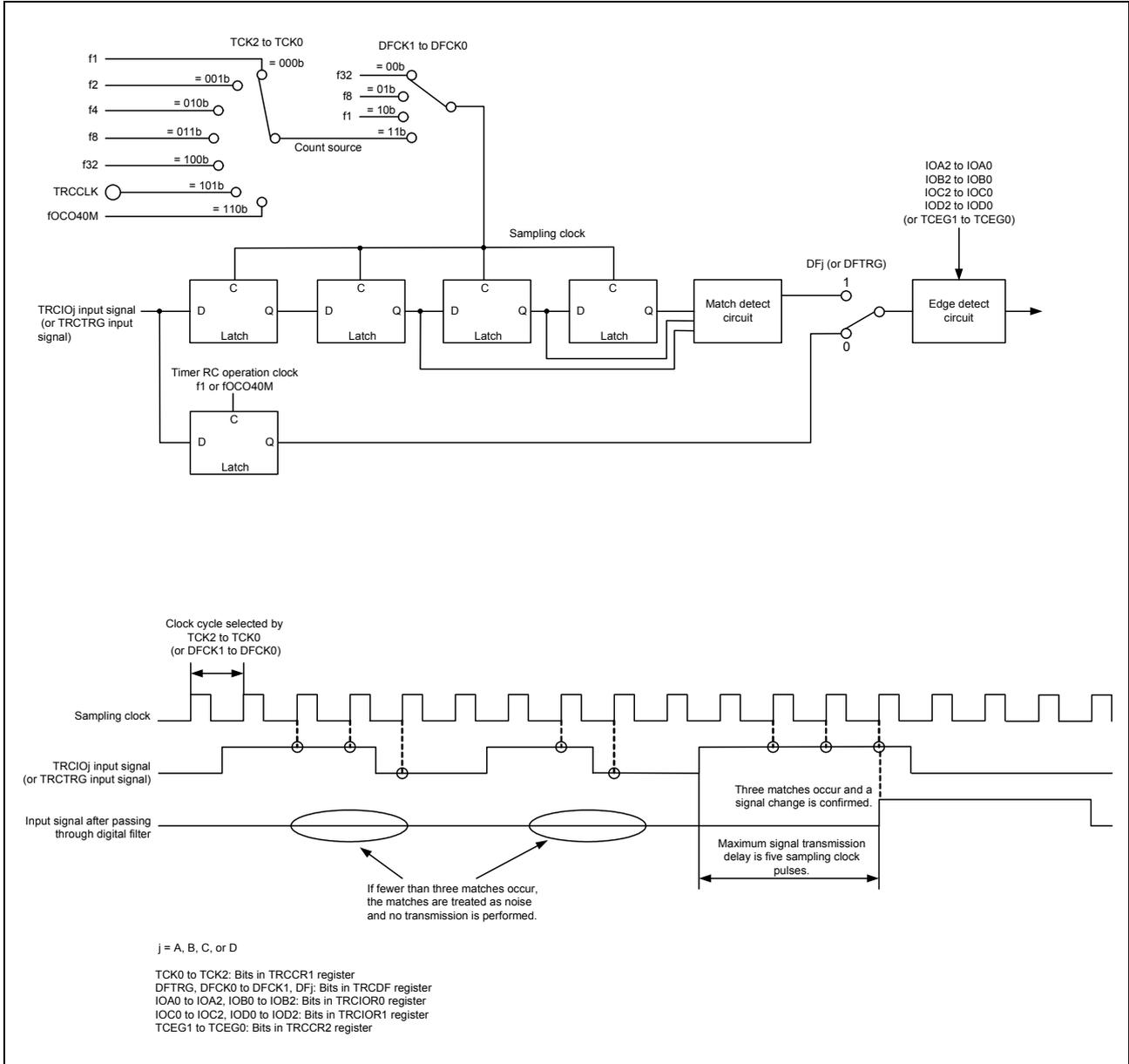


Figure 3.14 Block Diagram of Digital Filter

3.4 Timer Mode (Input Capture Mode Function)

This function measures the width or period of an external signal. An external signal input to the TRCIOj (j = A, B, C, or D) pin acts as a trigger for transferring the contents of the TRC register (counter) to the TRCGRj register (input capture). The input capture function, or any other mode or function, can be selected for each individual pin.

Table 3.6 lists the Specifications of Input Capture Function, Figure 3.15 shows a Block Diagram of Input Capture Function, Figure 3.16 and Figure 3.17 show registers associated with the input capture function, Table 3.7 lists the Functions of TRCGRj Register when Using Input Capture Function, and Figure 3.18 shows an Operating Example of Input Capture Function.

Table 3.6 Specifications of Input Capture Function

Item	Specification
Count source	f1, f2, f4, f8, f32, fOCO40M, or external signal (rising edge) input to TRCCLK pin
Count operation	Increment
Count period	$1/fk \times 65,536 fk$: Count source frequency
Count start condition	1 (count starts) is written to the TSTART bit in the TRCMR register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRCMR register. The TRC register retains a value before count stops.
Interrupt request generation timing	<ul style="list-style-type: none"> Input capture (valid edge of TRCIOj input signal) The TRC register overflows.
TRCIOA, TRCIOB, TRCIOC, and TRCIOD pin functions	Programmable I/O port or input capture input (selectable individually by pin)
INT0 pin function	Programmable I/O port or $\overline{INT0}$ interrupt input
Read from timer	The count value can be read by the reading TRC register.
Write to timer	The TRC register can be written to.
Select functions	<ul style="list-style-type: none"> Input capture input pin select One or more of pins TRCIOA, TRCIOB, TRCIOC, and TRCIOD Input capture input valid edge selected Rising edge, falling edge, or both rising and falling edges Buffer operation (refer to 3.3.2 Buffer Operation) Digital filter (refer to 3.3.3 Digital Filter)

j = A, B, C, or D

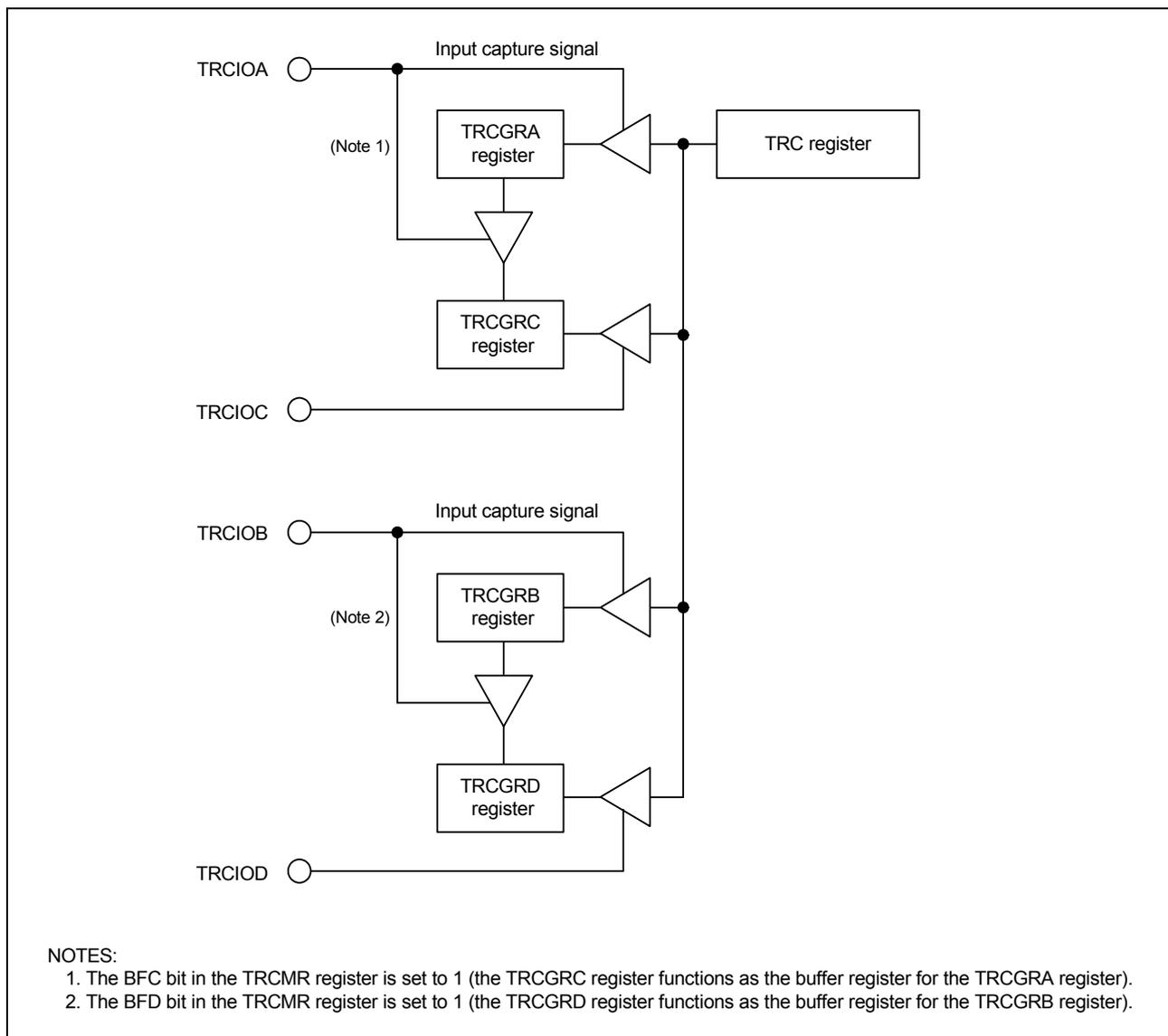


Figure 3.15 Block Diagram of Input Capture Function

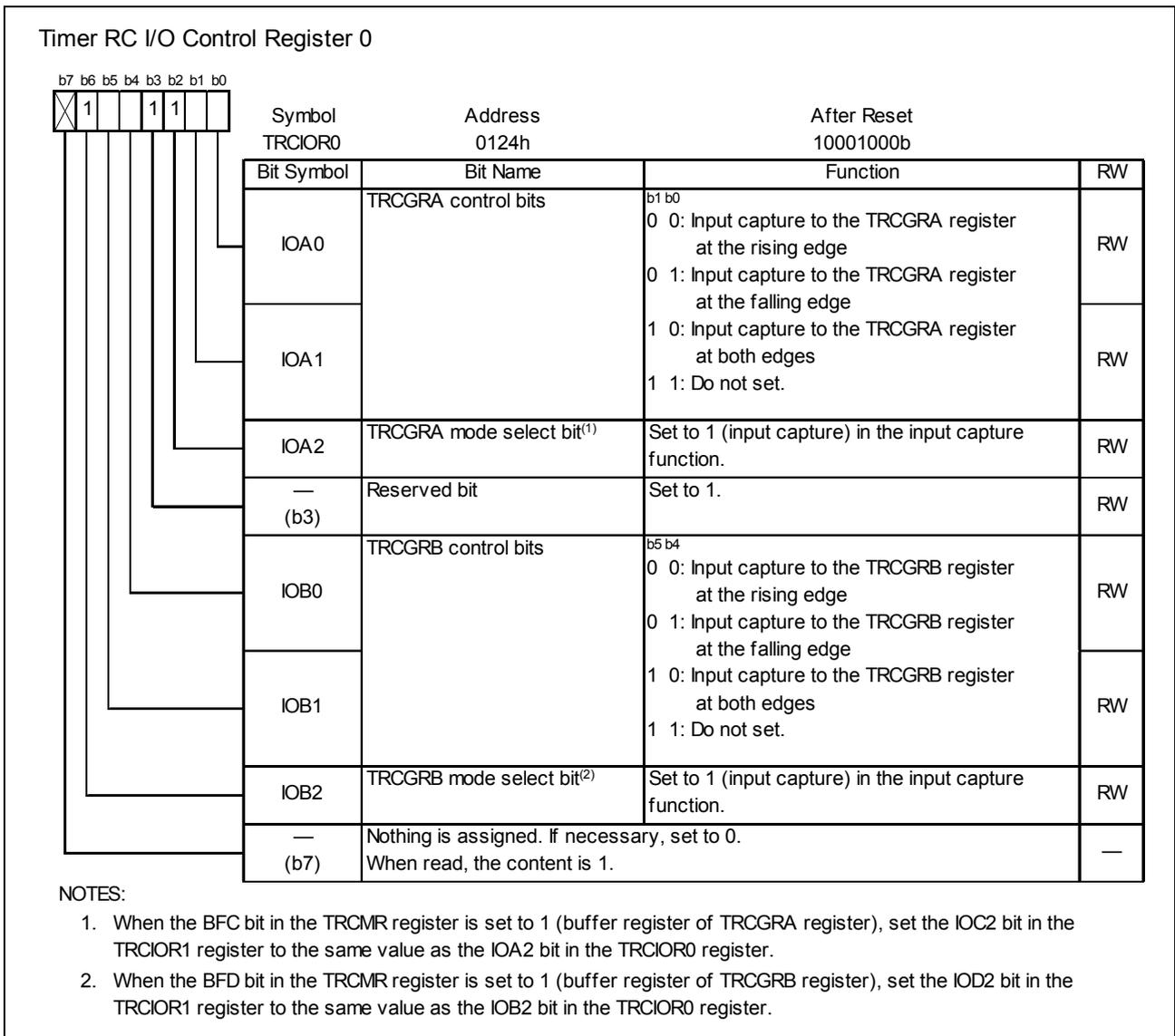


Figure 3.16 TRCIOR0 Register for Input Capture Function

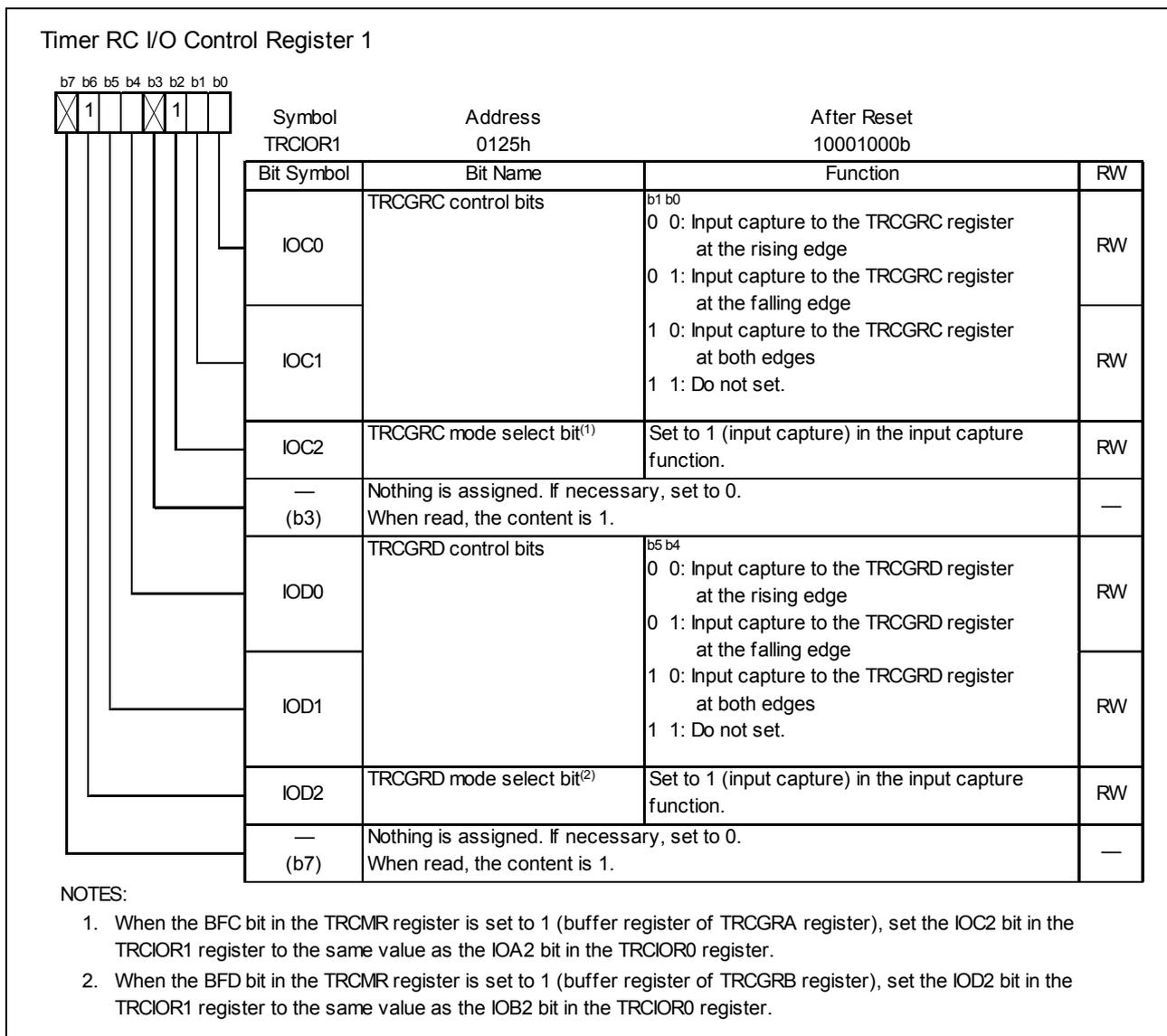


Figure 3.17 TRCIOR1 Register for Input Capture Function

Table 3.7 Functions of TRCGRj Register when Using Input Capture Function

Register	Setting	Register Function	Input Capture Input Pin
TRCGRA	—	General register. Can be used to read the TRC register value at input capture.	TRCIOA
TRCGRB			TRCIOB
TRCGRC	BFC = 0	General register. Can be used to read the TRC register value at input capture.	TRCIOC
TRCGRD	BFD = 0		TRCIOD
TRCGRC	BFC = 1	Buffer registers. Can be used to hold transferred value from the general register (refer to 3.3.2 Buffer Operation).	TRCIOA
TRCGRD	BFD = 1		TRCIOB

j = A, B, C, or D

BFC, BFD: Bits in TRCMR register

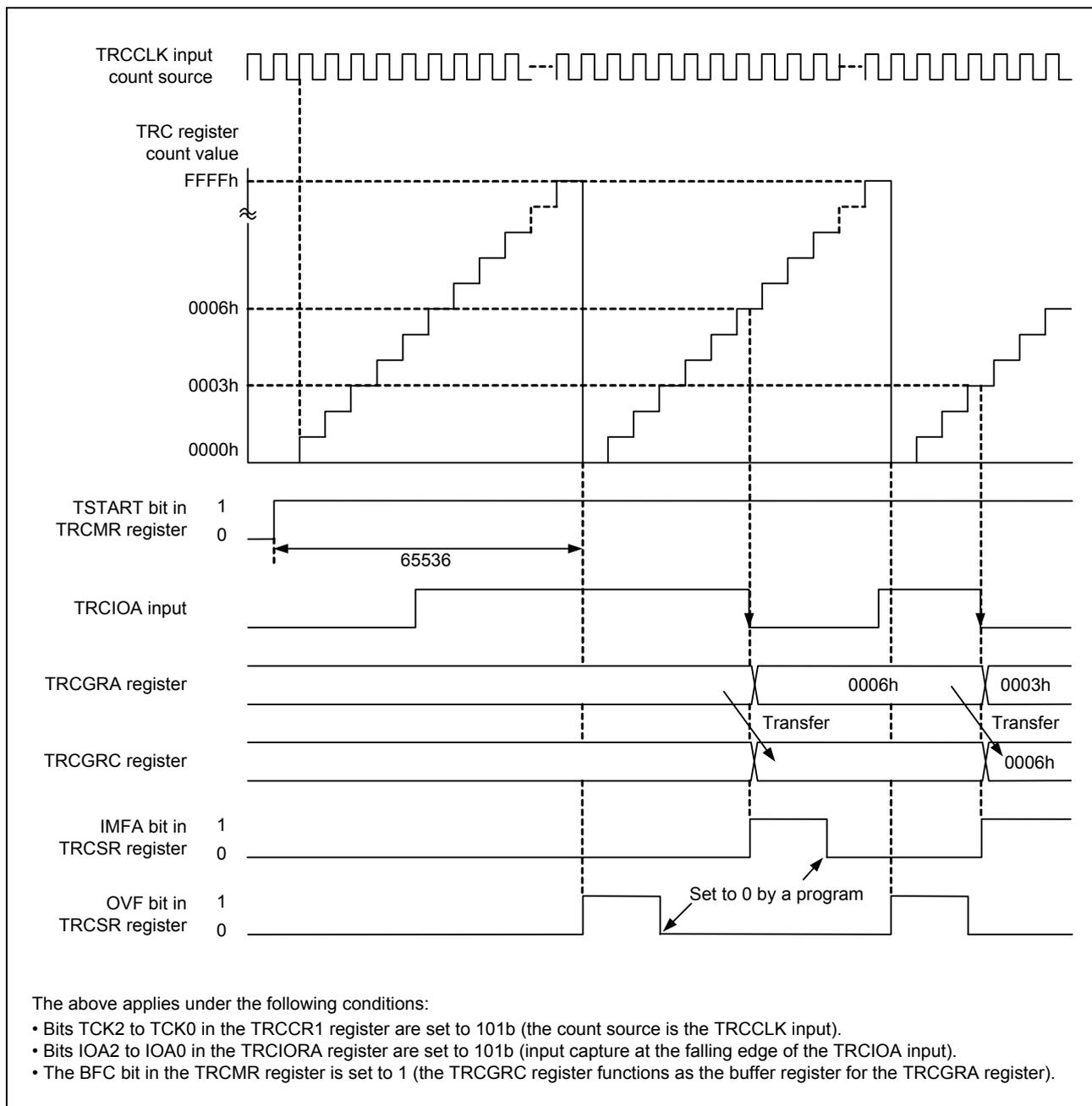


Figure 3.18 Operating Example of Input Capture Function

3.5 Timer RC Interrupt

Timer RC generates a timer RC interrupt request from five sources. The timer RC interrupt uses a single TRCIC register (bits IR and ILVL0 to ILVL2) and a single vector.

Table 3.8 lists the Registers Associated with Timer RC Interrupt, and Figure 3.19 is a Timer RC Interrupt Block Diagram.

Table 3.8 Registers Associated with Timer RC Interrupt

Timer RC Status Register	Timer RC Interrupt Enable Register	Timer RC Interrupt Control Register
TRCSR0	TRCIER	TRCIC

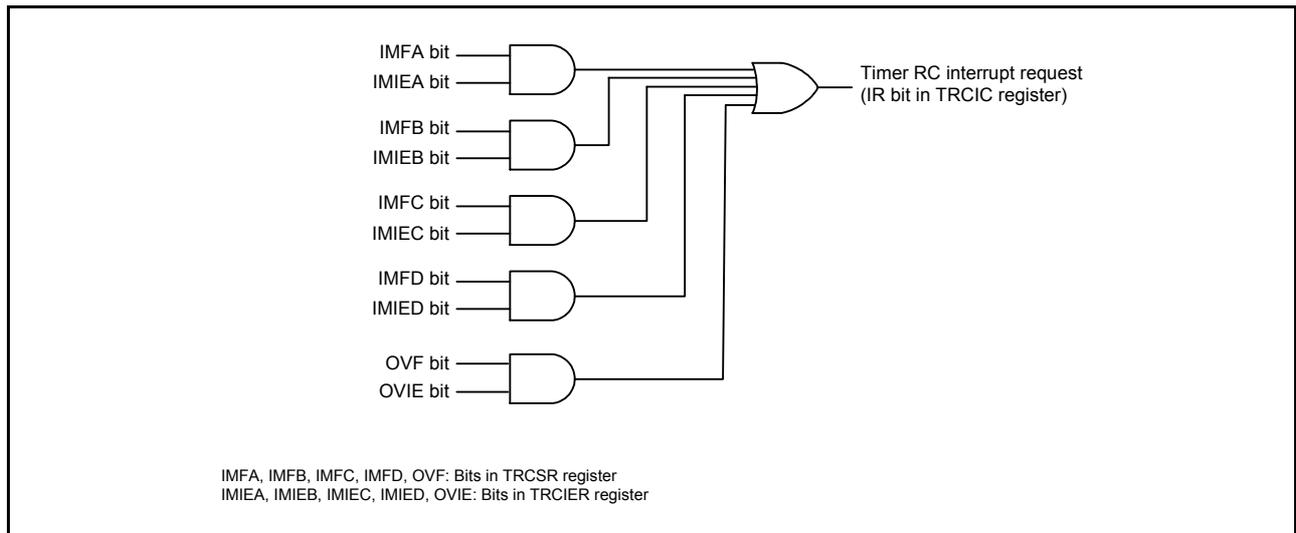


Figure 3.19 Timer RC Interrupt Block Diagram

Like other maskable interrupts, the timer RC interrupt is controlled by the combination of the I flag, IR bit, bits ILVL0 to ILVL2, and IPL. However, it differs from other maskable interrupts in the following respects because a single interrupt source (timer RC interrupt) is generated from multiple interrupt request sources.

- The IR bit in the TRCIC register is set to 1 (interrupt requested) when a bit in the TRCSR register is set to 1 and the corresponding bit in the TRCIER register is also set to 1 (interrupt enabled).
- The IR bit is set to 0 (no interrupt request) when the bit in the TRCSR register or the corresponding bit in the TRCIER register is set to 0, or both are set to 0. In other words, the interrupt request is not maintained if the IR bit is once set to 1, but the interrupt is not acknowledged.
- If after the IR bit is set to 1, another interrupt source is triggered, the IR bit remains set to 1 and does not change.
- If multiple bits in the TRCIER register are set to 1, use the TRCSR register to determine the source of the interrupt request.
- The bits in the TRCSR register are not automatically set to 0 when an interrupt is acknowledged. Set them to 0 within the interrupt routine. Refer to **Figure 3.5 TRCSR Register** for the procedure for setting these bits to 0.

Refer to **Figure 3.4 TRCIER Register** for details on the TRCIER register.

Refer to the **R8C/27 Group Hardware Manual** for details on the TRCIC register and for information on interrupt vectors.

3.6 Notes on Timer RC

3.6.1 TRC Register

- The following note applies when the CCLR bit in the TRCCR1 register is set to 1 (clear TRC register at compare match with TRCGRA register).

When using a program to write a value to the TRC register while the TSTART bit in the TRCMR register is set to 1 (count starts), ensure that the write does not overlap with the timing with which the TRC register is set to 0000h.

If the timing of the write to the TRC register and the setting of the TRC register to 0000h coincide, the write value will not be written to the TRC register and the TRC register will be set to 0000h.

- Reading from the TRC register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```

Program Example      MOV.W      #XXXXh, TRC          ;Write
                    JMP.B      L1              ;JMP.B instruction
                    L1:      MOV.W      TRC,DATA      ;Read

```

3.6.2 TRCSR Register

Reading from the TRCSR register immediately after writing to it can result in the value previous to the write being read out. To prevent this, execute the JMP.B instruction between the read and the write instructions.

```

Program Example      MOV.B      #XXh, TRCSR        ;Write
                    JMP.B      L1              ;JMP.B instruction
                    L1:      MOV.B      TRCSR,DATA   ;Read

```

3.6.3 Count Source Switching

- Stop the count before switching the count source.

Switching procedure:

- Set the TSTART bit in the TRCMR register to 0 (count stops).
- Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.

- After switching the count source from fOCO40M to another clock, allow a minimum of two cycles of f1 to elapse after changing the clock setting before stopping fOCO40M.

Switching procedure:

- Set the TSTART bit in the TRCMR register to 0 (count stops).
- Change the settings of bits TCK2 to TCK0 in the TRCCR1 register.
- Wait for a minimum of two cycles of f1.
- Set the FRA00 bit in the FRA0 register to 0 (high-speed on-chip oscillator off).

3.6.4 Input Capture Function

- The pulse width of the input capture signal should be three cycles or more of the timer RC operation clock (refer to Table 3.1 Timer RC Operation Clock).
- The value of the TRC register is transferred to the TRCGRj register one or two cycles of the timer RC operation clock after the input capture signal is input to the TRCIOj (j = A, B, C, or D) pin (when the digital filter function is not used).

4. Program Overview

When an active edge is detected on the external signal input to the TRCIOA pin (IMFA bit = 1), the contents of both the general (TRCGRA) and buffer (TRCGRC) registers will be read during main handling.

The setting conditions of this program are as follows:

- Select the high-speed on-chip oscillator (fOCOM40M) as count source.
- Detect an input capture to the TRCIOA pin at both edges.
- Retain the count value of timer RC counter (TRC) when an active edge is detected.

Figure 4.1 shows the Pin Used.

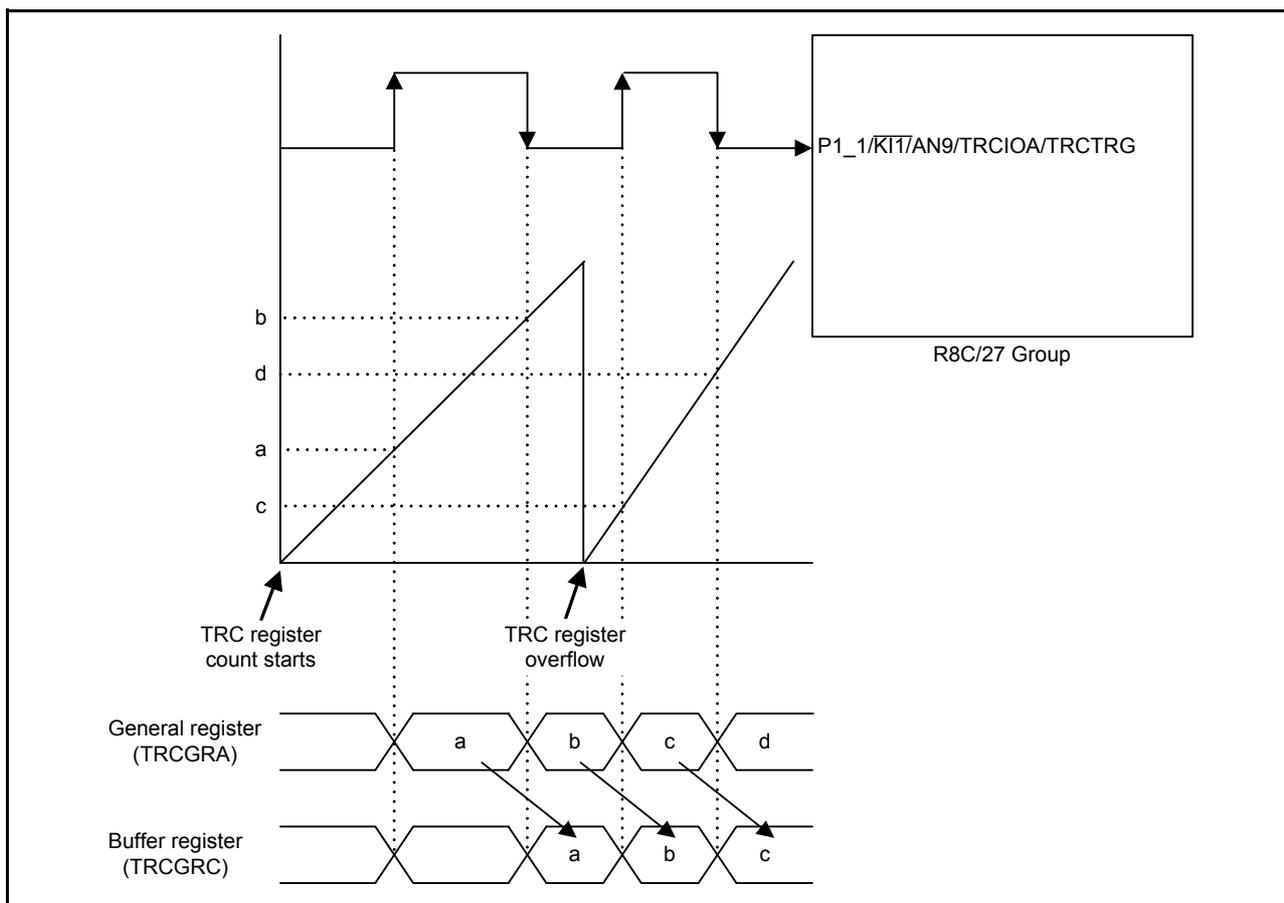


Figure 4.1 Pin Used

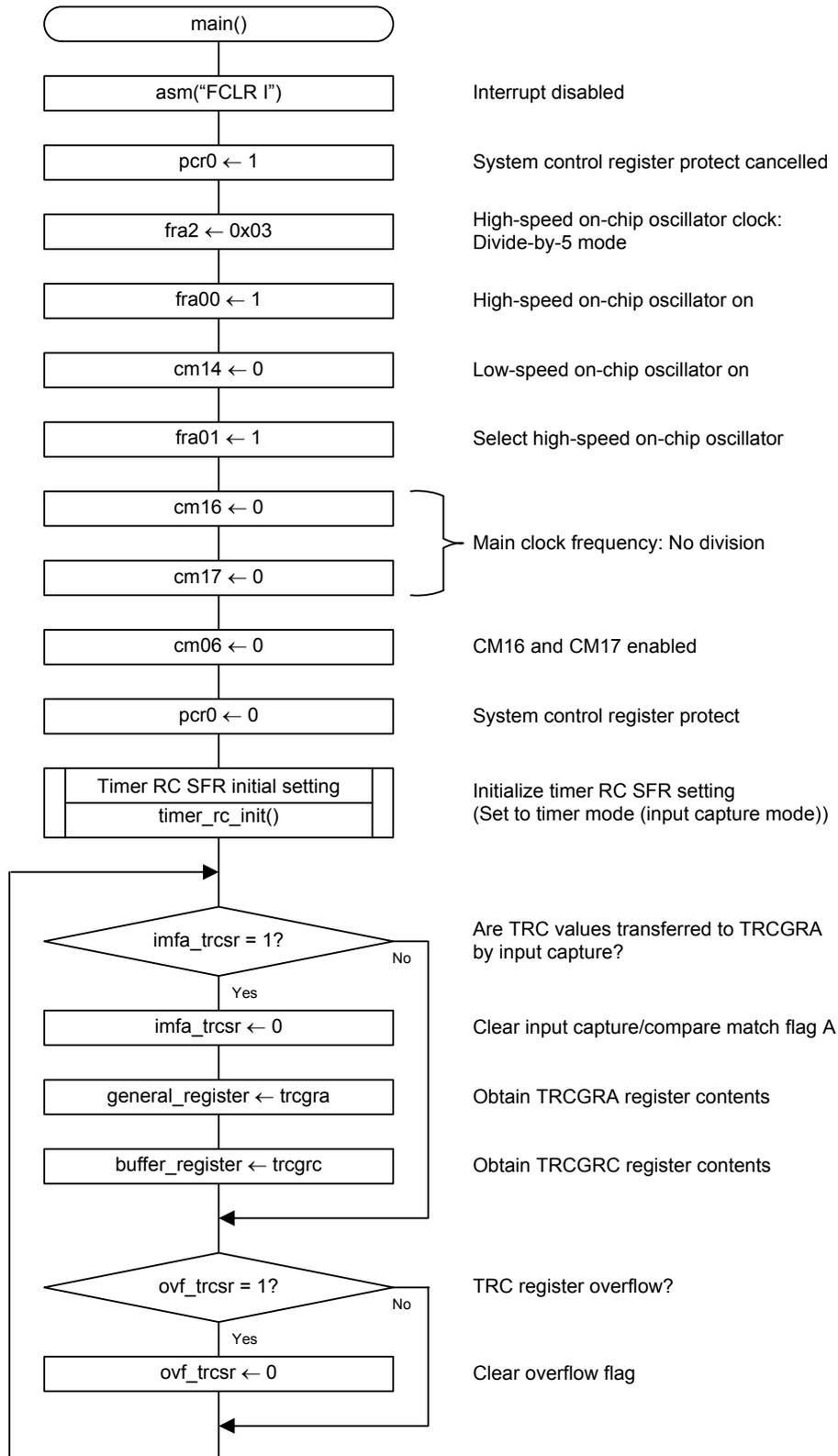
4.1 Function Table

Table 4.1

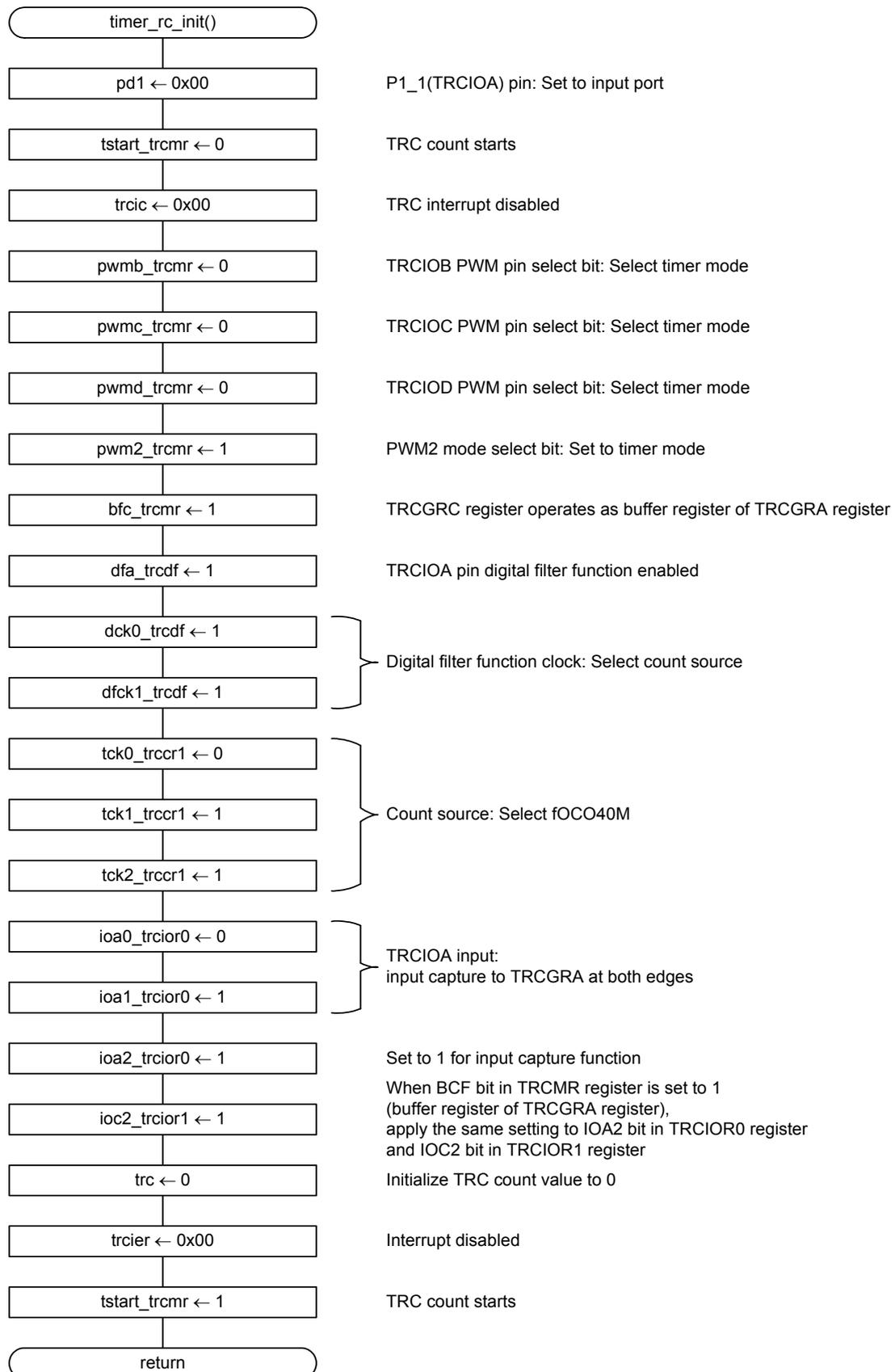
Declaration	void timer_rc_init(void)		
Overview	SFR initial setting associated with timer RC		
Argument	Argument name	Meaning	
	None		
Variable used (global)	Variable name	Usage	
	None		
Return value	Type	Value	Meaning
	None		
Function	Initialize the SFR registers associated with timer RC		

4.2 Flow chart

4.2.1 Main Function



4.2.2 Timer RC SER Initial Setting



5. Sample Programming Code

A sample program can be downloaded from the Renesas Electronics website.

6. Reference Documents

User's Manual: Hardware

R8C/27 Group Hardware Manual

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website

<http://www.renesas.com>

Inquiries

<http://www.renesas.com/contact/>

REVISION HISTORY	R8C/27 Group Timer RC in Input Capture Function
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Rev.	Date	Description	
		Page	Summary
1.00	Dec 01, 2006	–	First Edition issued
1.10	June 1, 2012	1	Note on oscillation stabilization wait time added
		–	Previous document number: REJ05B0837

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

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