R8C/38C Group

Serial I/O Operation (Clock Synchronous Serial I/O Mode)

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1. Abstract

This document describes the setting method and an application example for transmitting and receiving 10-byte data continuously using clock synchronous serial I/O mode in the R8C/38C Group.

2. Introduction

The application example described in this document applies to the following microcomputer (MCU):

- MCU: R8C/38C Group

This application note can be used with other R8C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

3.1 Program Outline

Transmit and receive 10-byte data continuously in 1-byte units every 250 µs. Transmit and receive 10-byte data again after 1 ms after transmitting and receiving 10-byte data. During a single 3.5 ms cycle, repeatedly transmit and receive 10-byte data.

Settings

- Use the P1_4/TXD0 pin for serial data output.
- Use the P1_5/RXD0 pin for serial data input.
- Use the P1_6/CLK0 pin for transfer clock output.
- Use the P1_4/TXD0 pin for CMOS output.
- Use UART0 for the channel.
- Use clock synchronous serial I/O mode.
- Use the internal clock for the transfer clock.
- Use LSB first for the transfer format.
- Select the transmit data output at the falling edge and the receive data input at the rising edge of the transfer clock for CLK polarity.
- Set 125000 bps (transfer clock: 8 µs period) as the bit rate.
- Use f8 for the BRG count source.
- Use timer RA to generate the transmission/reception period.
- Disable continuous receive mode.
- Do not use the UART0 transmit interrupt or UART0 receive interrupt.

Bit rate calculation
125000 bps = 20 MHz × 1/8 × 1/(9+1) × 1/2

Figure 3.1 shows a Block Diagram and Figure 3.2 shows a Transfer Format. Table 3.1 lists the pins used and their functions.

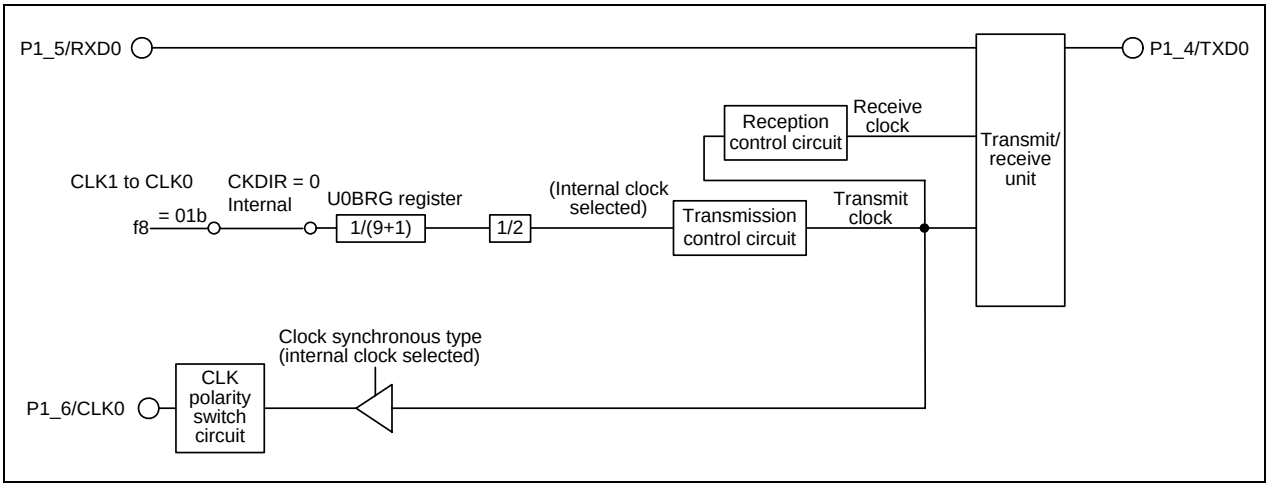


Figure 3.1 Block Diagram

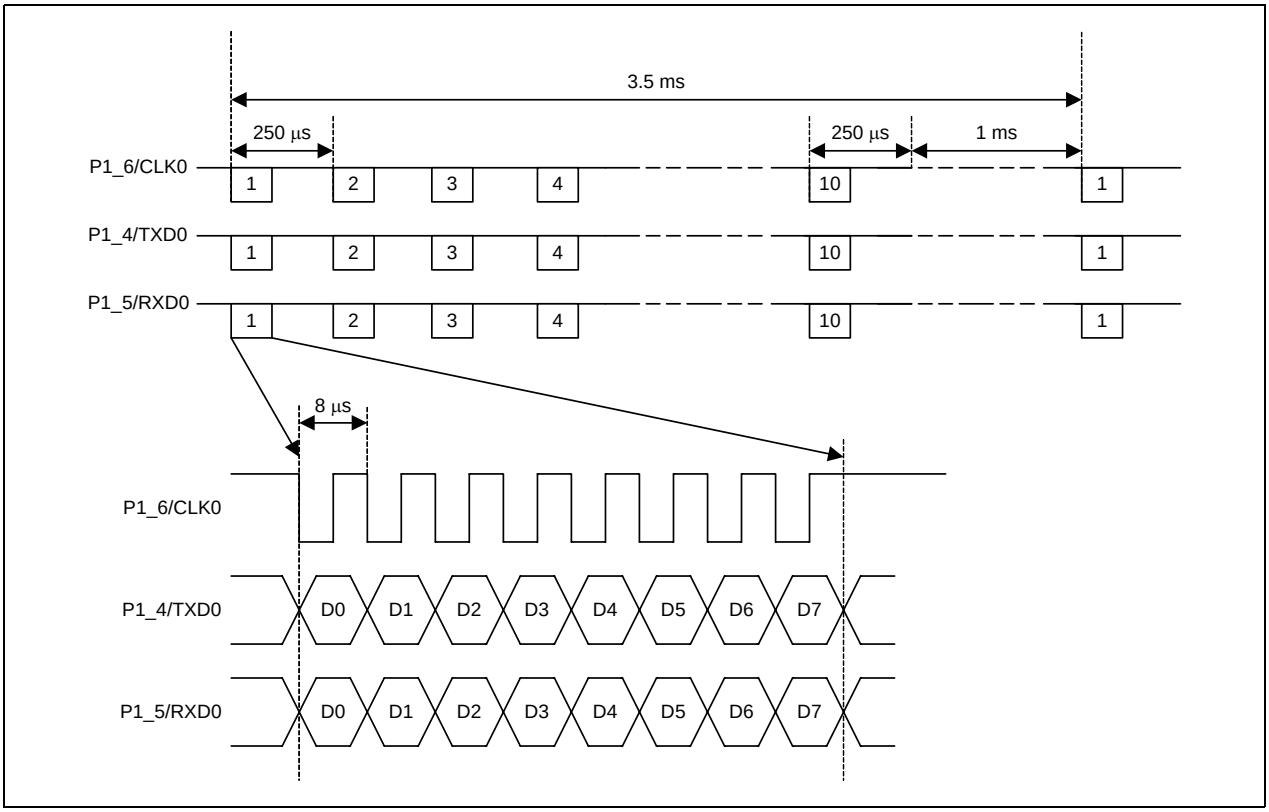


Figure 3.2 Transfer Format

Table 3.1 Pins and Their Functions

Pin Name	I/O	Function
P1_4/TXD0	Output	Serial data output
P1_5/RXD0	Input	Serial data input
P1_6/CLK0	Output	Transfer clock output

3.2 Memory

Table 3.2 Memory

Memory	Size	Remarks
ROM	247 bytes	In the rej05b1302_src.c module
RAM	21 bytes	In the rej05b1302_src.c module
Maximum user stack	13 bytes	
Maximum interrupt stack	0 bytes	

Memory size varies depending on the C compiler version and compile options.
The above applies to the following conditions:
C compiler: M16C/60, 30, 20, 10, and Tiny and R8C/Tiny Series Compiler V.5.45 Release 00
Compile option: -c -finfo -dir “$(CONFIGDIR)” -R8C

4. Software

This section shows the initial setting procedures and values to set the example described in section **3. Application Example**. Refer to the latest **R8C/38C Group hardware user's manual** for details on individual registers.

The × in the register's Setting Value represents bits not used in this application, blank spaces represent bits that do not change, and the dash represents reserved bits or bits that have nothing assigned.

4.1 Function Tables

Declaration	void mcu_init(void)		
Outline	System clock setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the system clock (high-speed on-chip oscillator).		

Declaration	void timer_ra_init(void)		
Outline	Timer RA associated SFR initial setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Perform the initial setting for the SFR register to use timer RA in timer mode.		

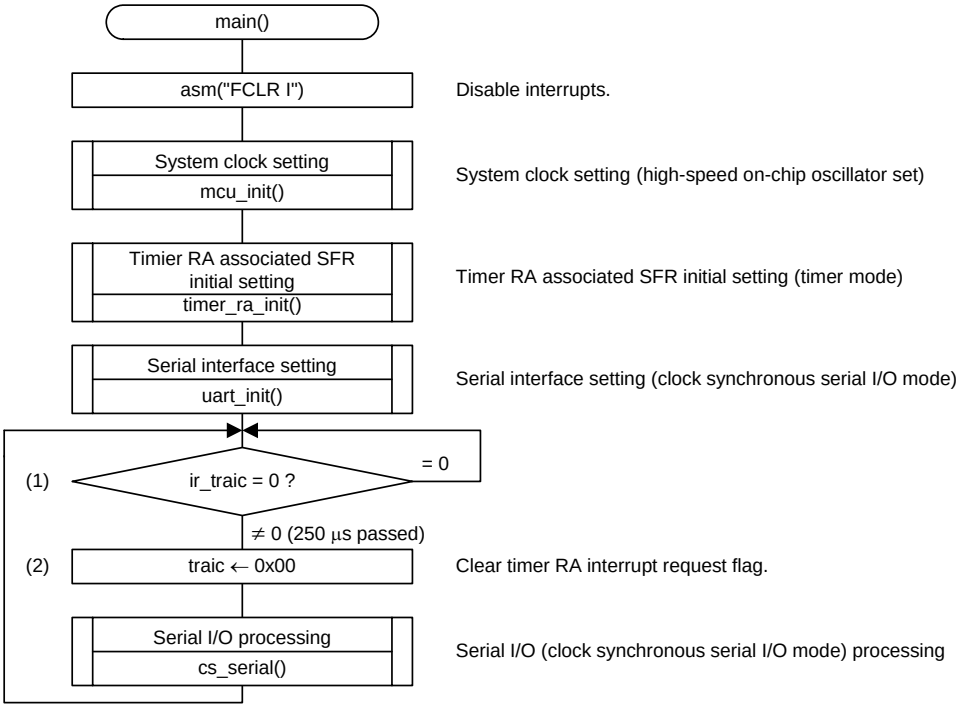
Declaration	void uart_init(void)		
Outline	Serial interface setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Set the serial interface (clock synchronous serial I/O mode).		

Declaration	void transmit_data_set(void)		
Outline	Transmit data setting		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	None		—
Returned value	Type	Value	Meaning
	None	—	—
Function	Make the transmit data. No processing is performed in this application note. Add processing based on the user system.		

Declaration	void cs_serial(void)		
Outline	Serial I/O (clock synchronous serial I/O mode) processing		
Argument	Argument name		Meaning
	None		—
Variable (global)	Variable name		Contents
	unsigned char serial_cnt		Transmit/receive data counter
	unsigned char rcv_buf[BUFF_SIZE]		Receive buffer
	unsigned char trn_buf[BUFF_SIZE]		Transmit buffer
Returned value	Type	Value	Meaning
	None	—	—
Function	Transmit and receive 10-byte data continuously in 1-byte units every 250 μs.		

4.2 Main Function

• Flowchart



• Register settings

(1) Wait until the timer RA interrupt request is generated.

Interrupt Control Register (TRAIC)

Bit	Symbol	Bit Name	Function	R/W
b3	IR	Interrupt request bit	0: No interrupt requested 1: Interrupt requested	R/W

(2) Clear the timer RA interrupt request flag.

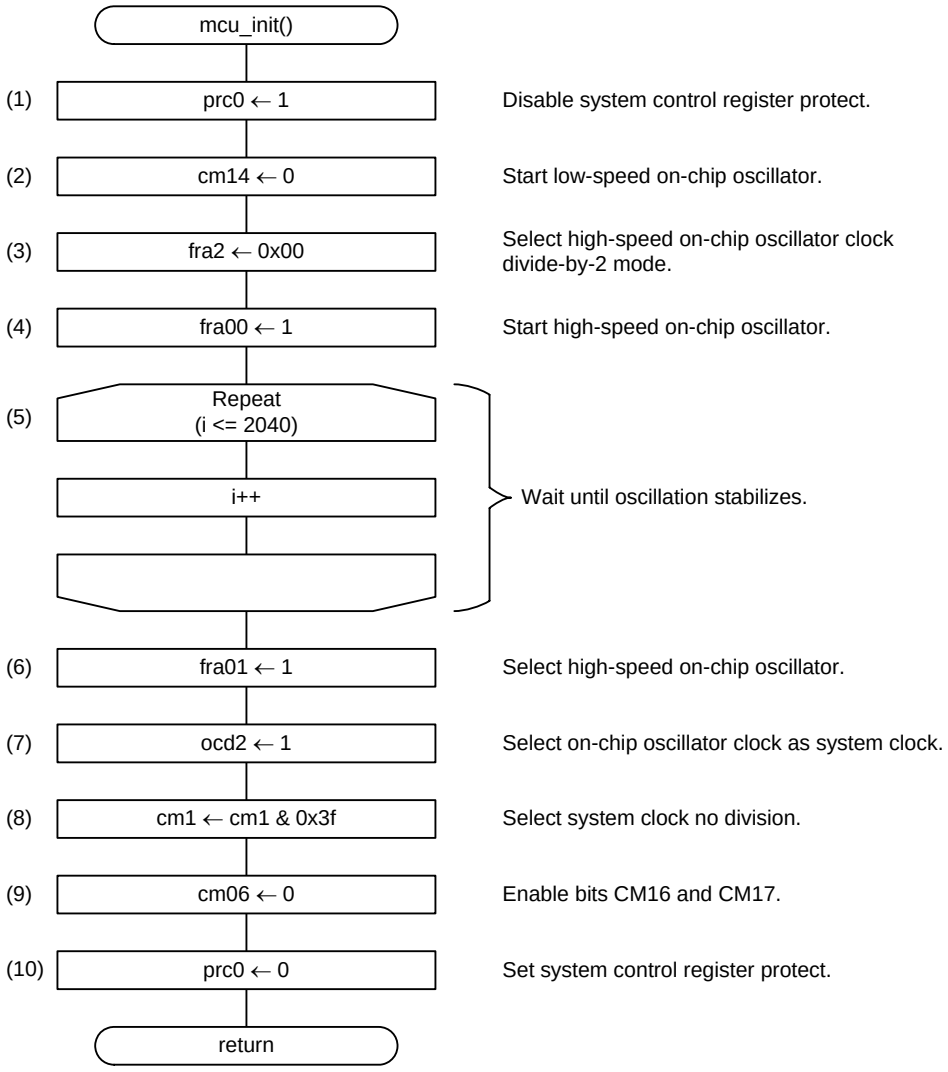
Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

4.3 System Clock Setting

• Flowchart



• Register settings

(1) Enable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	1

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 1: Write enabled	R/W

(2) Start the low-speed on-chip oscillator.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value			—	0	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b4	CM14	Low-speed on-chip oscillator stop bit	0: Low-speed on-chip oscillator on	R/W

(3) Set the division ratio for the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 2 (FRA2)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	FRA20	High-speed on-chip oscillator frequency switching bit	Division selection These bits select the division ratio for the high-speed on-chip oscillator clock. b2 b1 b0 0 0 0: Divide-by-2 mode	R/W
b1	FRA21			R/W
b2	FRA22			R/W

(4) Start the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—		1

Bit	Symbol	Bit Name	Function	R/W
b0	FRA00	High-speed on-chip oscillator enable bit	1: High-speed on-chip oscillator on	R/W

(5) Wait until oscillation stabilizes.

(6) Select the high-speed on-chip oscillator.

High-Speed On-Chip Oscillator Control Register 0 (FRA0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	—	1	

Bit	Symbol	Bit Name	Function	R/W
b1	FRA01	High-speed on-chip oscillator select bit	1: High-speed on-chip oscillator selected	R/W

(7) Select the on-chip oscillator clock as the system clock.

Oscillation Stop Detection Register (OCD)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	1	x	x

Bit	Symbol	Bit Name	Function	R/W
b2	OCD2	System clock select bit	1: On-chip oscillator clock selected	R/W

(8) Set system clock register 1.

System Clock Control Register 1 (CM1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	—		x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b6	CM16	CPU clock division select bit 1	b7 b6 0 0: No division mode	R/W
b7	CM17			R/W

(9) Set system clock control register 0.

System Clock Control Register 0 (CM0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	0	x	x	x	x	—	—

Bit	Symbol	Bit Name	Function	R/W
b6	CM06	CPU clock division select bit 0	0: Bits CM16 and CM17 in CM1 register enabled	R/W

(10) Disable writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3.

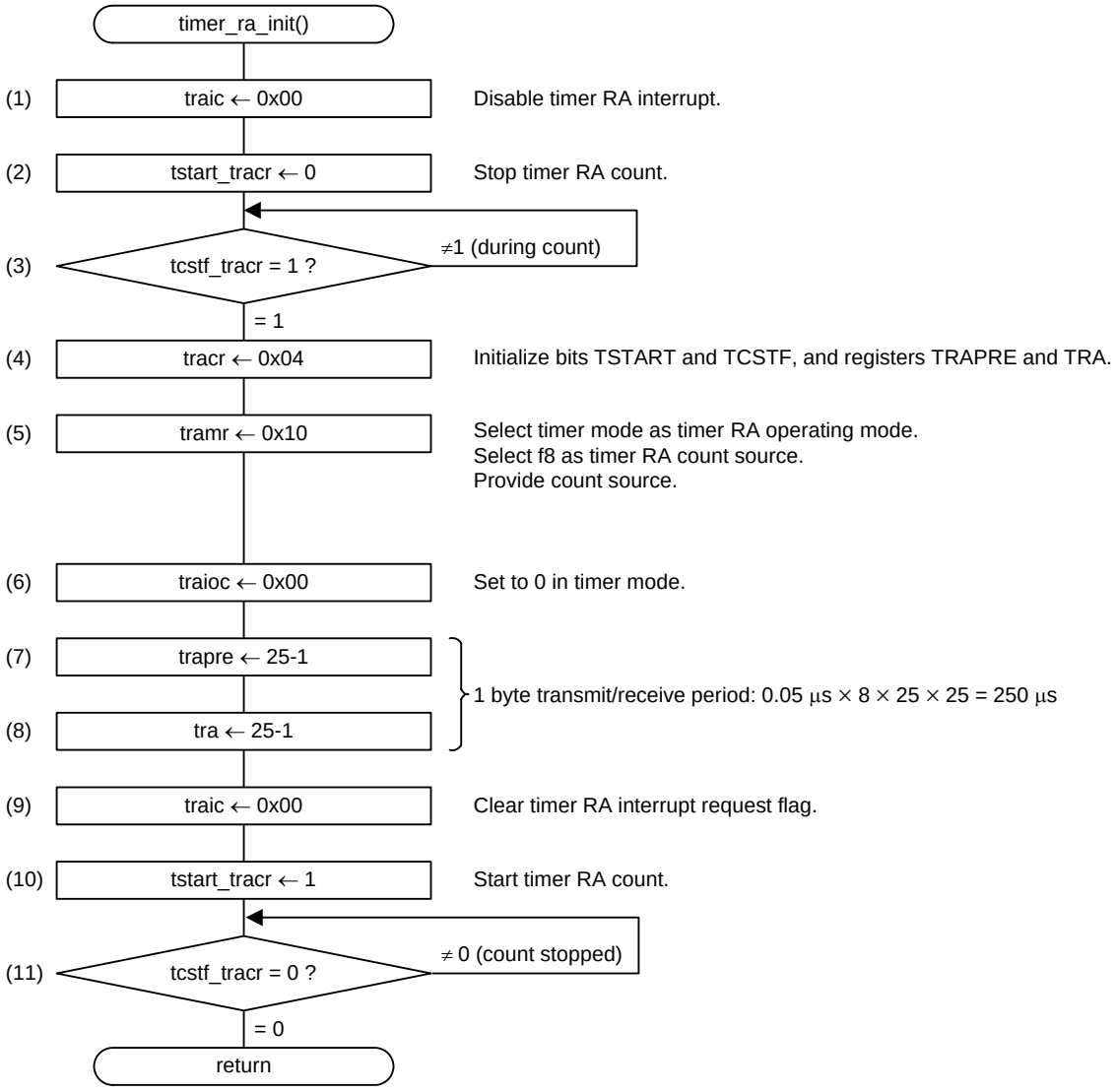
Protect Register (PRCR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	x	x	x	0

Bit	Symbol	Bit Name	Function	R/W
b0	PRC0	Protect bit 0	Enables writing to registers CM0, CM1, CM3, OCD, FRA0, FRA1, FRA2, and FRA3. 0: Write disabled	R/W

4.4 Timer RA Associated SFR Initial Setting

• Flowchart



• Register settings

(1) Disable the timer RA interrupt.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(2) Stop the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W

(3) Wait until the timer RA count stops.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count operation	R

(4) Initialize bits TSTART and TCSTF, and registers TRAPRE and TRA.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	0	—	1		0

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	0: Count stops	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count	R
b2	TSTOP	Timer RA count forcible stop bit	When this bit is set to 1, the count is forcibly stopped. When read, the content is 0.	R/W
b4	TEDGF	Active edge judgment flag	0: Active edge not received	R/W
b5	TUNDF	Timer RA underflow flag	0: No underflow	R/W

(5) Set the timer RA mode register.

Timer RA Mode Register (TRAMR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	1	—	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TMOD0	Timer RA operating mode select bit	b2 b1 b0 0 0 0: Timer mode	R/W
b1	TMOD1			R/W
b2	TMOD2			R/W
b4	TCK0	Timer RA count source select bit	b6 b5 b4 0 0 1: f8	R/W
b5	TCK1			R/W
b6	TCK2			R/W
b7	TCKCUT	Timer RA count source cutoff bit	0: Provides count source	R/W

(6) Set the timer RA I/O control register.

Timer RA I/O Control Register (TRAIOC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	TEDGSEL	TRAIO polarity switch bit	Set to 0 in timer mode.	R/W
b1	TOPCR	TRAIO output control bit		R/W
b2	TOENA	TRAO output enable bit		R/W
b3	TIOSEL	Hardware LIN function select bit	Set to 0. However, set to 1 when the hardware LIN function is used.	R/W
b4	TIPF0	TRAIO input filter select bit	Set to 0 in timer mode.	R/W
b5	TIPF1			R/W
b6	TIOGT0	TRAIO event input control bit		R/W
b7	TIOGT1			R/W

(7) Set the timer RA prescaler register to 25-1 (18h).

Timer RA Prescaler Register (TRAPRE)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	1	1	0	0	0

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts an internal count source	00h to FFh	R/W

(8) Set the timer RA register to 25-1 (18h).

Timer RA Register (TRA)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	1	1	0	0	0

Bit	Mode	Function	Setting Range	R/W
b7 to b0	Timer mode	Counts on underflow of TRAPRE register	00h to FFh	R/W

(9) Clear the timer RA interrupt request flag.

Interrupt Control Register (TRAIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(10) Start the timer RA count.

Timer RA Control Register (TRACR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—			—			1

Bit	Symbol	Bit Name	Function	R/W
b0	TSTART	Timer RA count start bit	1: Count starts	R/W

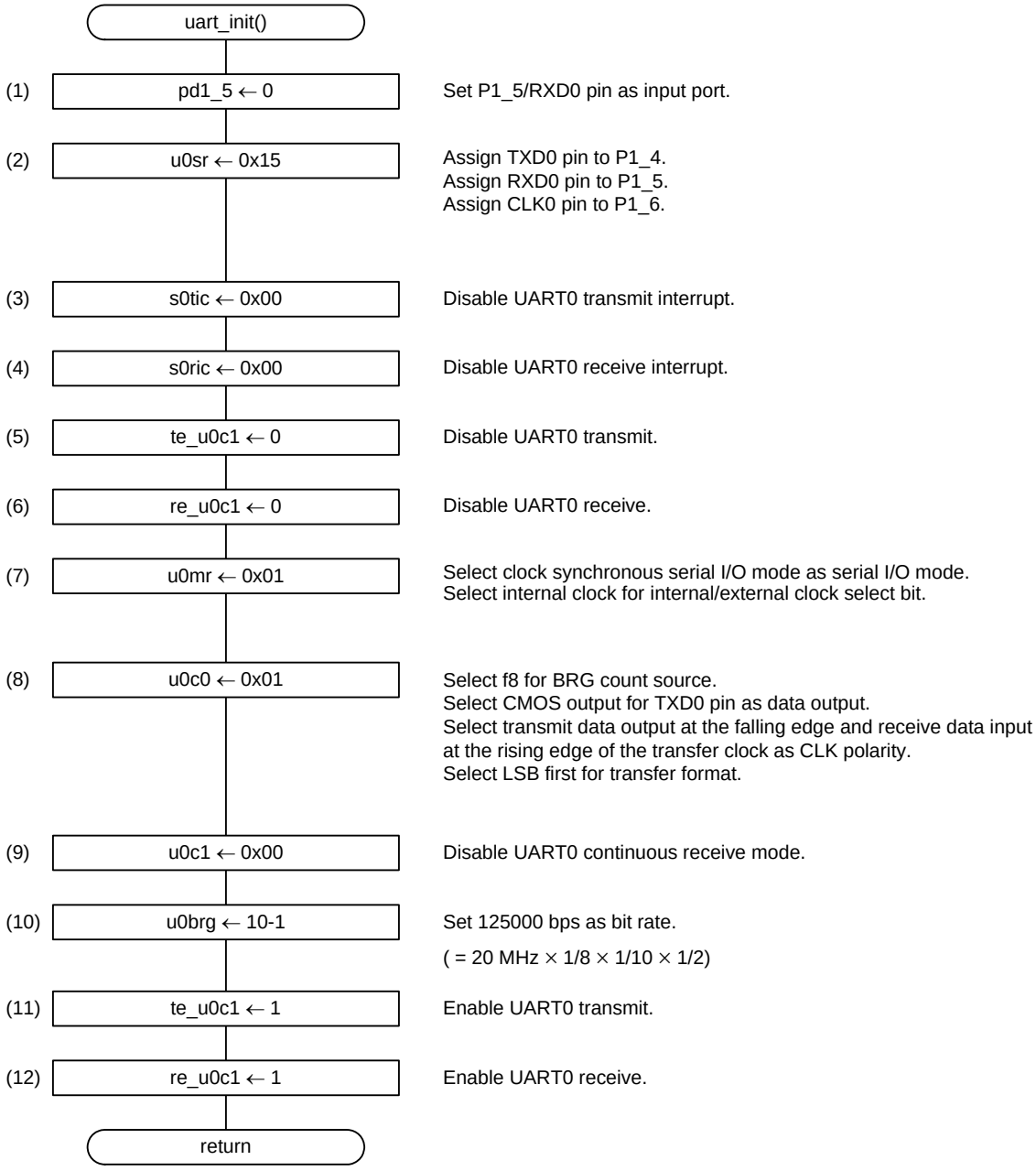
(11) Wait until the timer RA count starts.

Timer RA Control Register (TRACR)

Bit	Symbol	Bit Name	Function	R/W
b1	TCSTF	Timer RA count status flag	0: Count stops 1: During count operation	R

4.5 Serial Interface Setting

• Flowchart



• Register settings

(1) Set P1_5 as input mode.

Port P1 Direction Register (PD1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	0	x	x	x	x	x

Bit	Symbol	Bit Name	Function	R/W
b5	PD1_5	Port P1_5 direction bit	0: Input mode (functions as an input port)	R/W

(2) Set the TXD0 pin as port P1_4, the RXD0 pin as port P1_5, and the CLK0 pin as port P1_6.

UART0 Pin Select Register (U0SR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	1	—	1	—	1

Bit	Symbol	Bit Name	Function	R/W
b0	TXD0SEL0	TXD0 pin select bit	1: P1_4 assigned	R/W
b2	RXD0SEL0	RXD0 pin select bit	1: P1_5 assigned	R/W
b4	CLK0SEL0	CLK0 pin select bit	1: P1_6 assigned	R/W

(3) Disable the UART0 transmit interrupt.

Interrupt Control Register (S0TIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(4) Disable the UART0 receive interrupt.

Interrupt Control Register (S0RIC)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	—	—	0	0	0	0

Bit	Symbol	Bit Name	Function	R/W
b0	ILVL0	Interrupt priority level select bit	b2 b1 b0 0 0 0: Level 0 (interrupt disabled)	R/W
b1	ILVL1			R/W
b2	ILVL2			R/W
b3	IR	Interrupt request bit	0: No interrupt requested	R/W

(5) Disable the UART0 transmit.

UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—		x	x		x	0

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	0: Transmission disabled	R/W

(6) Disable the UART0 receive.

UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—		x	x	0	x	

Bit	Symbol	Bit Name	Function	R/W
b2	RE	Receive enable bit	0: Reception disabled	R/W

(7) Set the UART0 transmit/receive mode register.

UART0 Transmit/Receive Mode Register (U0MR)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	x	x	x	0	0	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	SMD0	Serial I/O mode select bit	b2 b1 b0 0 0 1: Clock synchronous serial I/O mode	R/W
b1	SMD1			R/W
b2	SMD2			R/W
b3	CKDIR	Internal/external clock select bit	0: Internal clock	R/W

(8) Set UART0 transmit/receive control register 0.

UART0 Transmit/Receive Control Register 0 (U0C0)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	—	x	—	0	1

Bit	Symbol	Bit Name	Function	R/W
b0	CLK0	BRG count source select bit	b1 b0 0 1: f8 selected	R/W
b1	CLK1			R/W
b5	NCH	Data output select bit	0: TXD0 pin set to CMOS output	R/W
b6	CKPOL	CLK polarity select bit	0: Transmit data output at the falling edge and receive data input at the rising edge of the transfer clock	R/W
b7	UFORM	Transfer format select bit	0: LSB first	R/W

(9) Disable UART0 continuous receive mode.

UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—	0	x	x		x	

Bit	Symbol	Bit Name	Function	R/W
b5	U0RRM	UART0 continuous receive mode enable bit	0: Continuous receive mode disabled	R/W

(10) Set the UART0 bit rate register. Set 125000 bps in this application note. Set 10-1 (09h) based on the following calculation:
125000 bps = 20 MHz × 1/8 × 1/10 × 1/2

UART0 Bit Rate Register (U0BRG)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0	0	0	0	1	0	0	1

Bit	Function	Setting Range	R/W
b7 to b0	If the setting value is n, U0BRG divides the count source by n+1.	00h to FFh	W

(11) Enable the UART0 transmit.

UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—		x	x		x	1

Bit	Symbol	Bit Name	Function	R/W
b0	TE	Transmit enable bit	1: Transmission enabled	R/W

(12) Enable the UART0 receive.

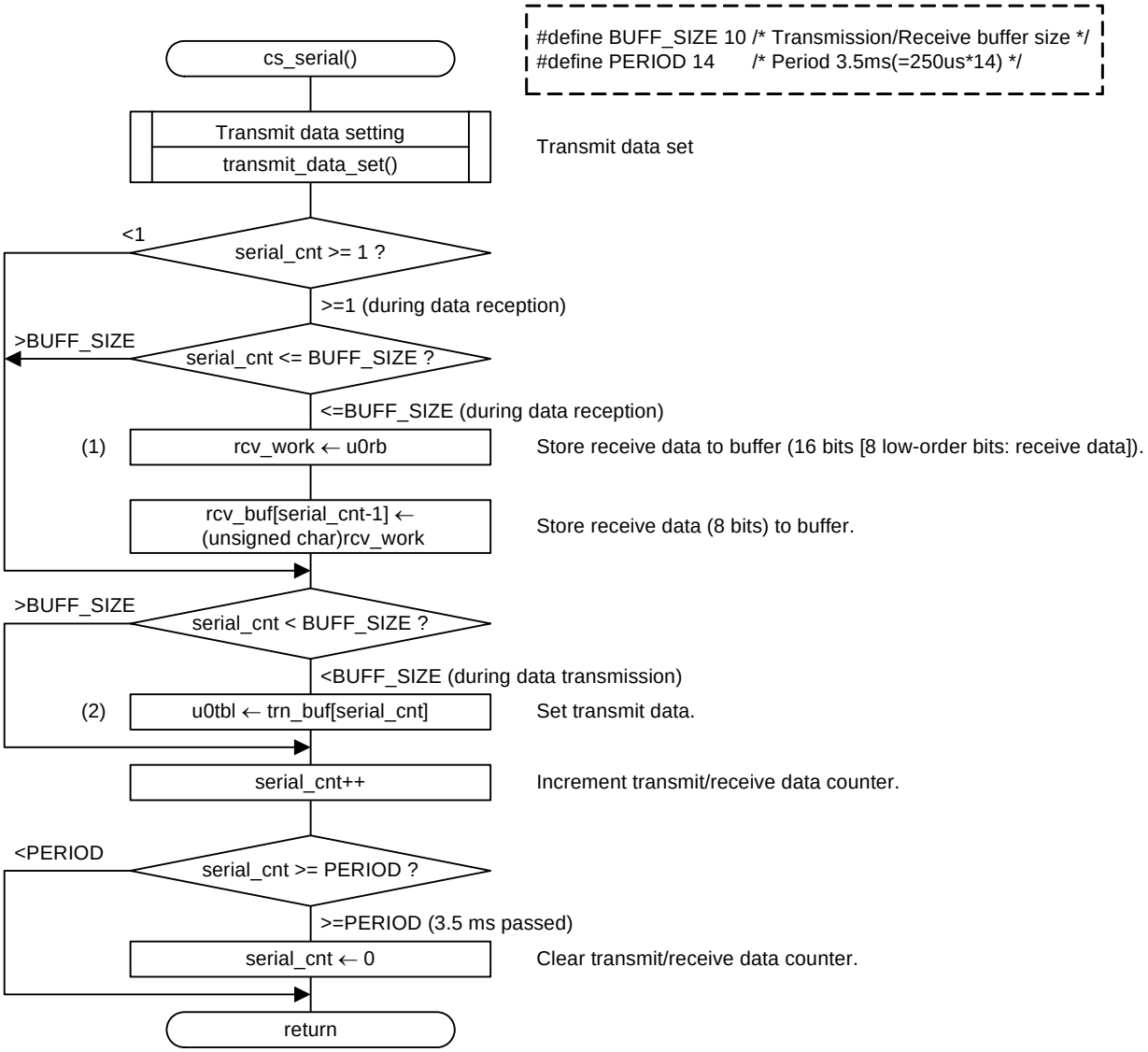
UART0 Transmit/Receive Control Register 1 (U0C1)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	—	—		x	x	1	x	

Bit	Symbol	Bit Name	Function	R/W
b2	RE	Receive enable bit	1: Reception enabled	R/W

4.6 Serial I/O (Clock Synchronous Serial I/O Mode) Processing

• Flowchart



• Register settings

(1) Read the receive data in the U0RB register.

UART0 Receive Buffer Register (U0RB)

Bit	Symbol	Bit Name	Function	R/W
b0	—	—	Receive data (D7 to D0)	R
b1	—			
b2	—			
b3	—			
b4	—			
b5	—			
b6	—			
b7	—			
b12	OER	Overrun error flag	0: No overrun error 1: Overrun error	R
b13	FER	Framing error flag	0: No framing error 1: Framing error	R
b14	PER	Parity error flag	0: No parity error 1: Parity error	R
b15	SUM	Error sum flag	0: No error 1: Error	R

(2) Set the transmit data to the low-order byte in the UART0 transmit buffer register.

UART0 Transmit Buffer Register (U0TB)

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

Bit	b7	b6	b5	b4	b3	b2	b1	b0
Setting Value	x	x	x	x	x	x	x	x

Bit	Symbol	Function	R/W
b0	—	Transmit data	W
b1	—		
b2	—		
b3	—		
b4	—		
b5	—		
b6	—		
b7	—		

5. Sample Program

A sample program can be downloaded from the Renesas Electronics website.
To download, click “Application Notes” in the left-hand side menu of the R8C Family page.

6. Reference Documents

R8C/38C Group User’s Manual: Hardware Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	R8C/38C Group Serial I/O Operation (Clock Synchronous Serial I/O Mode)

Rev.	Date	Description	
		Page	Summary
1.00	June 7, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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