RA Family, RL78 Family, RX Family, Renesas Synergy™ Platform

CTSU Self Test Software

Introduction

This application note explains the Functional safety solution for capacitive touch of Renesas Electronics.

Target Device

RA family

CTSU: RA2A1, RA4M1, RA4M2, RA4M3, RA4W1, RA6M1, RA6M2, RA6M3, RA6M4, RA6M5 Group

CTSU2: RA2L1, RA2E1 Group

RL78 Family

CTSUb: RL78/G16 Group

CTSU2L: RL78/G23 Group

CTSU2La: RL78/G22 Group

RX Family

CTSU: RX113, RX130, RX230, RX231, RX23W, RX671 Group

CTSU2SL: RX140 Group

Renesas Synergy™ Platform

Coming soon

Contents

1. Overview

Today, as automatic electronic controls systems continue to expand into many diverse applications, the requirement of reliability and safety are becoming an ever-increasing factor in system design. For example, the introduction of the IEC60730 safety standard for household appliances requires manufactures to design automatic electronic controls that ensure safe and reliable operation of their products.

1. Class A: Control functions, which are not intended to be relied upon for the safety of the equipment.

   Examples: Room thermostats, humidity controls, lighting controls, timers, and switches.

2. Class B: Control functions, which are intended to prevent unsafe operation of the controlled equipment.

   Examples: Thermal cut-offs and door locks for laundry equipment.

3. Class C: Control functions, which are intended to prevent special hazards.

   Examples: Automatic burner controls and thermal cut-outs for closed.

Appliances such as washing machines, dishwashers, dryers, refrigerators, freezers, and Cookers / Stoves will tend to fall under the classification of Class B.

This application note describes the CTSU diagnosis software and provides to assist with compliance with IEC60730 class B safety standards.

CTSU hardware can diagnose own internal circuit. This software controls the internal circuit and provides API to diagnose. This software implemented to Renesas RA family Flexible Software Package (FSP) V3.0.0 or later in part of the CTSU module. The diagnosis content is different between CTSU and CTSU2 hardware. This software provides five types of diagnostics for CTSU and nine types for CTSU2. Refer to section 2.CTSU diagnosis and section 3.CTSU2 diagnosis for detail. The diagnosis can be performed by calling API functions. Diagnosis is performed in addition to normal measurements. Refer to section 4.API specification and section 5.Flowchart of sample application for detail. When using the diagnosis function, it is recommended to output the config using “QE for Capacitive Touch”. By using QE, you can create a project, set a configuration, and output a sample application. Refer to section 6.Procedure for creating a project using “QE for Capacitive Touch” for the setting procedure and its details.

In addition, it is possible to accelerate the acquisition of IEC/UL60730 certification for final products which support capacitive touch by using "Renesas Functional Safety Solutions for Home Appliances" together.(It can also use your own program instead of Renesas Functional Safety Solutions for Home Appliances.)

2. CTSU Diagnosis

This chapter describes the following seven types of tests.

- Output Voltage Test
- Overvoltage Detection test
- Current Controlled Oscillator Test (19.2uA Correction Mode)
- Current Controlled Oscillator Test (2.4uA Correction Mode)
- SSCG Oscillator Test
- Current Offset DAC Test
- Current Offset DAC Test (without TS)

CTSU also includes CTSUb.

Current Offset DAC test requires a TS terminal with capacitor: 27pF connected*.
Note: CTSUb does not require a TS terminal with capacitor: 27pF connected.

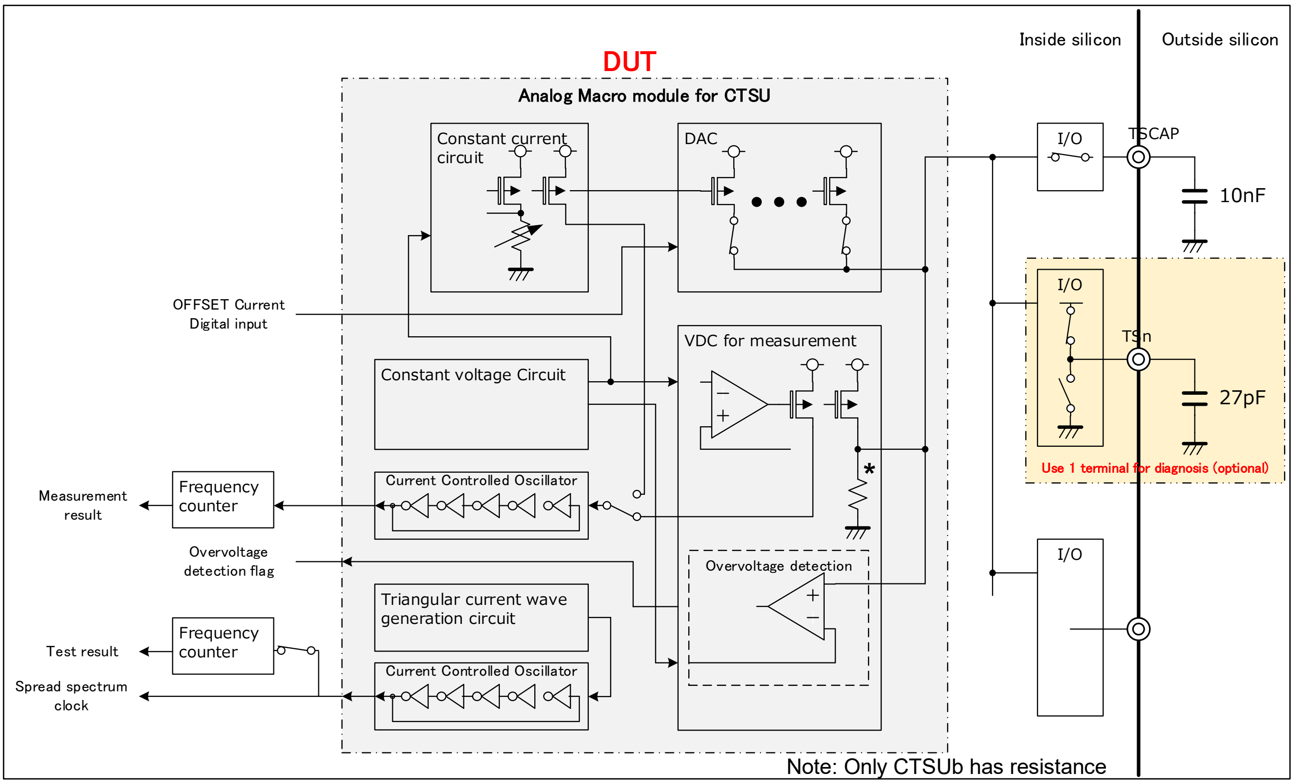

Figure 2.1 Circuits of CTSU Diagnosis

2.1 Output Voltage Test

Diagnose “Low drop output voltage down converter” (VDC) output voltage.
This test is for CTSUb other than CTSU.

Operation outline

(1) ADC module to the scan setting.

(2) Set CTSU power on.

(3) Set Self scan mode.

(4) Set SO value initialize.

(5) TSCAP voltage measurement by ADC for 4 times with following conditions.

- Set Load resistance 30k ohm and LDO output 40uA then measure TSCAP voltage by ADC.
- Set Load resistance 15k ohm and LDO output 40uA then measure TSCAP voltage by ADC.
- Set Load resistance 30k ohm and LDO output 80uA then measure TSCAP voltage by ADC.
- Set Load resistance 15k ohm and LDO output 80uA then measure TSCAP voltage by ADC.

(6) Store above measurement results to dedicated variables.

If stored measurement result is within the standard threshold value range, PASS the diagnosis.

If stored measurement result is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_OUTPUT_VOLTAGE.

2.2 Overvoltage Detection Test

Check ICOMP status while supplying current from Current Offset DAC for a certain period.

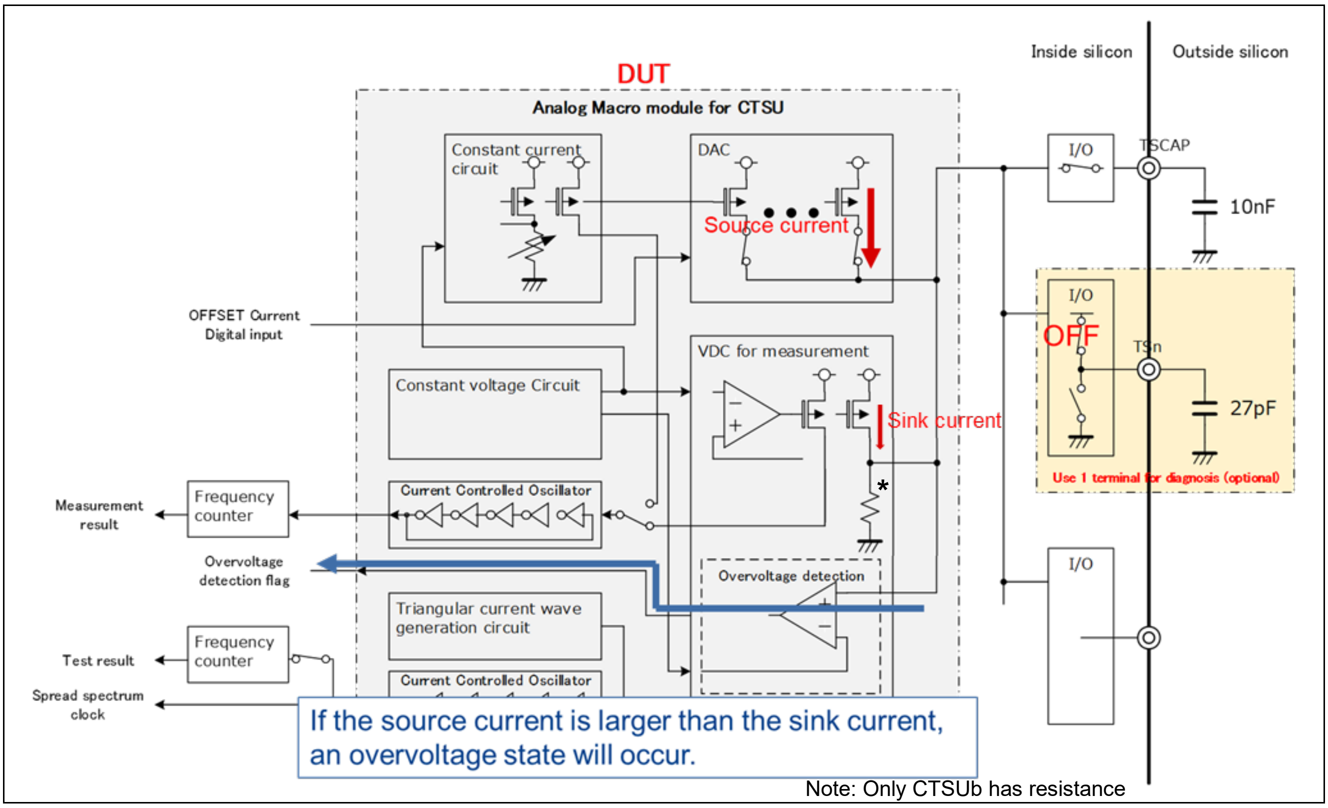

Figure 2.2 Circuits of Overvoltage Detection Test

CTSUICOMP: TSCAP Voltage Error Monitor BIT

CTSUSO0 : CTSU Sensor Offset Adjustment BIT

Operation outline

(1) Set CTSU power on.

(2) Synchronous Noise Reduction Setting.

(3) Set High Pass Noise Reduction.

(4) Set sensor Stabilization.

(5) Set CLK division.

(6) Set Self scan mode.

(7) Normal output IO = L fixed, sensor drive pulse output = Hi-z fixed.

(8) Start supplying a constant current from Current Offset DAC by setting “0x3FF” to CTSU register.

(9) CTSU Scan.

If “CTSUICOMP” = 1 in CTSUFN interrupt PASS the diagnosis.

If “CTSUICOMP” = 0 in CTSUFN interrupt, FAIL the diagnosis and return the FSP_ERR_CTSU_DIAG_LDO_OVER_VOLTAGE.

2.3 Current Controlled Oscillator Test (19.2uA Correction Mode)

Diagnose the frequency of Current Controlled Oscillator when 19.2uA correction mode.

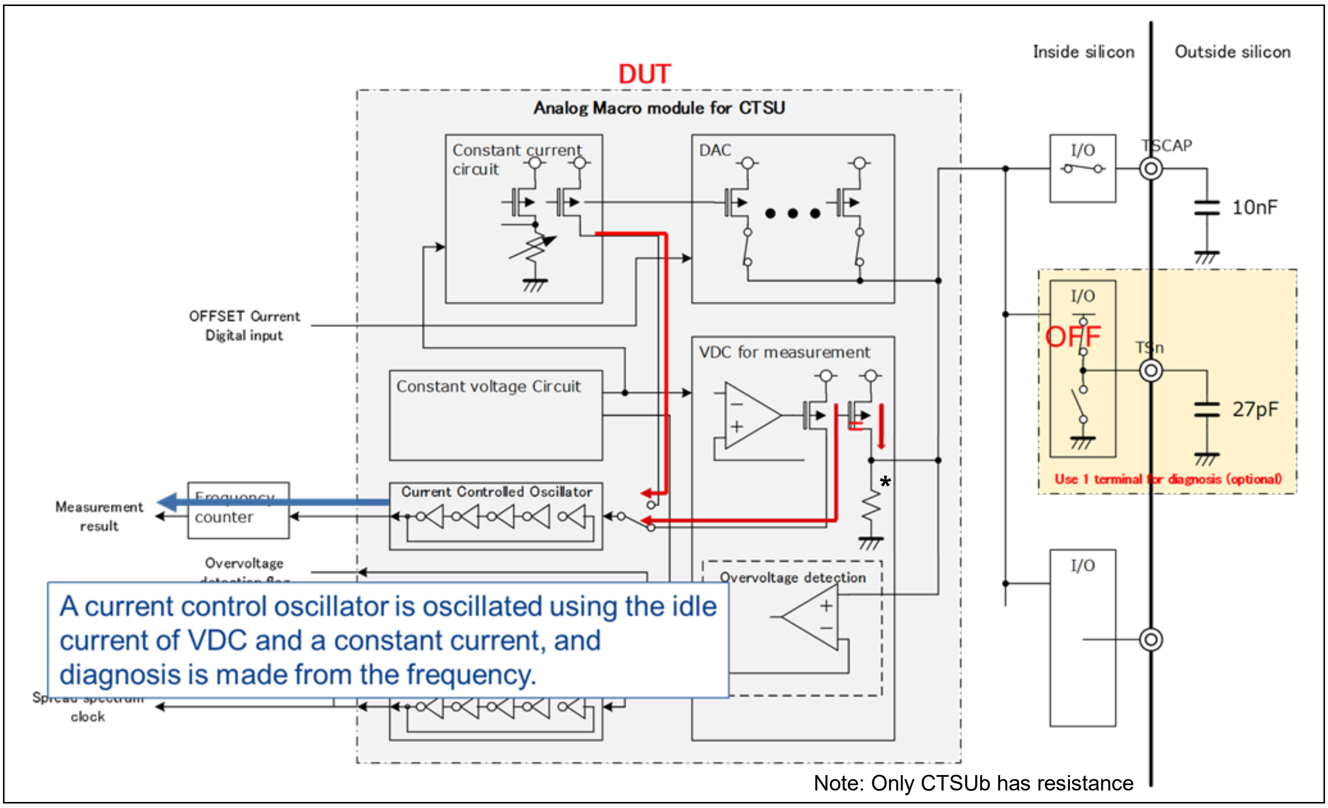

Figure 2.3 Circuits of Current Controlled Oscillator Test (19.2uA Correction Mode)

CTSUSPMD: Calibration Mode BIT (CTSUSPMD = 2 is Calibration Mode)

CTSUTSOC: Calibration Setting 2 BIT (CTSUTSOC = 1 is Calibration setting 2)

Operation outline

(1) Set CTSU power on.

(2) Synchronous Noise Reduction Setting.

(3) Set High Pass Noise Reduction.

(4) Set sensor Stabilization.

(5) Set CLK division.

(6) Set Self scan mode.

(7) Set CTSUSPMD = 2, CTSUTSOC = 1.

(8) CTSU scan for fixed 19.2uA setting.

(9) Store scan result to dedicated variables.

(10) If stored scan result is within the standard threshold value range, PASS the diagnosis.

If stored scan result is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_CCO_HIGH.

2.4 Current Controlled Oscillator Test (2.4uA Correction Mode)

Diagnose the frequency of Current Controlled Oscillator when 2.4uA correction mode.

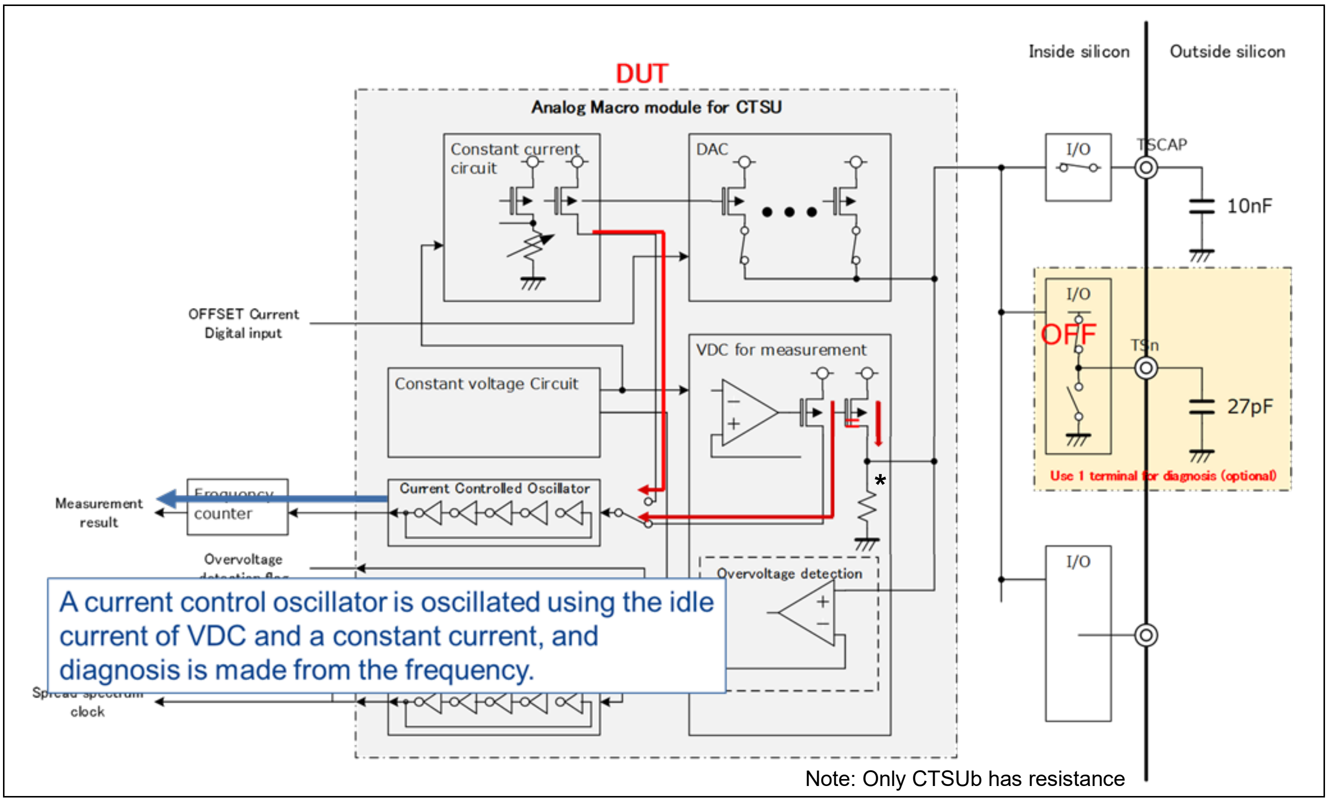

Figure 2.4 Circuits of Current Controlled Oscillator Test (2.4uA Correction Mode)

CTSUSPMD: Calibration Mode BIT (CTSUSPMD = 0 is Capacitance scan mode)

CTSUTSOC: Calibration Setting 2 BIT (CTSUTSOC = 1 is Calibration setting 2)

Operation outline

(1) Set CTSU power on.

(2) Synchronous Noise Reduction Setting.

(3) Set High Pass Noise Reduction.

(4) Set sensor Stabilization.

(5) Set CLK division.

(6) Set Self scan mode.

(7) Set CTSUSPMD = 0, CTSUTSOC = 1.

(8) CTSU scan for fixed 2.4uA setting.

(9) Store scan result to dedicated variables.

(10) If stored scan result is within the standard threshold value range, PASS the diagnosis.

If stored scan result is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_OSCILLATOR_LOW.

2.5 SSCG Oscillator Test

Diagnose the output frequency of SSCG (Spread Spectrum) Oscillator.

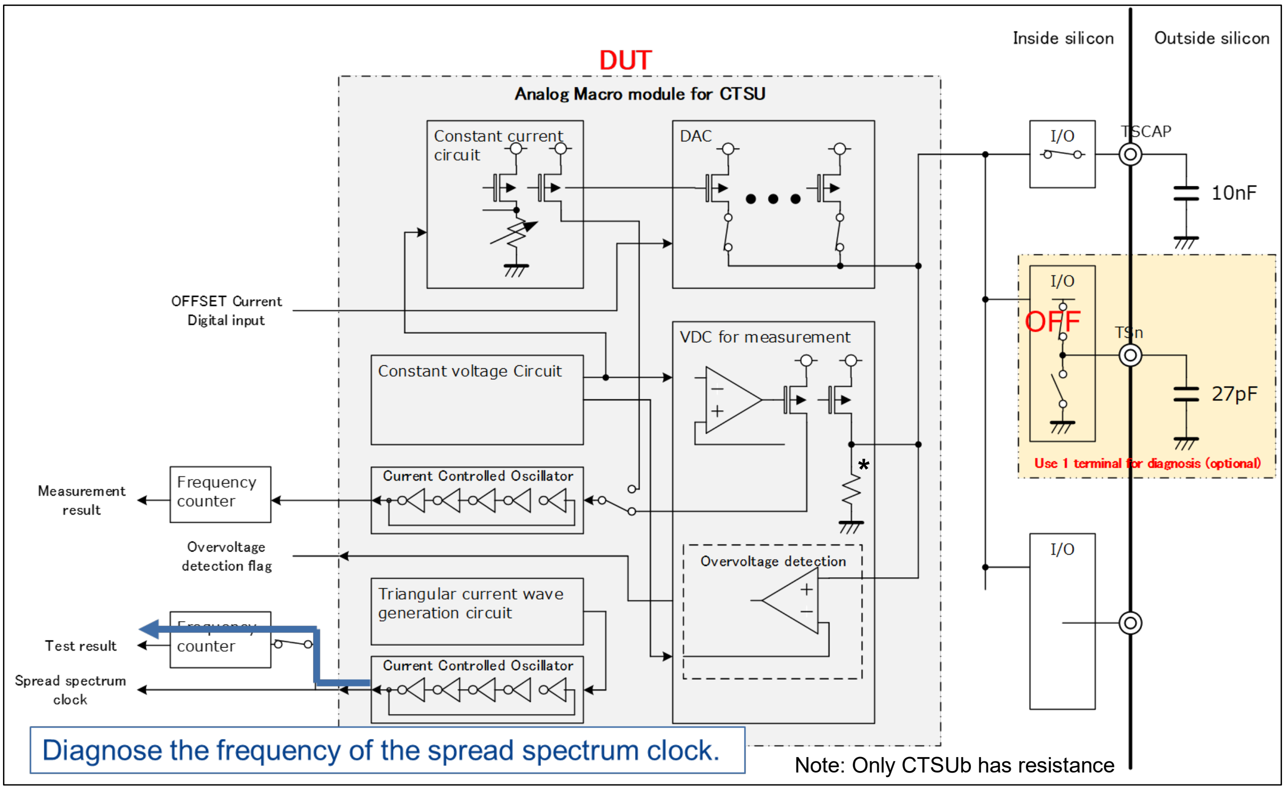

Figure 2.5 Circuits of SSCG Oscillator Test

CTSUSPMD: Calibration Mode BIT (CTSUSPMD = 0 is Capacitance scan mode)

CTSUTSOC: Calibration Setting 2 BIT (CTSUTSOC = 1 is Calibration setting 2)

CTSUCLK1 : Spread clock count test BIT (CTSUCLK1 = 1 is spread clock test mode)

Operation outline

(1) Set CTSU power on.

(2) Synchronous Noise Reduction Setting.

(3) Set High Pass Noise Reduction.

(4) Set sensor Stabilization.

(5) Set CLK division.

(6) Set Self scan mode.

(7) Set CTSUSPMD = 0, CTSUTSOC = 1, CTSUCLKSEL1 = 1.

(8) CTSU scan.

(9) Store reference value of scan result to dedicated variables.

(10) If stored scan result is within the standard threshold value range, PASS the diagnosis.

(11) If stored scan result is without the standard threshold value range, FAIL the diagnosis and return the FSP_ERR_CTSU_DIAG_SSCG.

2.6 Current Offset DAC Test

Diagnose the frequency of scan result when Current Offset DAC setting is changed. External capacitor of 27pF is necessary for this test.
This test is for CTSU other than CTSUb.

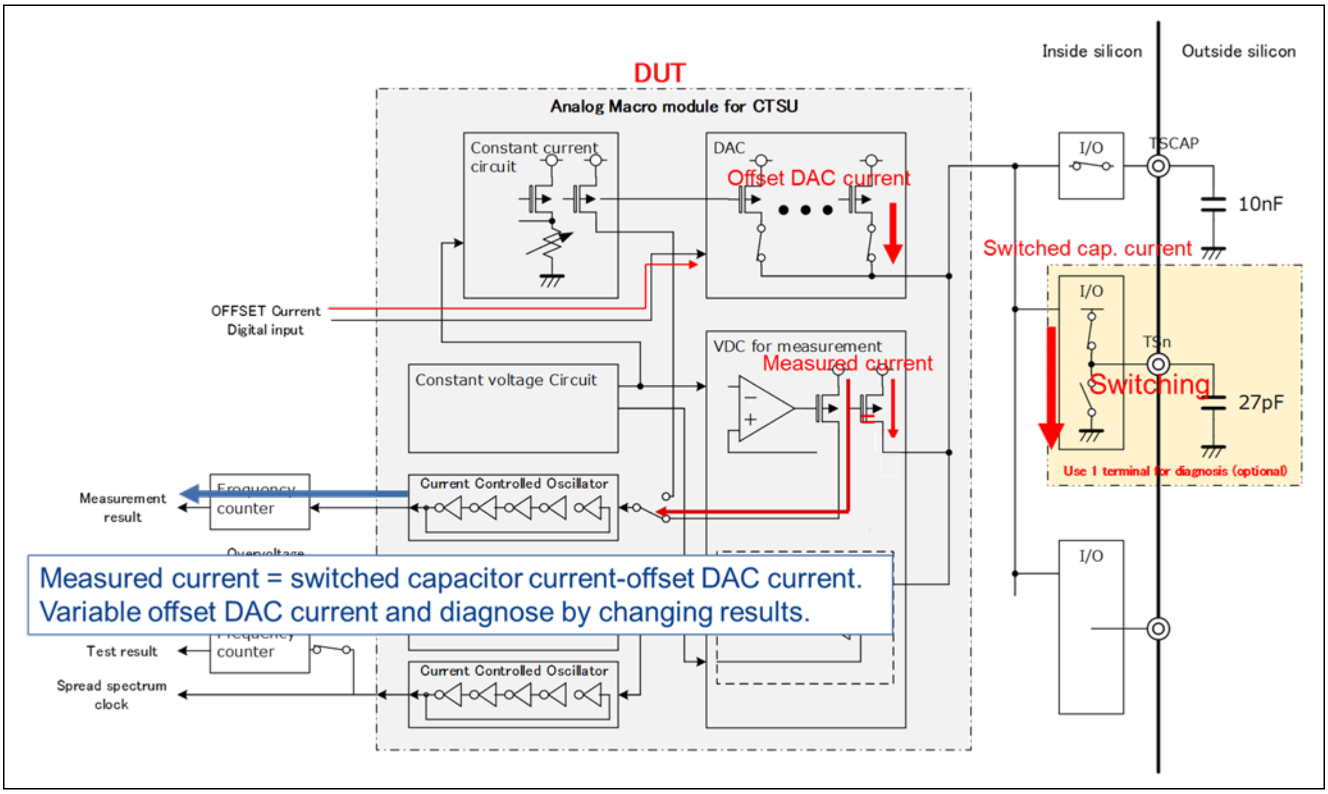

Figure 2.6.1 Circuits of Current Offset DAC Test

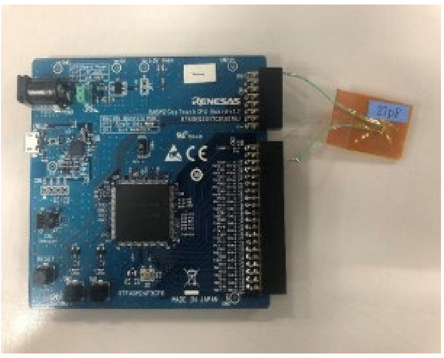

Figure 2.6.2 External circuits for Current Offset DAC Test

CTSUSO0: CTSU Sensor Offset Adjustment BIT

Operation outline

(1) Connect lower limit specification capacitor: 27pF between a TS terminal and GND as Figure 2.5.2.

(2) Coding into "qe_define.h" for the TS terminal number as following example.

```
---------------------------------------------------------------------
Example: Connect capacitor with TS7.
#define CTSU_CFG_DIAG_DAC_TS                (7)
---------------------------------------------------------------------
```

(3) Set CTSU power on.

(4) Synchronous Noise Reduction Setting.

(5) Set High Pass Noise Reduction.

(6) Set sensor Stabilization.

(7) Set CLK division.

(8) Set Self scan mode.

(9) 1 TS terminal connected with user electrode.

(10) Set offset value to "CTSUSO0" as scan result becomes around theoretical value 10240 without touching the electrode.

(11) Repeat CTSU scan for 6 times with following conditions.

Set (2) offset value to "ctsuso0" then CTSU scan without touching the electrode.

Set (2) offset value - 0x10 to "CTSUSO0" then CTSU scan without touching the electrode.

Set (2) offset value - 0x20 to "CTSUSO0" then CTSU scan without touching the electrode.

Set (2) offset value - 0x40 to "CTSUSO0" then CTSU scan without touching the electrode.

Set (2) offset value - 0x80 to "CTSUSO0" then CTSU scan without touching the electrode.

Set (2) offset value - 0x100 to "CTSUSO0" then CTSU scan without touching the electrode.

(12) Store above 6 scan results to dedicated variables.

If stored correction value is within the standard threshold value range, PASS the diagnosis.

If stored scan result is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_DAC.

2.7 Current Offset DAC Test (without TS)

Check the frequency of scan result when Current Offset DAC setting is changed.
This test is for CTSUb other than CTSU.

(1) ADC module to the scan setting.

(2) Set CTSU power on.

(3) TSCAP voltage measurement by ADC for 8 times with following conditions.

Set Load resistance 15k ohm and CTSUSO is 0x200 then measure TSCAP voltage by ADC.

Set Load resistance 30k ohm and CTSUSO is 0x100 then measure TSCAP voltage by ADC.

Set Load resistance 60k ohm and CTSUSO is 0x080 then measure TSCAP voltage by ADC.

Set Load resistance 60k ohm and CTSUSO is 0x070 then measure TSCAP voltage by ADC.

Set Load resistance 60k ohm and CTSUSO is 0x060 then measure TSCAP voltage by ADC.

Set Load resistance 60k ohm and CTSUSO is 0x050 then measure TSCAP voltage by ADC.

Set Load resistance 60k ohm and CTSUSO is 0x030 then measure TSCAP voltage by ADC.

Set Load resistance 60k ohm and CTSUSO is 0x088 then measure TSCAP voltage by ADC.

(4) Store above 8 scan results to dedicated variables.

If stored correction value is within the standard threshold value range, PASS the diagnosis.

If stored scan result is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_DAC.

3. CTSU2 Diagnosis

This chapter describes the following nine types of tests.

- Output Voltage Test
- Overvoltage Detection Test
- Over Current Detection Test
- Load Resistance Measurement Test
- Current Source Test
- SENSCLK Frequency Gain Test
- SUCLK Frequency Gain Test
- Clock Recovery Test
- CFC Oscillator Gain Test

CTSU2 also includes CTSU2L, CTSU2La, CTSU2SL.

Output Voltage Test requires the ADC module.

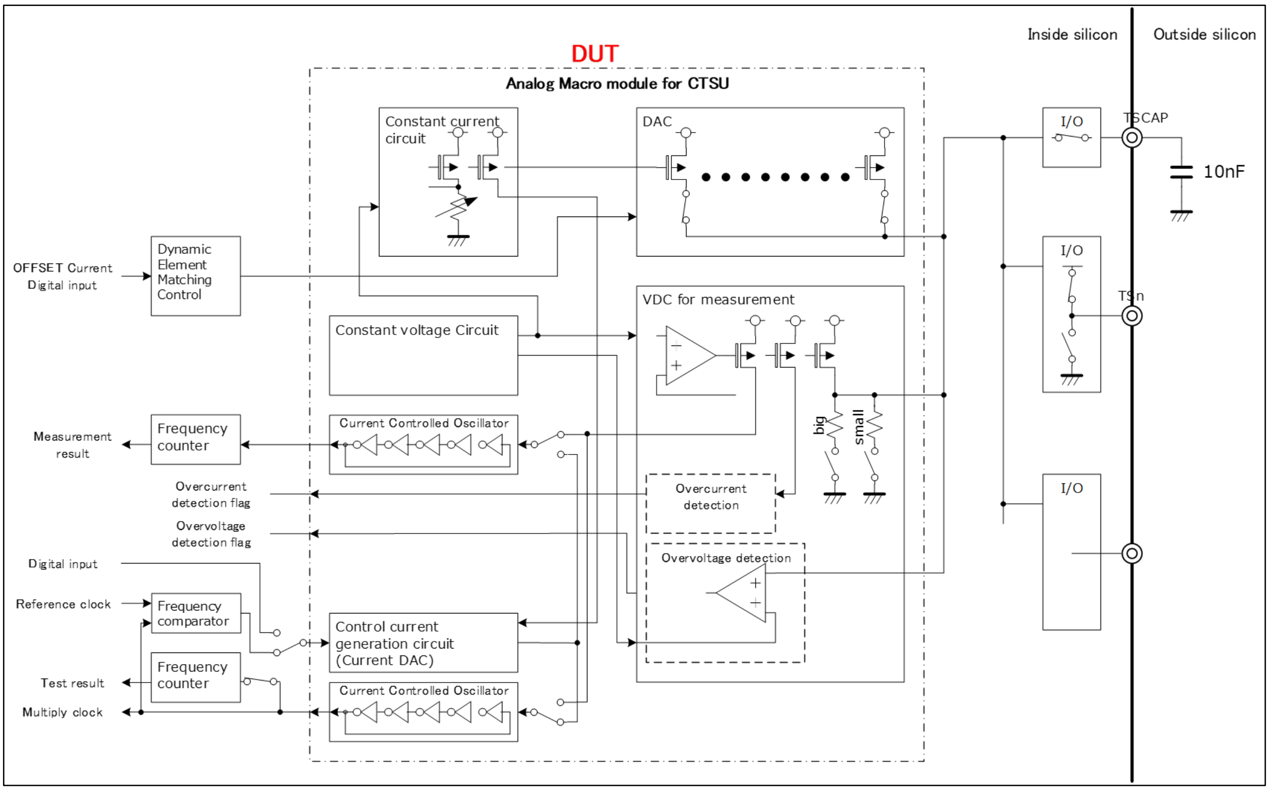

Figure 3.1 Circuits of CTSU2 Diagnosis

3.1 Output Voltage Test

Diagnose “Low drop output voltage down converter” (VDC) output voltage.

Operation outline

(1) Set 16ch of the ADC module to the scan setting.

(2) Set CTSU power on.

(3) Set Self scan mode.

(4) Set SO value initialize.

(5) TSCAP voltage measurement by ADC for 8 times with following conditions.

- Set Load resistance 60k ohm then measure TSCAP voltage by ADC.
- Set Load resistance 30k ohm then measure TSCAP voltage by ADC.
- Set Load resistance 15k ohm then measure TSCAP voltage by ADC.
- Set Load resistance 7.5k ohm then measure TSCAP voltage by ADC.
- Set VDC gain 20uA then measure TSCAP voltage by ADC.
- Set VDC gain 40uA then measure TSCAP voltage by ADC.
- Set VDC gain 80uA then measure TSCAP voltage by ADC.
- Set VDC gain 160uA then measure TSCAP voltage by ADC.

(6) Store above measurement results to dedicated variables.

If stored measurement result is within the standard threshold value range, PASS the diagnosis.

If stored measurement result is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_OUTPUT_VOLTAGE.

3.2 Overvoltage Detection Test

Diagnose overvoltage detection circuit.

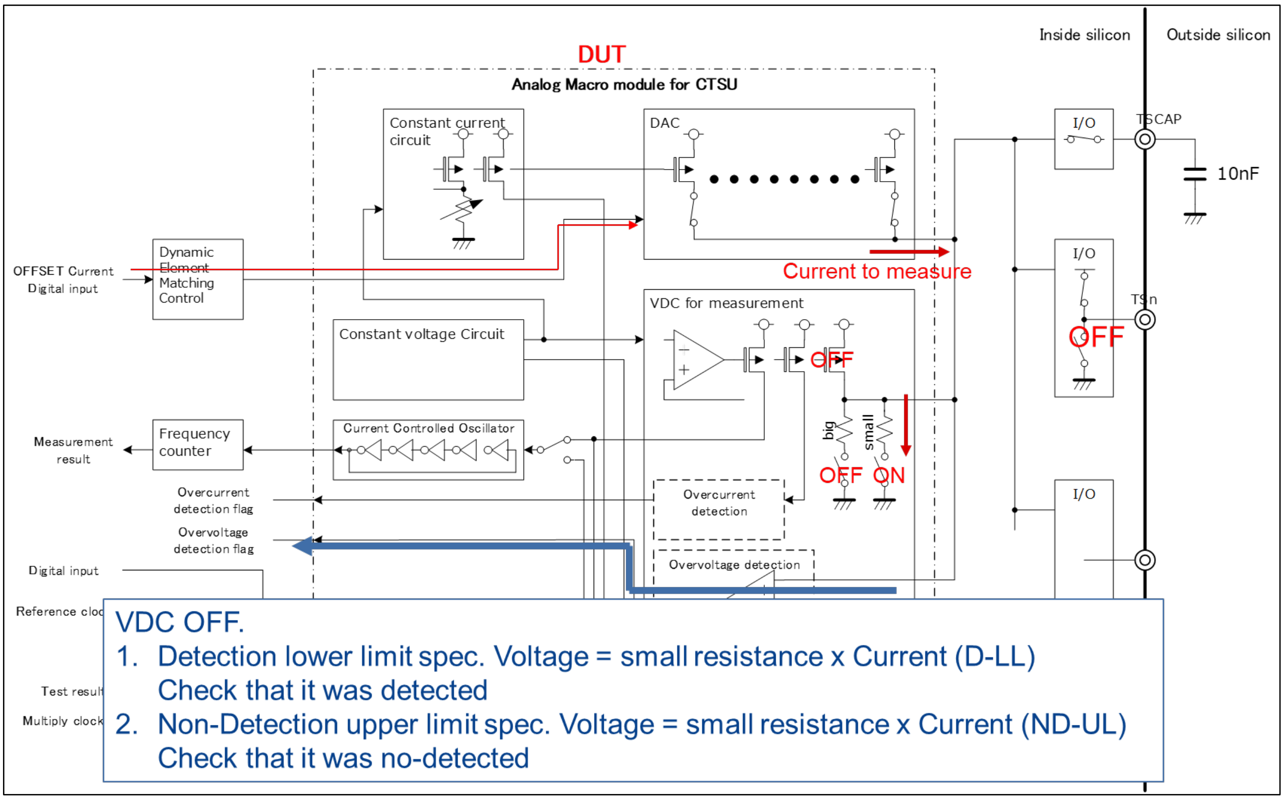

Figure 3.2 Circuits of Overvoltage Detection Test

ICOMP0 : TSCAP Voltage Error Monitor This bit monitors the error status of the TSCAP voltage.
(ICOMP0 = 0: Normal TSCAP voltage ICOMP0 = 1: Abnormal TSCAP voltage)

ICOMPRST: CTSU CTSUICOMP1 Flag Reset. When 1 is written to the ICOMPRST bit, the ICOMP0 and ICOMP1 bits are cleared.

Operation outline

(1) Set CTSU power on.

(2) Set to internal calibration mode.

(3) Set internal voltage as less than 1.65V.

ICOMP0 = 0: PASS

ICOMP0 = 1: FAIL, return FSP_ERR_CTSU_DIAG_OVER_VOLTAGE

(4) Set internal voltage as equal or greater than 1.65V.

ICOMP0 = 1: PASS

ICOMP0 = 0: FAIL, return FSP_ERR_CTSU_DIAG_OVER_VOLTAGE

(5) Set "ICOMPRST" =1 (Since internal voltage is equal or greater than 1.65V).

ICOMP0 = 1: PASS

ICOMP0 = 0: FAIL, return FSP_ERR_CTSU_DIAG_OVER_VOLTAGE

(6) Set internal voltage as less than 1.65V (Since it doesn't execute "ICOMPRST"=1).

ICOMP0 = 1: PASS

ICOMP0 = 0: FAIL, return FSP_ERR_CTSU_DIAG_OVER_VOLTAGE

(7) Set "ICOMPRST" =1 (It is reset).

ICOMP0 = 0: PASS

ICOMP0 = 1: FAIL, return FSP_ERR_CTSU_DIAG_OVER_VOLTAGE

3.3 Over Current Detection Test

Diagnose over current detection circuit.

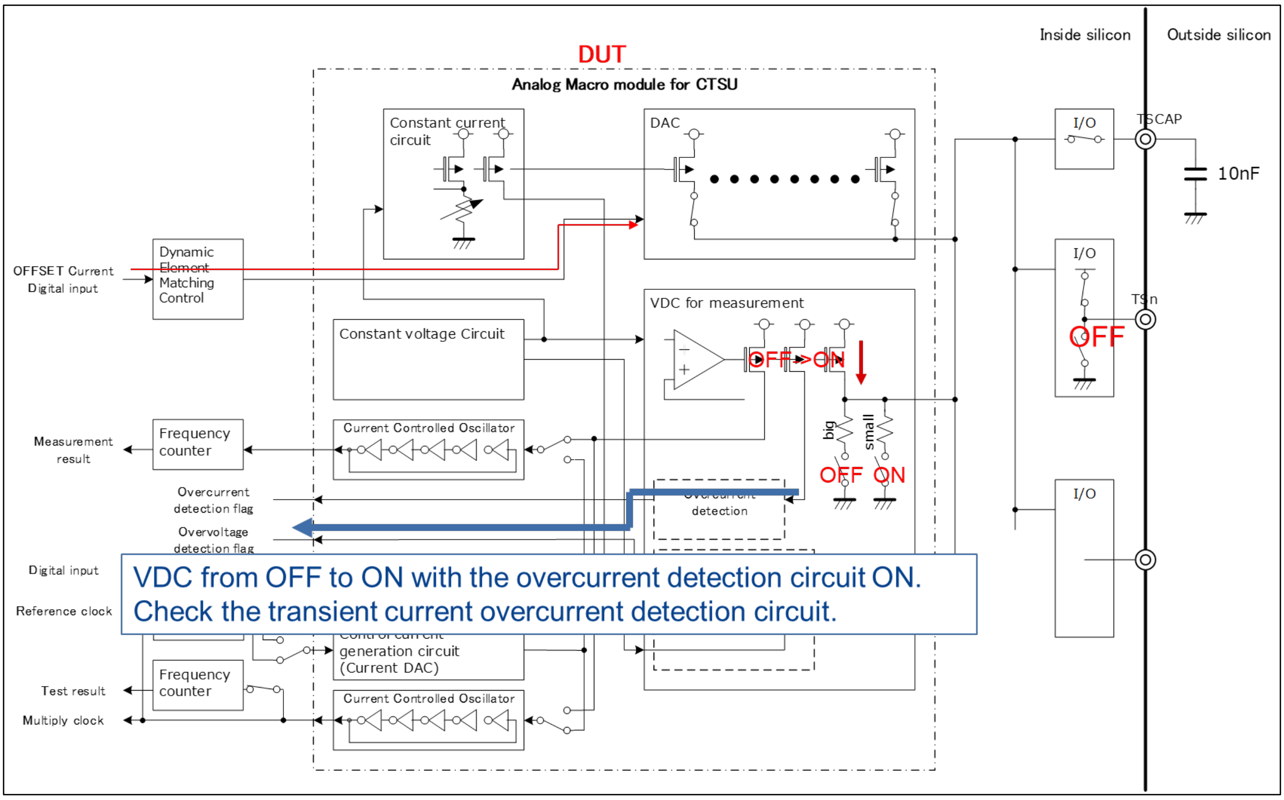

Figure 3.3 Circuits of Over Current Detection Test

CTSUPON: CTSU Power Supply Enable

ICOMP1: CTSU Sense Current Error Monitor. This bit monitors the error status of the sensor current (ICOMP0 = 0: Normal TSCAP current ICOMP0 = 1: Abnormal TSCAP current)

Operation outline

(1) Discharge TSCAP Capacitor.

(2) Charge TSCAP Capacitor by CTSUPON.

(3) CTSU scan start.

(4) If “ICOMP1” =1 in CTSUFN interrupt, PASS the diagnosis.

If “ICOMP1” =0 in CTSUFN interrupt, FAIL the diagnosis, and return FSP_ERR_CTSU_DIAG_OVER_CURRENT.

3.4 Load Resistance Measurement Test

Diagnose VDC internal resistance.

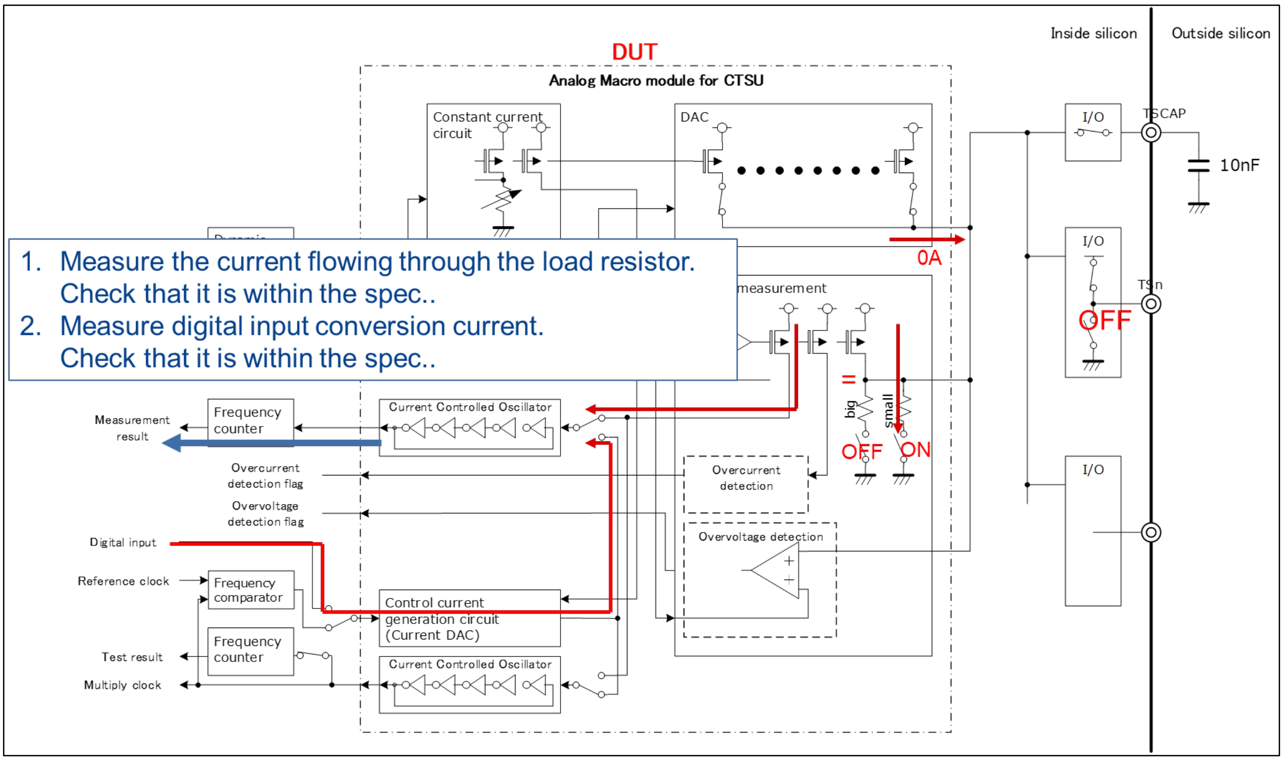

Figure 3.4 Circuits of Load Resistance Measurement Test

Operation outline

(1) Set CTSU power on.

(2) Set high resolution pulse mode.

(3) Scan the current input to the ICO by passing current through the internal resistance in each range.

Scan CTSU under the following conditions.

- Set Load resistance 60k ohm, then CTSU scan.
- Set Load resistance 30k ohm, then CTSU scan.
- Set Load resistance 15k ohm, then CTSU scan.
- Set Load resistance 7.5k ohm, then CTSU scan.

(4) Correct the above 4 scan results by Load resistance variation (Trimming Register) coefficient.

(5) Store above correcting value to dedicated variables.

(6) If stored correcting value is within the standard threshold value range, PASS the diagnosis.

If stored correcting value is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_LOAD_RESISTANCE.

3.5 Current Source Test

Diagnose Current Offset DAC Current source.

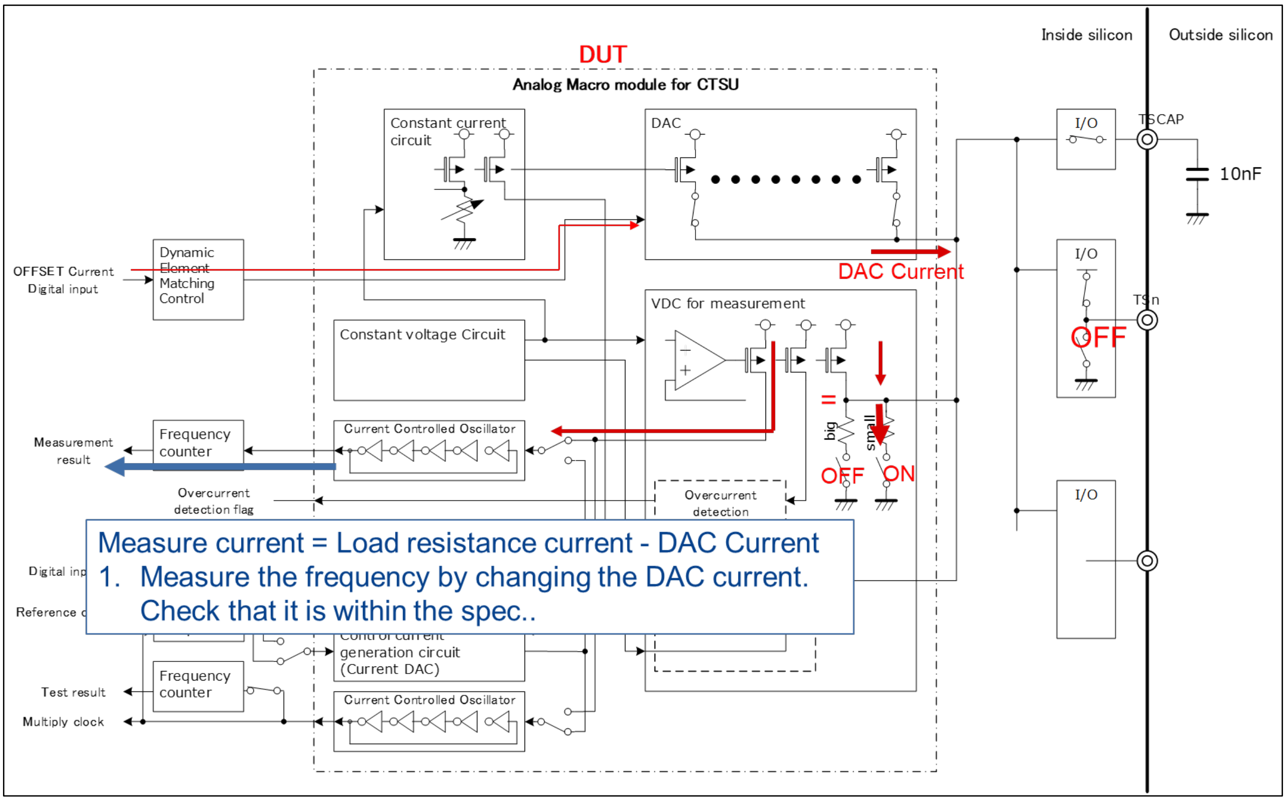

Figure 3.5 Circuits of Current Source Test

Operation outline

(1) Set CTSU power on.

(2) Set high resolution pulse mode.

(3) Set Self scan mode.

(4) Set SO value initialization.

(5) VDC N-ch setting (40uA mode)

(6) DAC initial setting.

(7) Scan CTSU under the following conditions.

7-1) Scan the upper current source 16 times.

DAC: Upper current source 1 unit ON [10uA]

7-2) All combinations of lower current source 8/10 units Scan 10 times each. (1 unit = 1.25uA)

DAC: 8 units of lower current source ON [total 10uA]

(8) Store above correcting value to dedicated variables.

(9) If the calculation values of (“scan value with setting Load resistance 30k ohm” in “Load Resistance Scan Test”) – (stored scan values) is within range of standard threshold value range, PASS the diagnosis.

If the value is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_CURRENT_SORCE.

3.6 SENSCLK Frequency Gain Test

Diagnose SENSCLK gain for Current Controlled Oscillator DAC current source from 1 to 12 units ON.

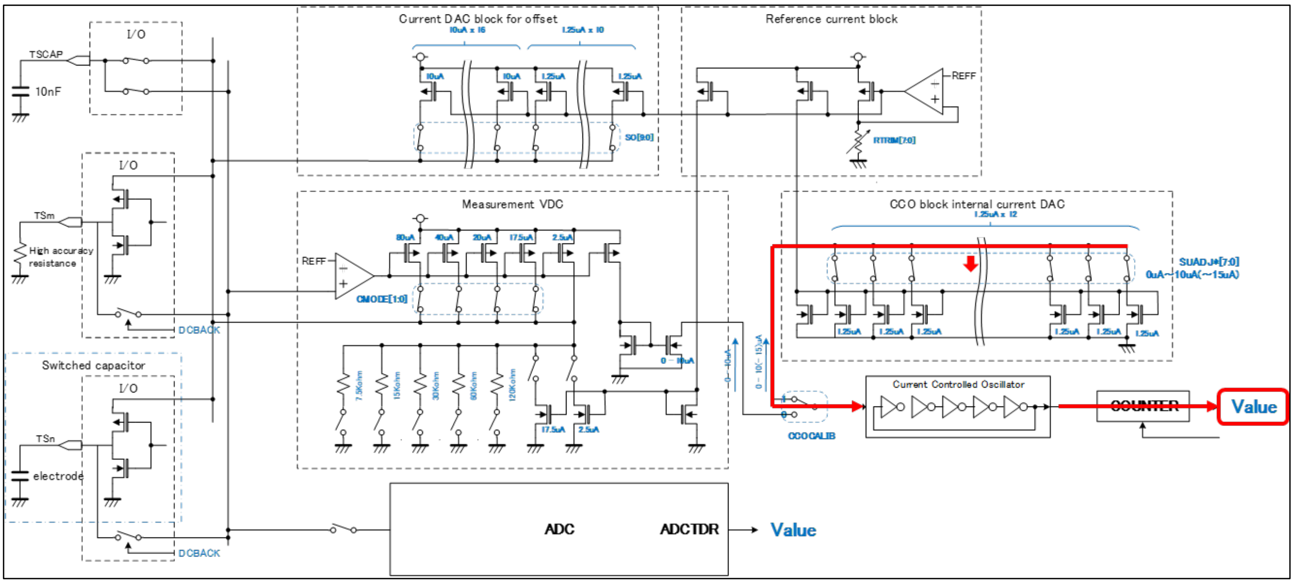

Figure 3.6 Circuits of SENSCLK Frequency Gain Test

SUADJ0 : CCO-DAC current setting BIT

SUCARRY: CCO-DAC current setting BIT

SUCNT : CCO-DAC current setting BIT

CCOCALIB: Calibration Selection of Current Controlled Oscillator for Scan.

Operation outline

(1) Set CTSU power on.

(2) Set high resolution pulse mode.

(3) Set Self scan mode.

(4) CCOCALB = 1; setting.

(5) Set "CTSUSUCLKA.SUADJ0[7:0]" as Current Controlled Oscillator Current DAC current source is set ON from 1 to 12 units.

(6) Scan by inputting each constant current from internal DAC to ICO scan count value of "SENSCLK".

(7) Store above scan value to dedicated variables.

(8) Repeat above from 1 to 12 units of DAC current source.

(9) If stored scan value is within the standard threshold value range, PASS the diagnosis.

If stored scan value is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_SENSCLK_GAIN.

3.7 SUCLK Frequency Gain Test

Diagnose SUCLK gain for Current Controlled Oscillator DAC current source from 1 to 12 units ON.

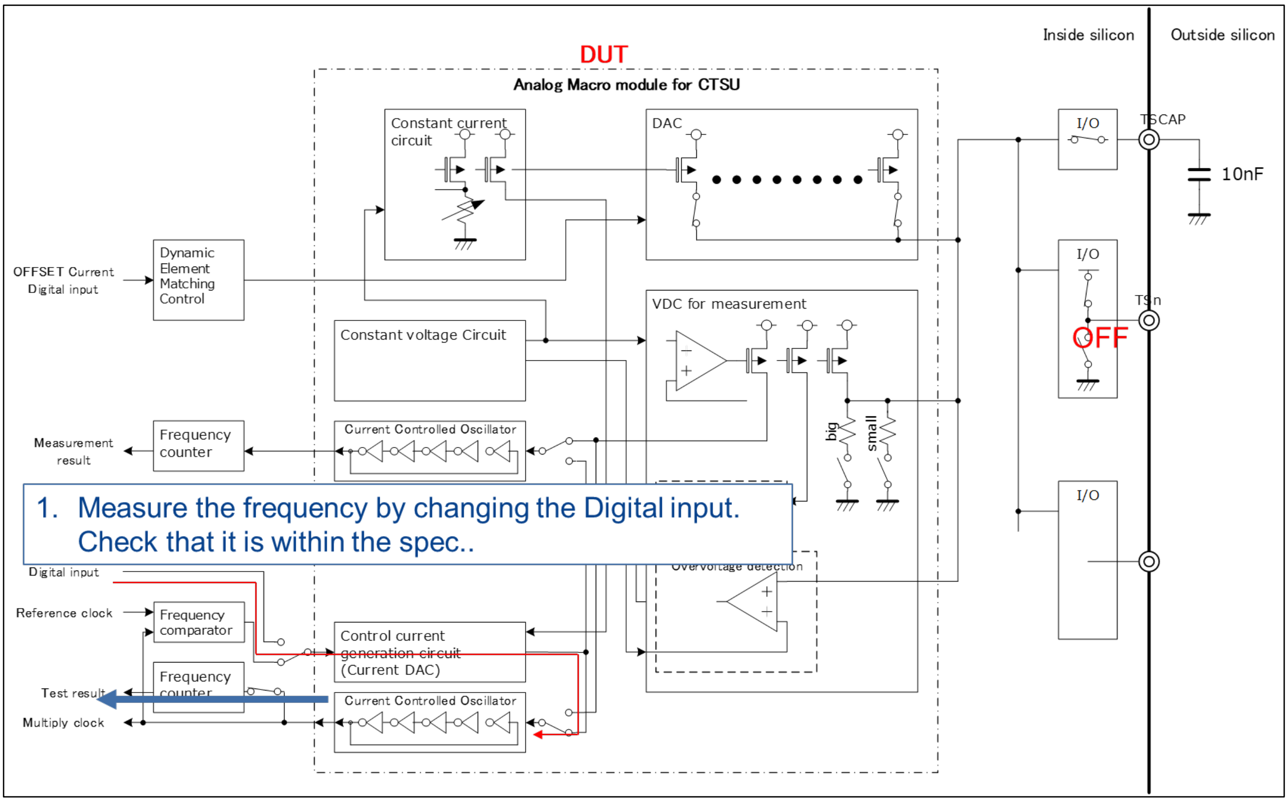

Figure 3.7 Circuits of SUCLK Frequency Gain Test

SUADJ0 : CCO-DAC current setting BIT

SUCARRY : CCO-DAC current setting BIT

SUCNT : CCO-DAC current setting BIT

CCOCALIB : Calibration Selection of Current Controlled Oscillator for Scan.

Operation outline

(1) Set CTSU power on.

(2) Set high resolution pulse mode.

(3) Set Self scan mode.

(4) CCOCALB = 0; setting.

(5) Set SUADJ0, SUCARRY, SUCNT as Current Controlled Oscillator Current DAC current source is set ON from 1 to 12 units.

(6) Scan by inputting each constant current from internal DAC to ICO scan count value of “SUCLK”.

(7) Scan count value of “SUCLK”.

(8) Store above scan value to dedicated variables.

(9) Repeat above from 1 to 12 units of DAC current source.

If stored scan value is within the standard threshold value range, PASS the diagnosis.

If stored scan value is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_SUCLK_GAIN.

3.8 Clock Recovery Test

Diagnose SUCLK Clock Recovery function.

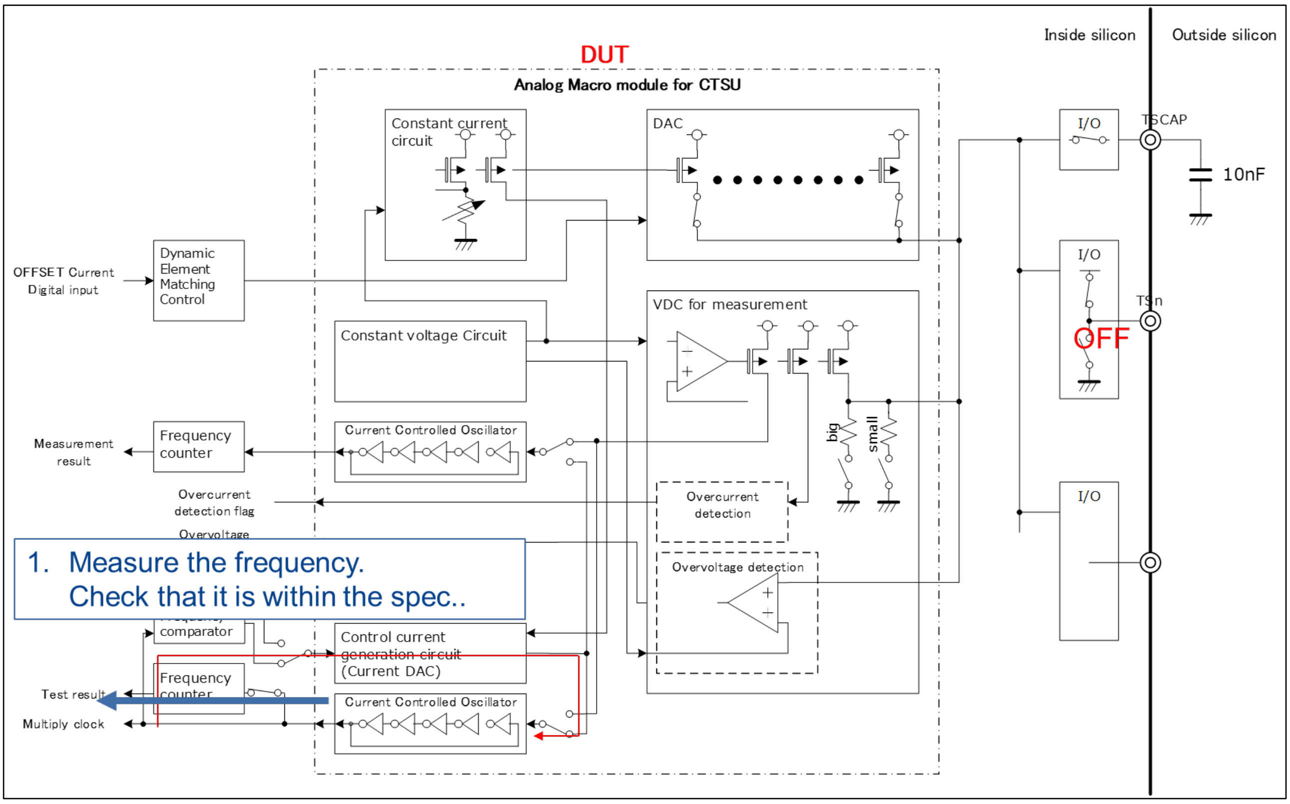

Figure 3.8 Circuits of Clock Recovery Test

Operation outline

(1) Set Normal scan settings in the CTSUCRA register.

(2) Set Normal scan settings in the CTSUCRB register.

(3) SUCLK operation mode.

(4) Set Self scan mode.

(5) Set SO value initialize.

(6) Set 3 frequencies multi scan setting.

(7) CTSU scan.

(8) Store above scan value to dedicated variables.

(9) Calculates SUCLK frequency.

(10) If the result compared stored scan value and calculated frequency is within the standard threshold value range, PASS the diagnosis.

If the compared value is without the standard threshold value range, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_CLOCK_RECOVERY.

3.9 CFC Oscillator Gain Test

Diagnose CFC Oscillator Gain.

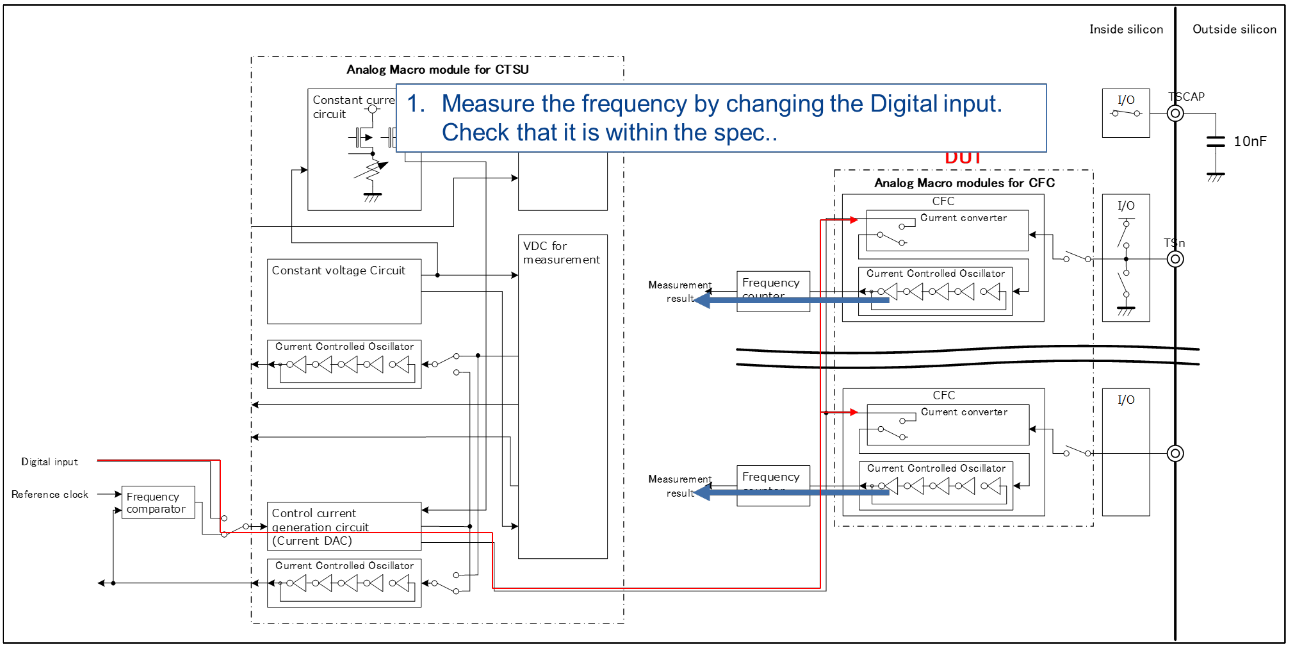

Figure 3.9 Circuits of CFC Oscillator Gain Test

SUADJ0: CCO-DAC current setting BIT

Operation outline

(1) Set CFC power on.

(2) Set CFC self-capacity mode.

(3) Set high resolution pulse mode.

(4) Set CFC external current scan mode.

(5) Set SUADJ0 as current source of Current Controlled Oscillator Current DAC enabled from 1 to 5 sources.

(6) Scan CFC counter value.

(7) Store above scan value to dedicated variables.

(8) Repeat above scan for 1 to 5 sources.

(9) Compare scan count result and target value.

(10) If the compared result becomes larger as the number of DAC current sources increase, PASS the diagnosis.

If the compared result becomes lower as the number of DAC current sources increase, FAIL the diagnosis and return FSP_ERR_CTSU_DIAG_CFC_GAIN.

4. API specification

Syntax	
fsp_err_t R_CTSU_Diagnosis (ctsu_ctrl_t * const p_ctrl)	
Description	
This API is called when the return value of R_CTSU_DataGet for the diagnostic instance is FSP_SUCCESS. Diagnostic processing is performed using the measured results, and the result is notified as return values.	
Arguments	
ctsu_ctrl_t * const p_ctrl	ctsu_instance_ctrl_t g_ctsu_ctrl_diagnosis;
Return Values	
fsp_err_t	If all measurement for diagnoses is completed without any issue, return FSP_SUCCESS. If there was FAIL, return error code of each diagnosis as follows. For CTSU MCU FSP_ERR_CTSU_DIAG_LDO_OVER_VOLTAGE FSP_ERR_CTSU_DIAG_CCO_HIGH FSP_ERR_CTSU_DIAG_CCO_LOW FSP_ERR_CTSU_DIAG_SSCG FSP_ERR_CTSU_DIAG_DAC For CTSU2 MCU FSP_ERR_CTSU_DIAG_OUTPUT_VOLTAGE FSP_ERR_CTSU_DIAG_OVER_VOLTAGE FSP_ERR_CTSU_DIAG_OVER_CURRENT FSP_ERR_CTSU_DIAG_LOAD_RESISTANCE FSP_ERR_CTSU_DIAG_CURRENT_SOURCE FSP_ERR_CTSU_DIAG_SENSCLK_GAIN FSP_ERR_CTSU_DIAG_SUCLK_GAIN FSP_ERR_CTSU_DIAG_CLOCK_RECOVERY FSP_ERR_CTSU_DIAG_CFC_GAIN

5. Flowchart of sample application

Flowchart of sample application is shown Figure 5.1.

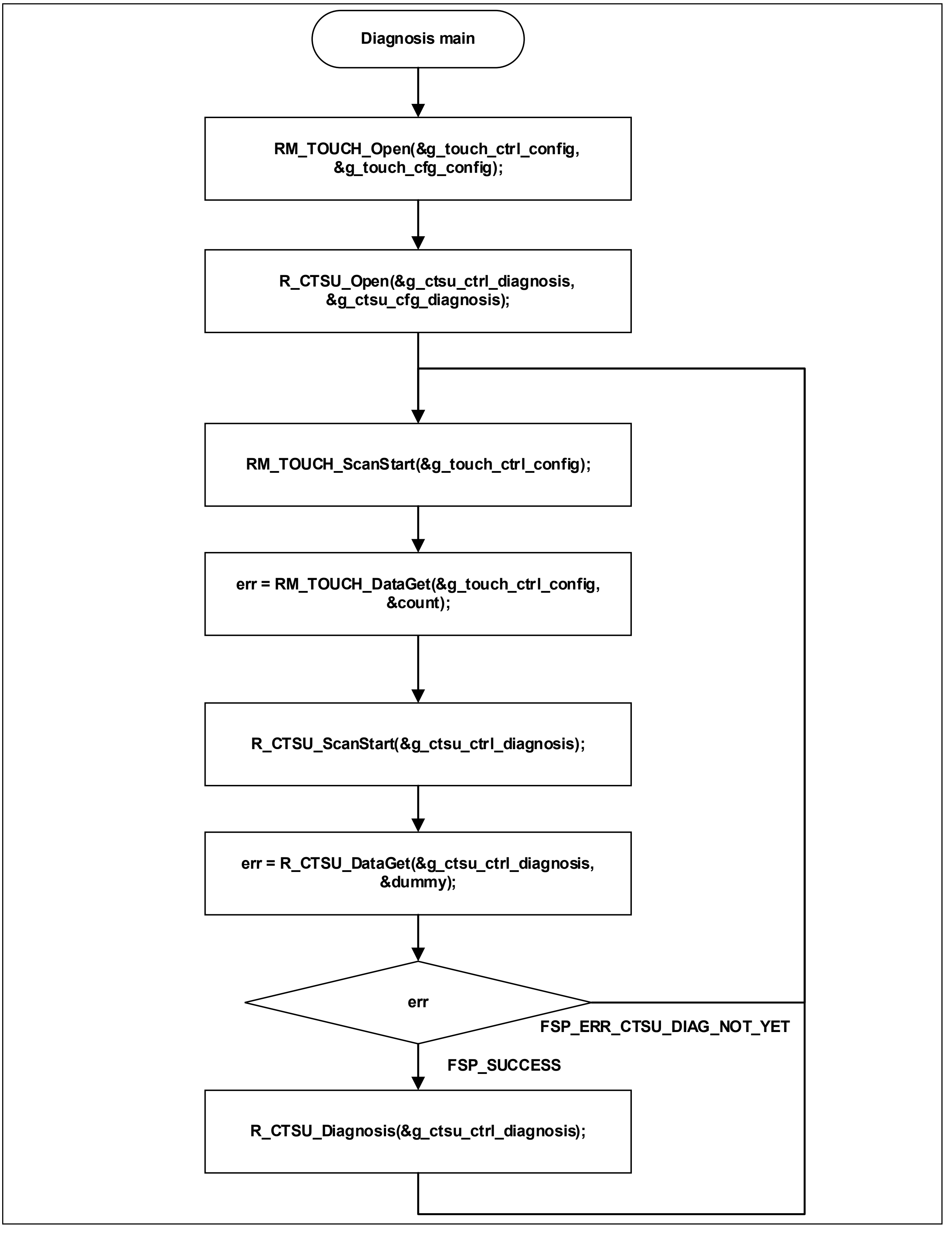

Figure 5.1 Flowchart of sample application for CTSU diagnosis

6. Procedure for creating a project using “QE for Capacitive Touch”

The procedure for creating a project using QE for Capacitive Touch is shown below.

6.1 RA Family

1) Create a new project.

2) Add a stack in the configurator.

Add touch middleware stack.

* Additional settings required when using CTSU2

Add ADC driver stack (Figure 6.1), and change the name “g_adc0” to “g_adc_ctsu”. (Figure 6.2)

(Click “FSP Configuration in the upper right corner, change the name in Properties.)

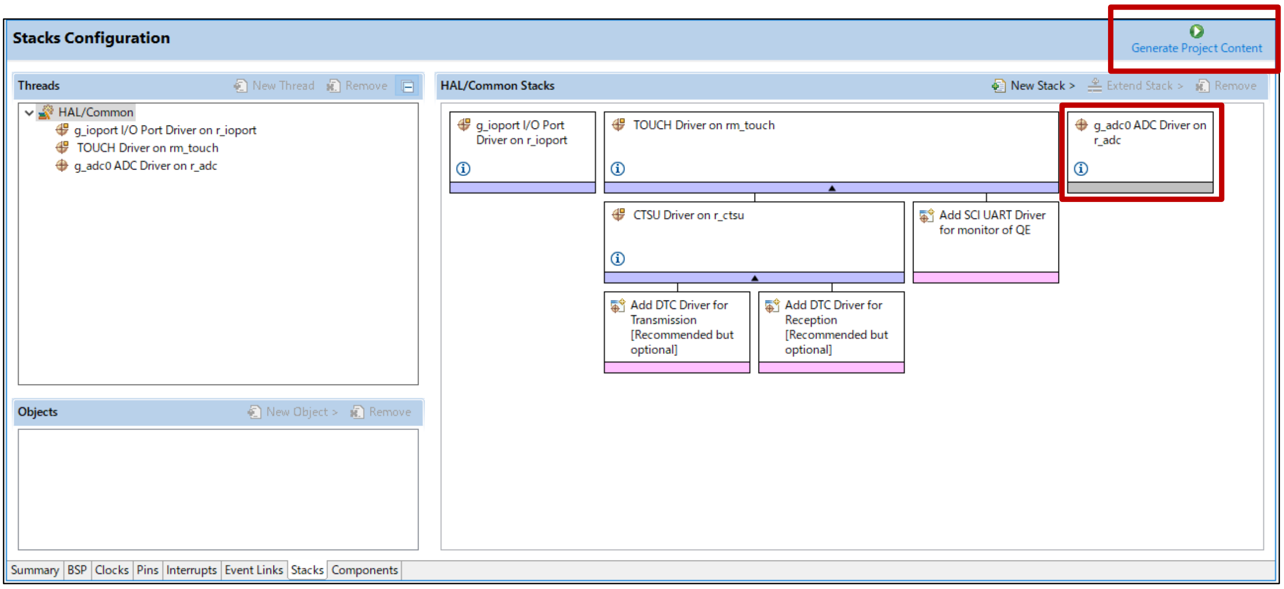

Figure 6.1 Stacks Configurations view

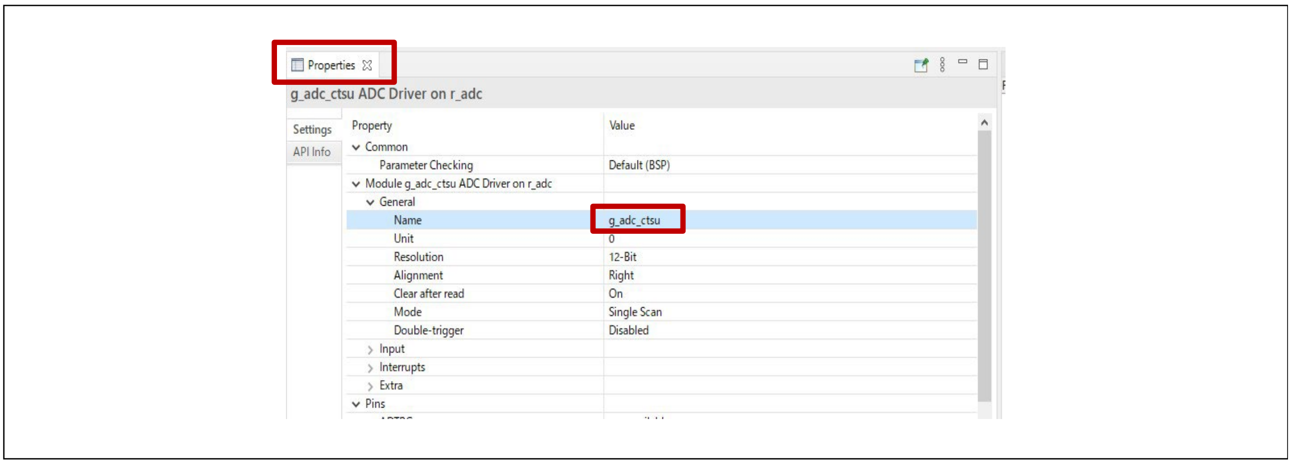

Figure 6.2 Change the name of “g_adc0”

3) Select the channel 16 checkbox in the ADC properties of Channel Scan Mask (Figure 6.3).

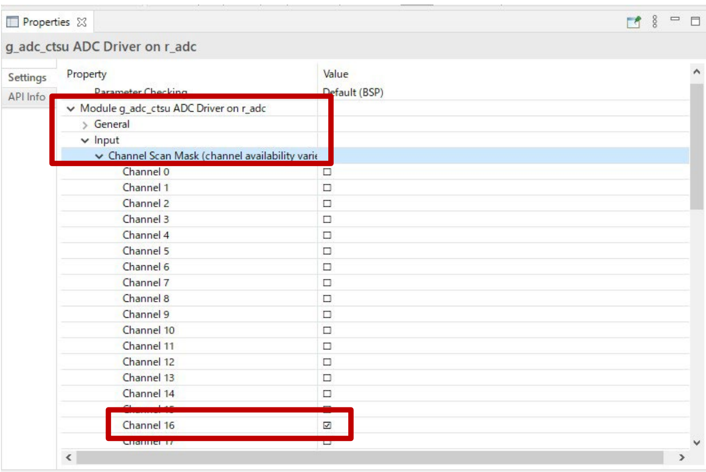

Figure 6.3 Select the "channel 16" checkbox in property of ADC

4) Set the pin in the configurator.

Select check box of TS terminal you want to use with CTSU scan.

For CTSU, need to select the TS terminal for "Current Offset DAC Test".

5) Generate code.

Click "Generate Project Content" in the upper right corner of the Configurator. (Figure 6.1)

6) Create a configuration with QE.

For QE ver3.2 or later, proceed to (A). For QE ver3.1 or before, please proceed to (B).

(A) QE ver3.2 or later

(A-1) Open the "Cap Touch Workflow (QE)" from Renesas views.

Click "Modify Configuration" as shown in Figure 6.4. Create element for CTSU scan. For CTSU, select to "Diagnosis Pin" for "Current Offset DAC Test". as shown in Figure 6.5

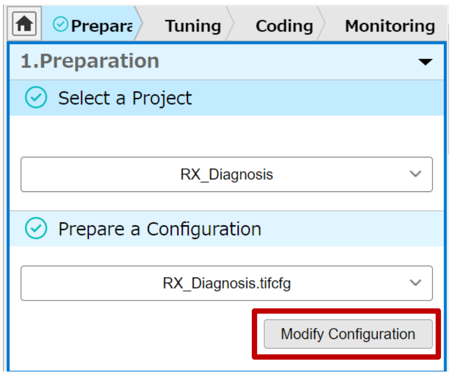

Figure 6.4 Modify Configuration in "Cap Touch Workflow (QE)

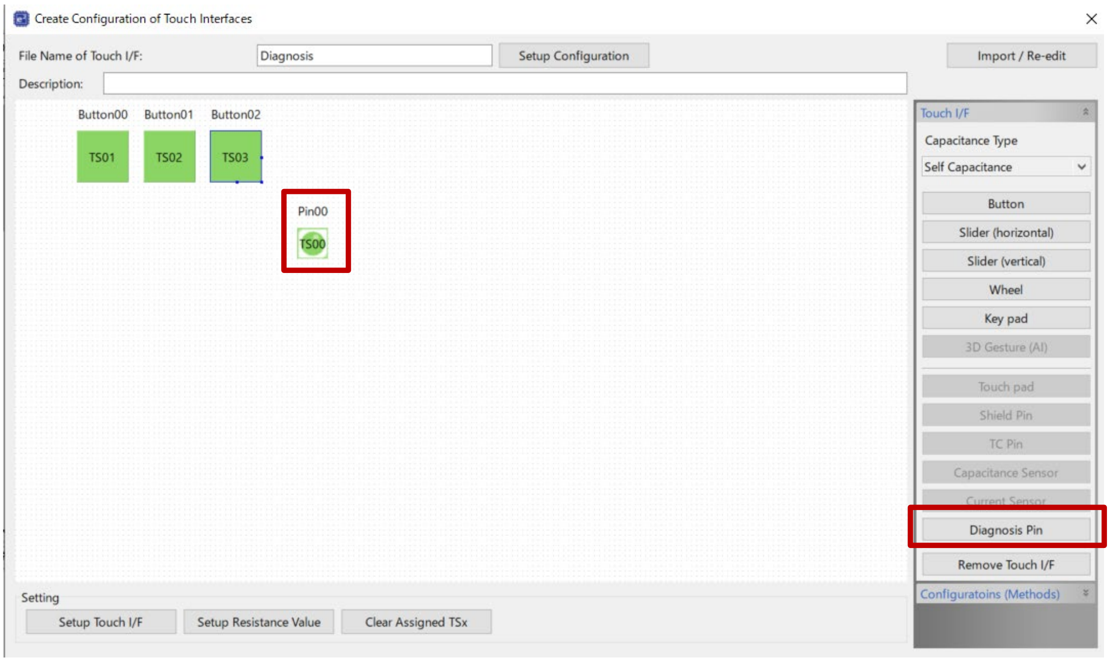

Figure 6.5 Select to "Diagnosis Pin" in Configuration of Touch Interfaces

(A-2) Complete tuning.

Click “Start Tuning” as shown in Figure 6.6. Follow the instructions from QE to complete the tuning operation. After that, check ”Use Diagnostic Code” as shown in Figure 6.6, and Click ”Output Parameter Files”.

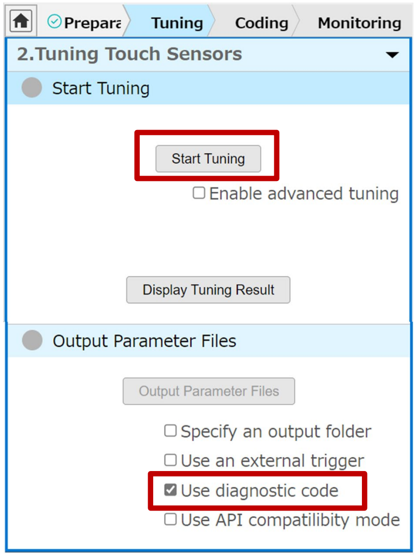

Figure 6.6 Modify Configuration in “Cap Touch Workflow (QE)”

(A-3) Output sample code.

Click “Show Sample” and open “Show Sample Code” view. Then click “Output to a File” and generate “qe_touch_sample.c” as shown in Figure 6.7.

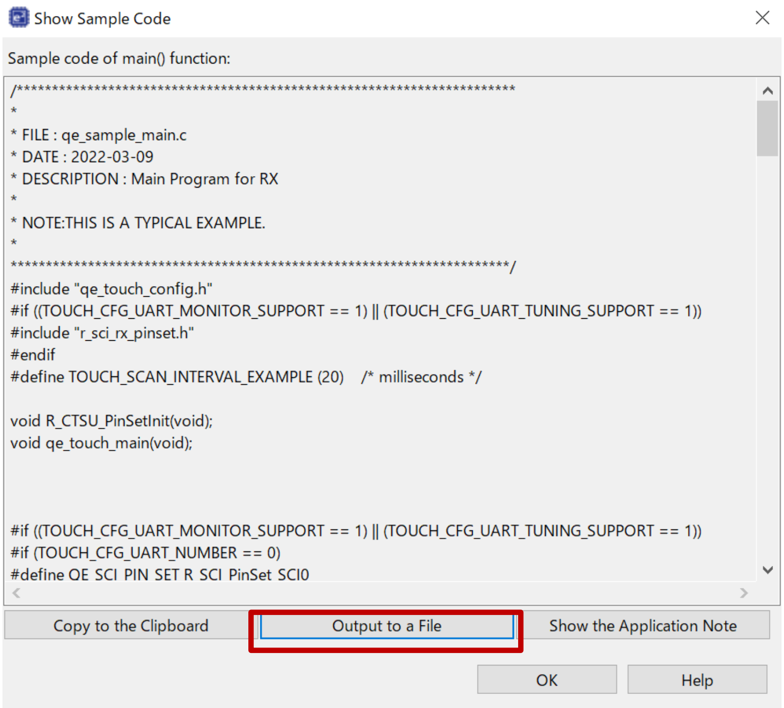

Figure 6.7 Modify Configuration in "Cap Touch Workflow (QE)"

(B) QE ver3.1 or before

(B-1) Open the "Cap Touch Main (QE)" from Renesas views.

Click "Modify Configuration" as shown in Figure 6.8. Create element for CTSU scan. For CTSU, select to "Diagnosis Pin" for "Current Offset DAC Test". as shown in Figure 6.9

(B-2) Complete tuning.

Click "Start Tuning" as shown in Figure 6.8. Follow the instructions from QE to complete the tuning operation. After that, check "Use Diagnostic Code" as shown in Figure 6.8, and Click "Output Parameter Files".

(B-3) Output sample code.

Click "Show Sample" and open "Show Sample Code" view. Then click "Output to a File" and generate "qe_touch_sample.c" as shown in Figure 6.10.

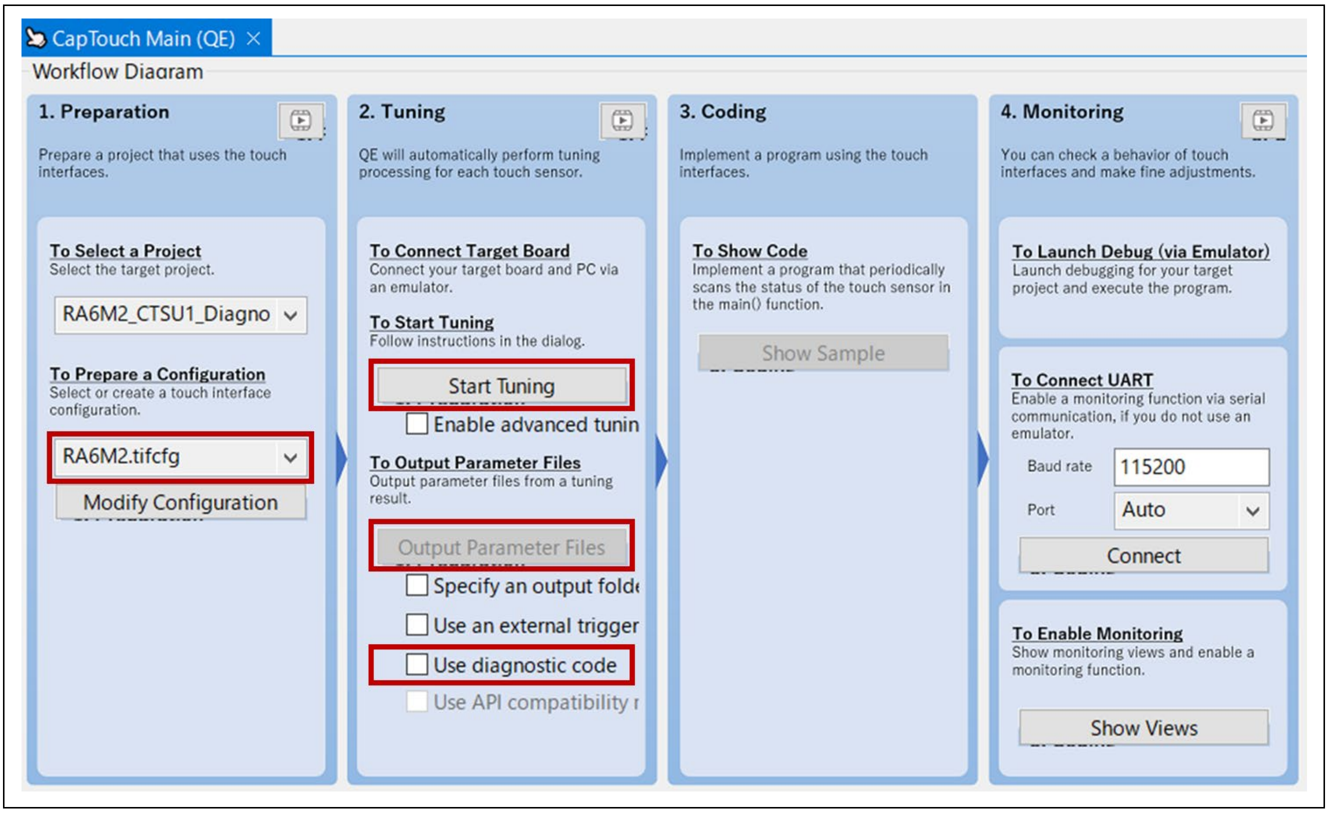

Figure 6.8 "Cap Touch Main (QE)"

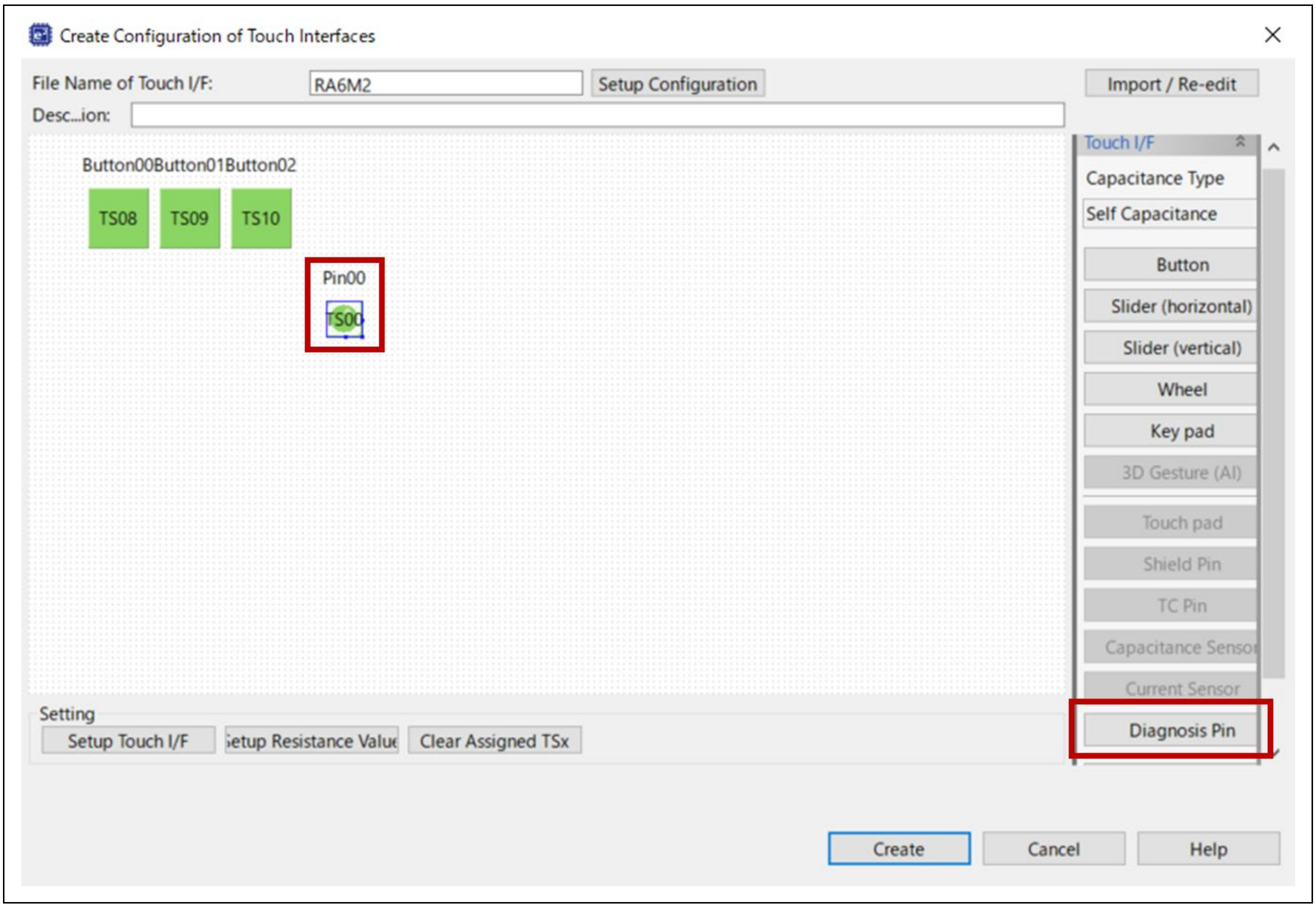

Figure 6.9 "Cap Touch Main (QE)"

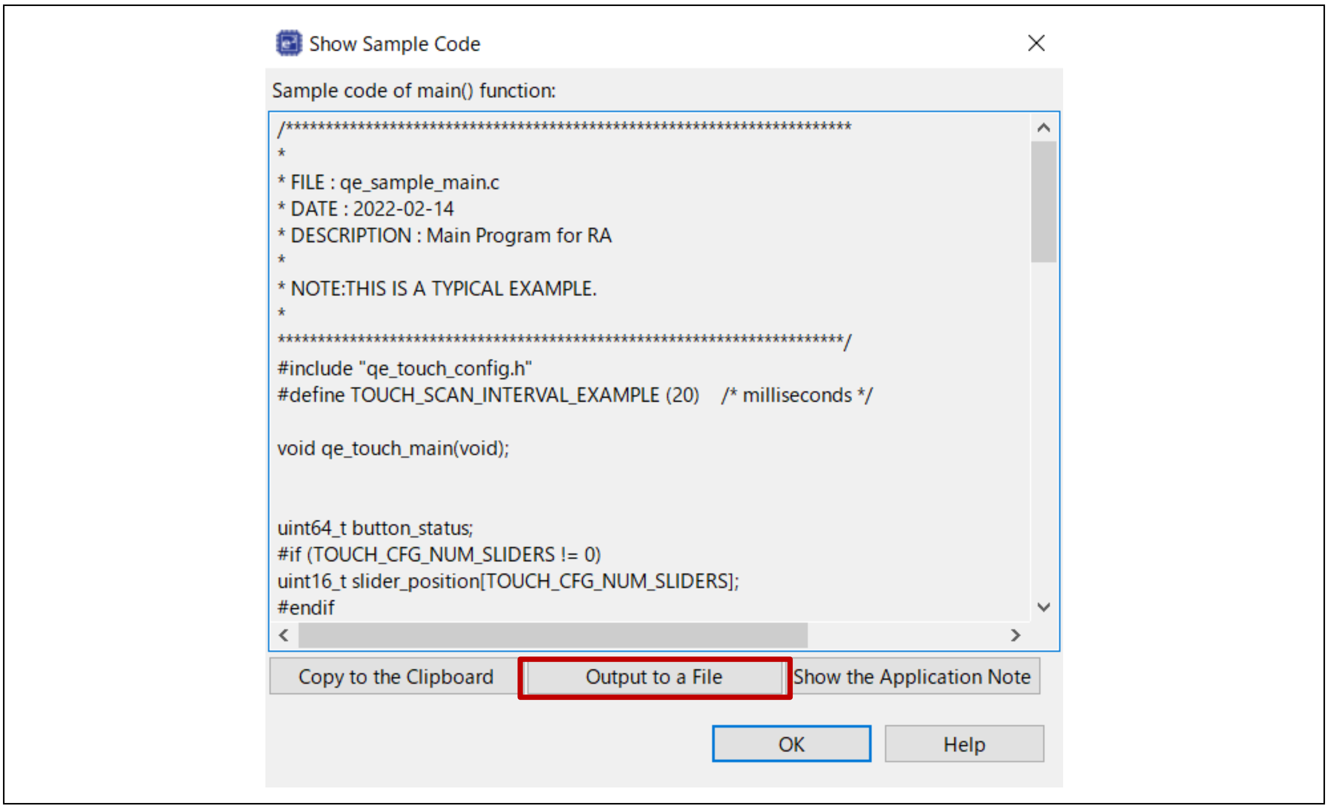

Figure 6.10 "Cap Touch Main (QE)"

6.2 RL78 Family

1) Create a new project.

2) Add a component in the configurator.

Add TOUCH middleware and CTSU Driver as shown in Figure 6.11.

3) Set the pin in the configurator.

Select check box of TS terminal you want to use with CTSU scan.

4) Generate code.

Click "Generate Code" in the upper right corner of the Configurator. (Figure 6.11)

5) Create a configuration with QE.

Same as "6.1 RA Family" [(6) Create a configuration with QE].

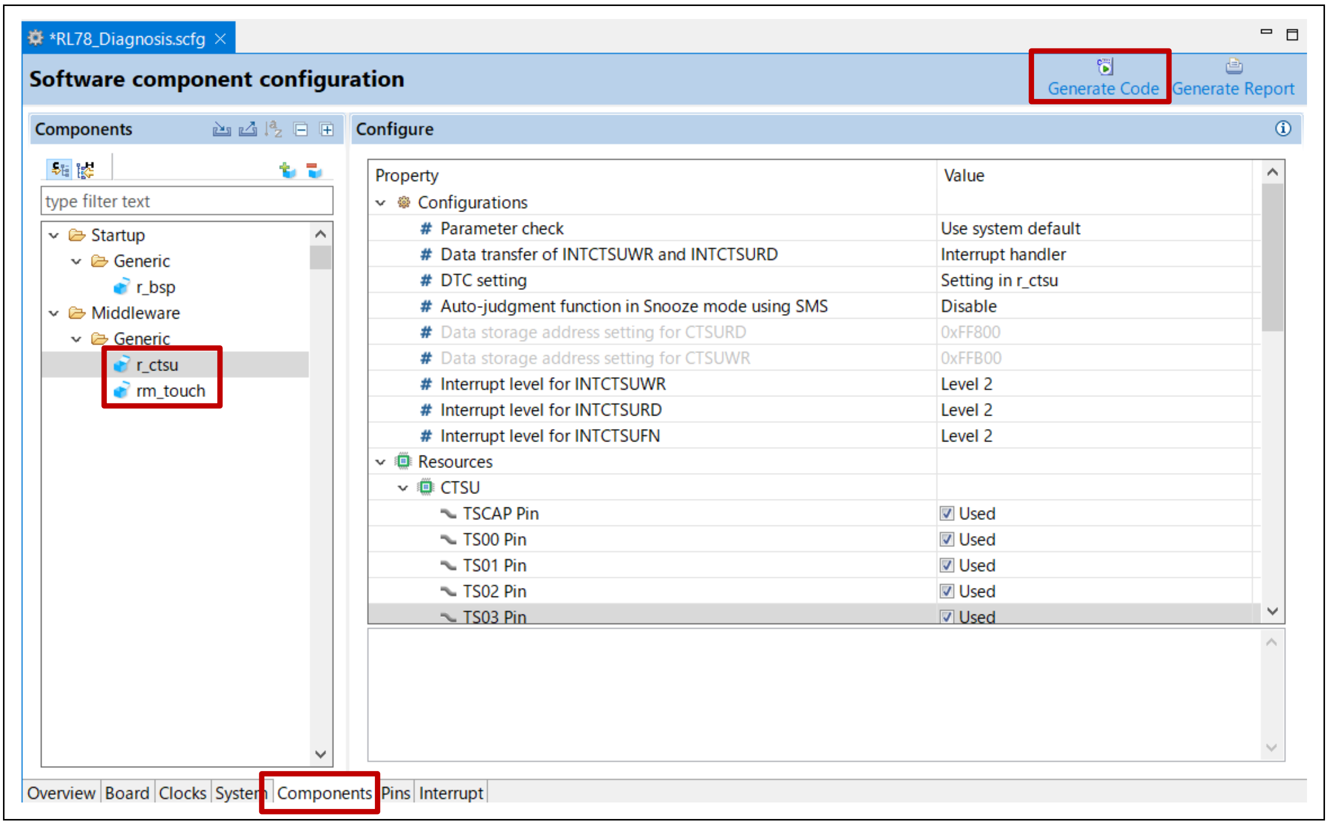

Figure 6.11 Software component configuration view

6.3 RX Family

1) Create a new project.

2) Add a component in the configurator.

Add touch middleware as shown in Figure 6.12.

* Additional settings required when using CTSU2

Add ADC driver “r_s12ad_rx” as shown in Figure 6.13. Also, don't need to select an ADC pin (ANxxx).

3) Generate code.

Click Generate Project Content in the upper right corner of the Configurator.

4) Create a configuration with QE.

Same as “6.1 RA Family” [(6) Create a configuration with QE].

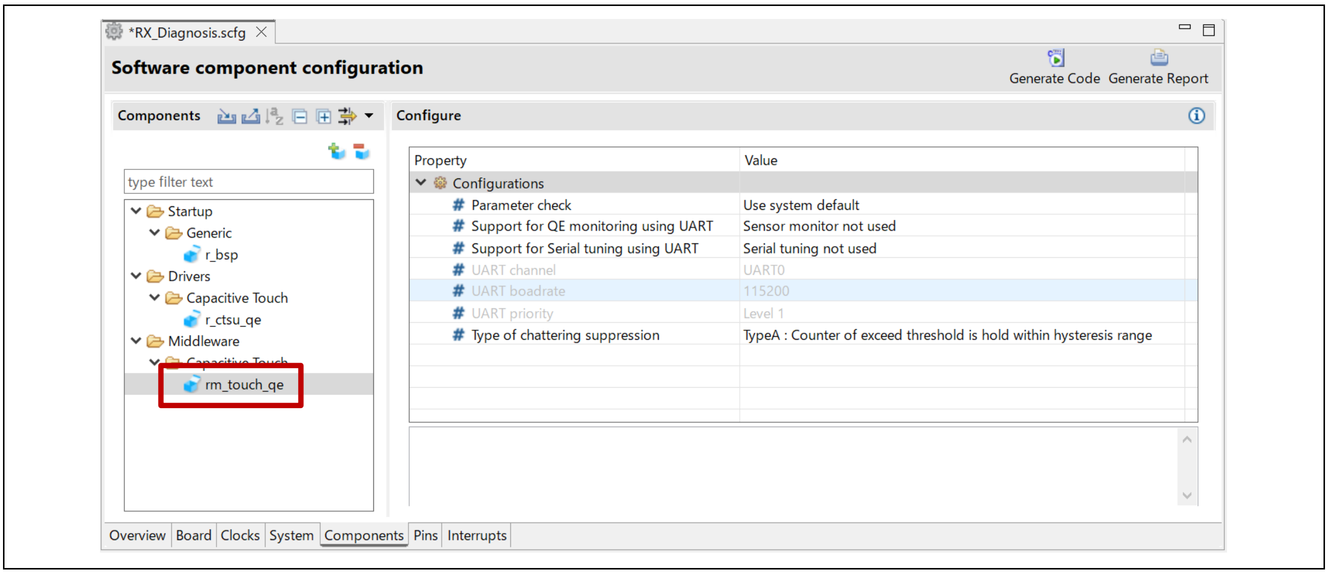

Figure 6.12 Add touch middleware in Software component configuration

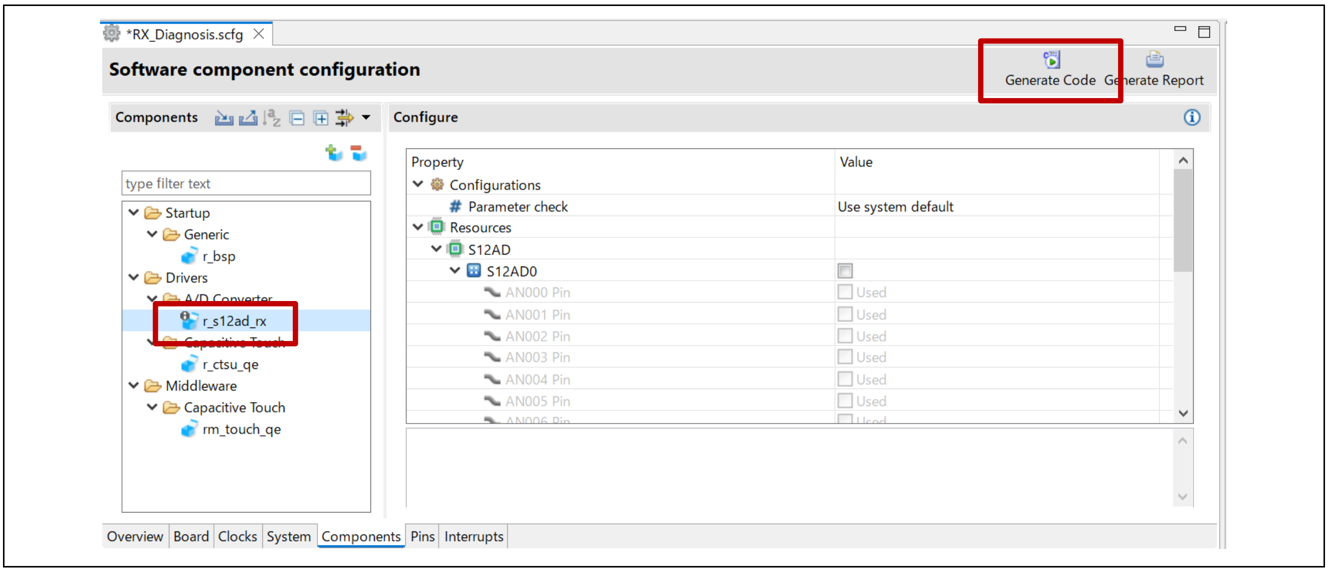

Figure 6.13 Add ADC driver “r_s12ad_rx” in Software component configuration

Revision History

Rev.	Date	Description	
		Page	**Summary**
1.00	Oct.25.21	-	First edition issued
1.10	Mar.31.23	-	Added target device
1.20	Oct.16.23	-	Added target device
		5	Added test for CTSUb
		8	Corrected current value
		10	Corrected CTSU figures
		12	Added test for CTSUb

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
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