RA6W1 PSRAM Integration

This application note describes the hardware integration of PSRAM on RA6W1 EVKs and how to use the FSP stack(s) for quick development. The PSRAM device from vendor AP Memory is used for reference implementation.

Contents

Figures

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1. Terms and Definitions

PSRAM	Pseudo Static Random Access Memory
QSPI	Quad Serial Peripheral Interface
EVB	Evaluation Board
FSP	Flexible Software Package

2. References

[1] RA6W1 Datasheet, Renesas Electronics.
[2] RA6W1 DEVKT Electric Schematic, Renesas Electronics.
[3] RA6W1 EVK Hardware Description, Manual, Renesas Electronics.
[4] RA6W1 FSP Documentation, Renesas Electronics.
[5] APS6404L-SQRH, Datasheet, Rev. 3.6, (https://www.mouser.com/datasheet/2/1127/APM_PSRAM_QSPI_APS6404L_SQRH_v3_6_PKG-1954817.pdf).
[6] RZ Ecosystem Partner Solution, AP Memory Octal SPI PSRAM Solution, (https://www.renesas.com/en/document/prb/ap-memory-octal-spi-psram-solutions-renesas-rz-partner-ecosystem).
[7] QSPI PSRAM Example application, (https://github.com/renesas/rafw-fsp-examples/releases/download/rafw_fsp_v1.0.0.example.1/r19an0442ee0100-ek-ra6w1-exampleprojects.zip).

Note 1 References are for the latest published version, unless otherwise indicated.

3. Introduction

RA6W1 is a highly integrated ultra-low-power Wi-Fi system on a chip (SoC) integrating an Arm® Cortex®-M33 system processor with a dual band 802.11 a/b/g/n/ax Wi-Fi-6 subsystem, on-chip memory, flexible peripheral interfaces, and power management features. The module has 704 kB of SRAM memory that is enough for IoT applications. Customer solutions requiring more random-access storage for applications can extend memory with integrating PSRAM. This document is intended to help new or existing users to quickly work with interfacing PSRAM into their solutions, with the EK-RQ61 EVB as a reference design.

4. QSPI PSRAM Overview

The PSRAM device used with the referenced EVK is APS6404L-SQRH—QSPI PSRAM from AP Memory vendor. This PSRAM device features a high speed, low pin count interface and has four Single Data Rate (SDR) I/O pins. It operates in Serial Peripheral Interface (SPI) or Quad Peripheral Interface (QPI) mode with frequencies up to 133 MHz. The data input (A/DQ) to the memory relies on clock (CLK) to latch all instructions, addresses, and data. This device is most suitable for low-power and low-cost portable applications. It incorporates a seamless self-managed refresh mechanism, and because of this it does not require the support of DRAM refresh from system host. SPI/QPI PSRAM device is byte addressable. The device recognizes the following commands specified by the various input methods.

Table 1. QSPI PSRAM commands

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Addr	Wait Cycle	DIO	Max.Freq.	Cmd	Addr	Wait Cycle	DIO	Max Freq.
Read	'h03	S	S	0	S	33	N/A				
Fast Read	'h0B	S	S	8	S	84	Q	Q	4	Q	66
Fast Read Quad	'hEB	S	Q	6	Q	84	Q	Q	6	Q	84
Write	'h02	S	S	0	S	84	Q	Q	0	Q	84
Quad Write	'h38	S	Q	0	Q	84	same as 'h02				
Enter Quad Mode	'h35	S	-	-	-	84	N/A				
Exit Quad Mode	'hF5	N/A					Q	-	-	-	-
Reset Enable	'h66	S	-	-	-	-	-	-	-	-	84
Reset	'h99	S	-	-	-	-	-	-	-	-	84
Half Sleep Entry	'hC0	S	-	-	-	84	N/A				
Read ID	'h9F	S	S	0	S	33	N/A				

The regular use case does not involve executing commands directly. But the `Read ID` command is particularly useful to read device information. This is explained in Section 8 QPSI PSRAM Example Application.

5. Hardware Integration

RA6W1 EVK has reserved U203 location for additional expandability requirements.

5.1 Specification for PSRAM

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage to any ball except VDD relative to VSS	VT	-0.4 to VDD+0.4	V
Voltage on VDD supply relative to VSS	VDD	-0.4 to +2.45	V
Storage Temperature	Tstg	-55 to +150	°C

5.2 AC Characteristics

Table 3. READ/WRITE Timing

Symbol	Parameter	Min	Max	Unit
t_{CLK}	CLK period - SPI Read ('h03)	30.3		ns
	CLK period - QPI Read ('h0B)	15.1		ns
	CLK period - all other operations	7		ns

For more detailed DC specifications, see Section 6 Power Consumption.

5.3 Reference Design with Compatible Part Number

AP Memory APS6404L-SQRH (Ref. 1) is a compatible part number. This is a 64 MB QUAD SPI serial RAM. APS6404L module needs to be mounted at U203, and the I/O voltage selection needs to be 1.8 V by configuring J101.

5.4 Part Assembly

Figure 1 shows the schematic for the referenced circuit and Figure 2 shows the placement position of the PSRAM (U203) on EVK. U203 part is placed but not powered or connected to the QUAD SPI I/O lines. You need to solder DNI resistors R27, R247, R248, R249, R250, R254, R256, R258 to enable U203 on EVK. All parts are 0402 package. For details, see Section 5.5 Wiring Notes.

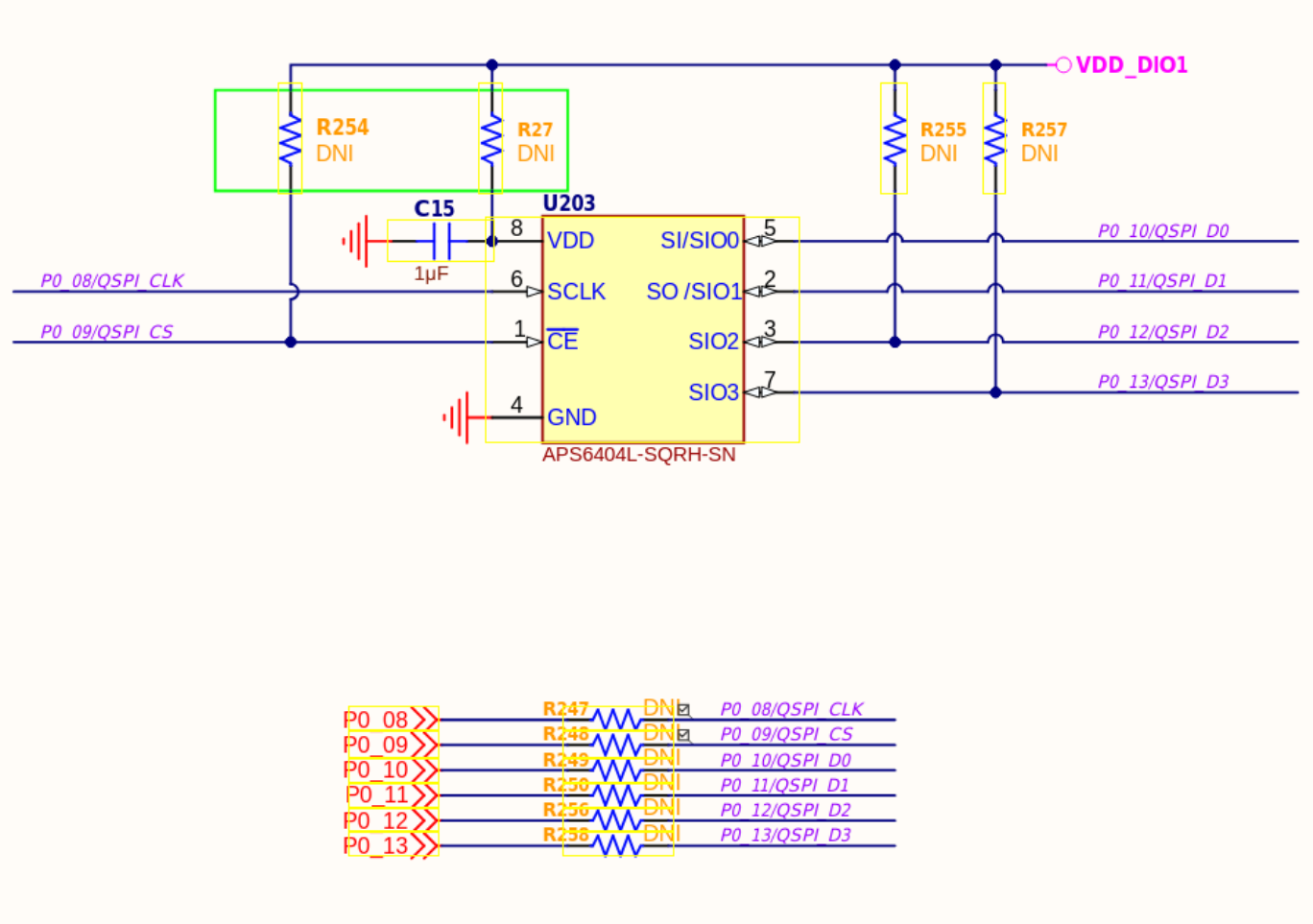

Figure 1. PSRAM Circuitry schematic

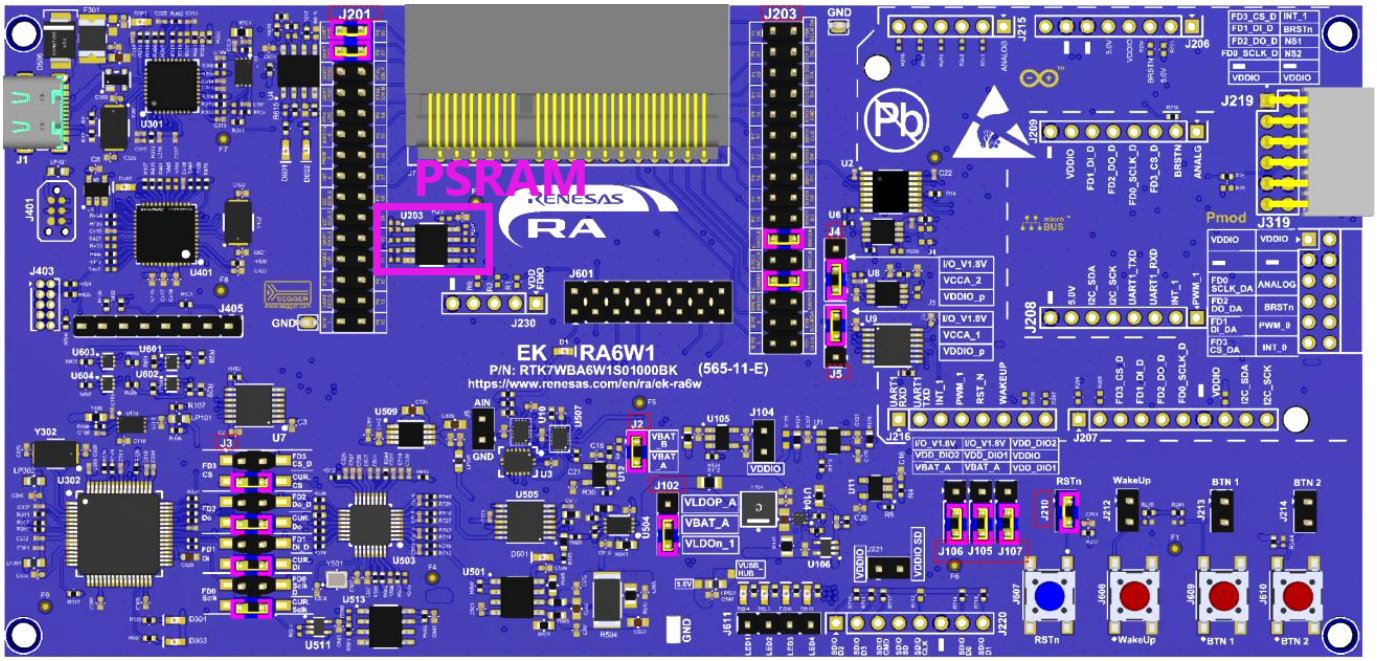

Figure 2. U203(PSRAM) Placement on EVK motherboard

5.5 Wiring Notes

The RA6W1 EVB (565-11-E) already has the U203 part (PSRAM) placed. To enable PSRAM:

- Mount R27 = 0R (0402)
- Mount R254 = 10K (0402)
- Mount R247, R248, R249, R250, R256 and R258 = 0R (0402)
- Mount pins 1-2 of J105 (For VDD_DIO1 = 1.8 V).

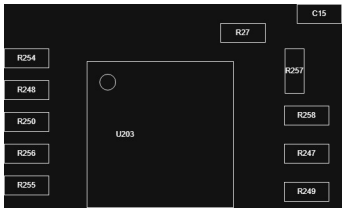

Figure 3. Resistor mounting

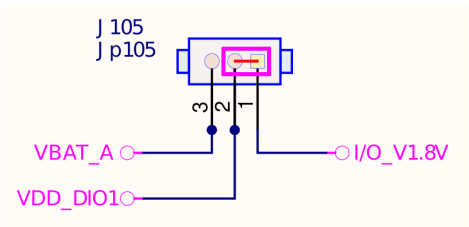

Figure 4. VDDIO jumper configuration for 1.8 V (schematic)

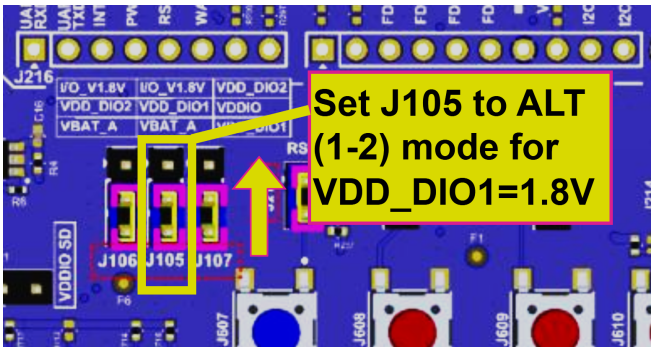

Figure 5. VDDIO jumper configuration for 1.8 V - EVB reference

6. Power Consumption

In the RA6W1 reference motherboard, power to the U203/PSRAM is supplied from VDD_DIO1 which is same as the power rail to the RA6W1 chipset. In this setup, power consumed by the PSRAM reflects in the overall power consumption of the system. This should be carefully noted if you are measuring the overall power consumption.
It is possible to exclude the power consumption of PSRAM. One way this can be done is by removing 0-Ω resistor mounted on R27 and soldering a wire to R27, as in the diagram below. I/O_V1.8V is 1.8 V and it is generated externally.

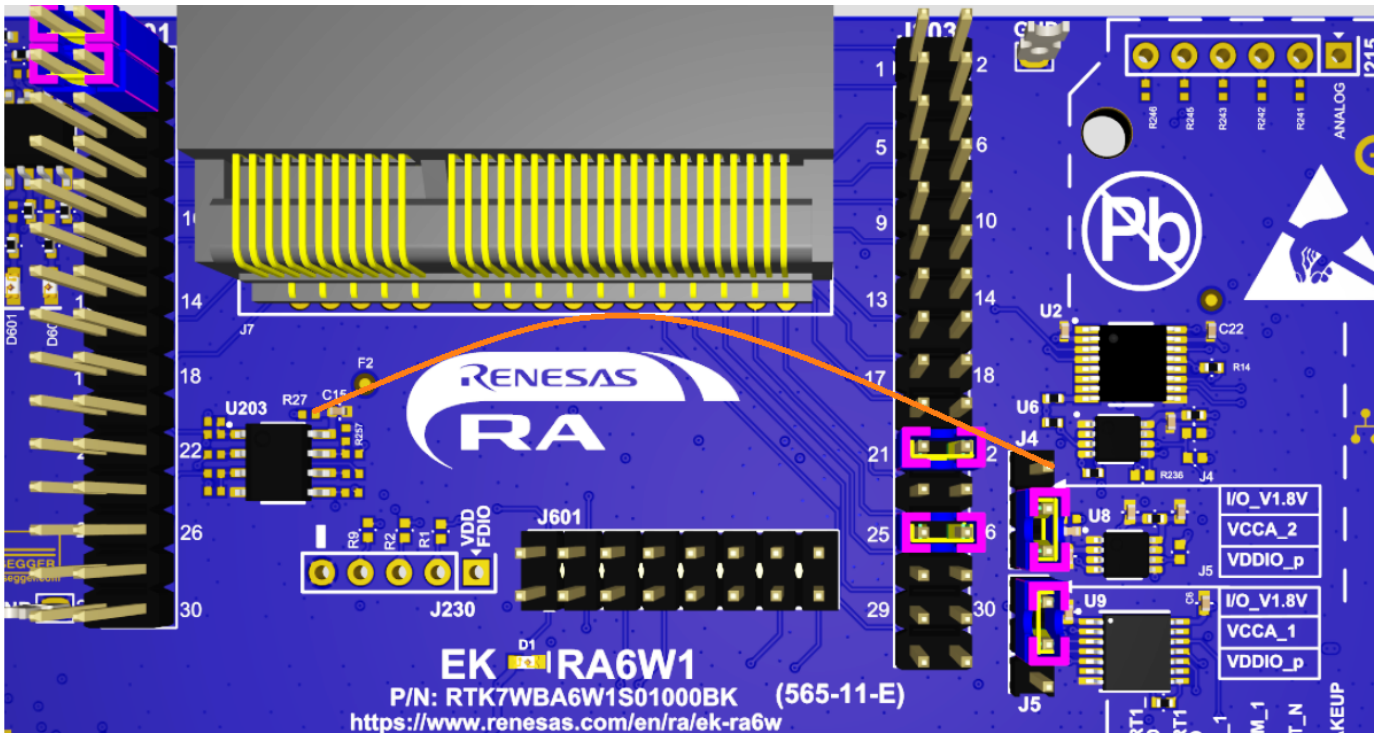

Figure 6. Alternate power source for PSRAM

Actual power consumption of PSRAM module depends on the part being used. Table 4 provides the ratings for APS6404L-SQRH.

Table 4. APS6404L-SQH, DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply Voltage	1.62	1.98	V	
V_{IH}	Input high voltage	V_{DD}-0.4	V_{DD}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DD}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DD}	V	
I_{LI}	Input leakage current		1	µA	
I_{LO}	Output leakage current		1	µA	
I_{CC}	Read/Write		7	mA	1,2
ISB_{EXT}	Standby current(105C)		300	µA	3
ISB_{STD}	Standby current(85C)		200	µA	3

Note 1 Output load current not included.

Note 2 50% bus toggling rate.

Note 3 Standby current is measured when CLK is in DC low state.

Note 4 Typical $ISB_{STDROOM}$ is 66 µA.

Note 5 Typical ISB_{STD_HS} is 20 µA.

7. Software Integration

The Renesas FSP stack for RA6W1 provides a ready-to-use clean APIs for seamless integration of PSRAM into application. The FSP stack provides multiple options to configure PSRAM peripheral to different application needs and to work with multiple vendor devices.

7.1 FSP Stack

To start using PSRAM peripheral, add the provided FSP stack by going to **Stacks** > **NewStack** > **Storage** > **QSPI RAM(r_qspi_w)**.

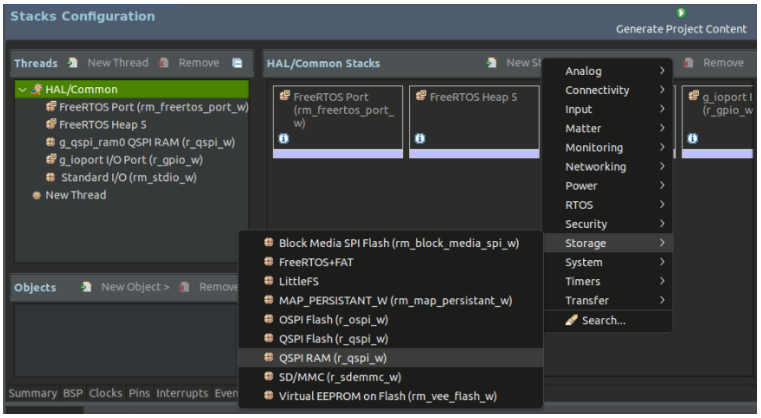

Figure 7. Adding QSPI PSRAM stack

7.2 Pin Configuration

The QSPI pins are auto assigned. When working with EVK, make sure to follow the guidelines below:

- Do not change **P0_08** - **P0_13** pin assignments.
- Do not assign alternate functions to **P0_08** - **P0_13** pins when PSRAM is integrated.

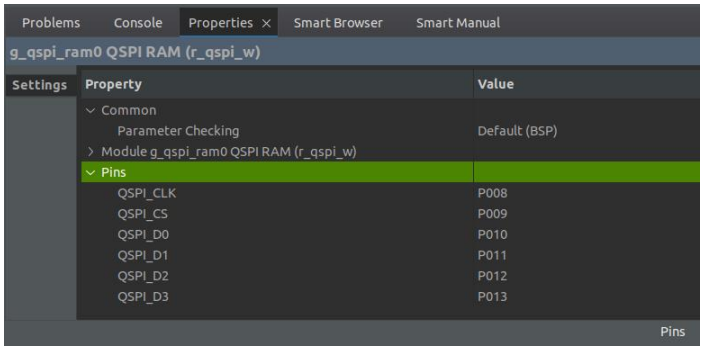

Figure 8. Default pin assignment for QSPI PSRAM

7.3 FSP QSPI-PSRAM Configuration Options

Many configurable options are available under FSP stack properties, see Table 5 and Table 6.

Table 5. General QSPI RAM configuration options

Option	Description	Value
Address Bytes	Length of address bytes.	3, 4, 4 with 4-byte read code
Read Mode	Read mode to be used.	Standard Read, Fast Read, Fast Read Dual Output, Fast Read Dual I/O, Fast Read Quad Output, Fast Read Quad I/O
Dummy Clocks for Fast Read	Dummy cycles for fast read.	Default, 0,2,4,6,8,12,16,24 (default 6 for Fast Read Quad I/O, 4 for fast read Dual I/O, 8 for Fast Read Quad Output, Fast Read Dual Output and Fast Read)
Data Cache	Enable data cache if supported by chip.	Enable/Disable
SPI clock mode	Supported SPI clock modes.	Mode 0, Mode 3

Table 6. Bus Timing related QSPI RAM configuration options

Option	Description	Value
QSPI_CLK Divisor	Clock divisor value	1, 2, 4, 8 – default 1
Minimum QSPI_CS Deselect Cycles		0-7 QSPI_CLK – default 4
Maximum Allowed Time of tCEM	Maximum allowed "Chip Enable maximum Time"	0-1023 – default 0

8. QPSI PSRAM Example Application

For quick development of PSRAM integrated applications, you can refer to the example application. This application demonstrates the use of "Read ID" command as well as basic read/write of entire 64 MB addressable memory region of APS6404L-SQRH chip.
Here is a sample log from the example application `r_qspi_w_psram_example_ek_ra6wx_ep` (for code, see Ref. 6).

```
r_qspi_w_psram_basic_example: EXAMPLE WITH APS6404L-SQRH QSPI PSRAM
ID: 0xd 0x5d 0x46 0xf6 0xf5 0xa1 0x9e 0x5c 0xd
Info:
        MF ID  : 0x0D
        KGD    : 0x5D
        Density: 0x02 (64M)

psram_full_range_wr_test: Full Region r/w example
Clearing 67108864 Bytes=65536KB=64MB
CLEAR: 1MB Block[64] OK, 100%
WRITE: 1MB Block[64] OK, 100%
READ: 1MB Block[64] OK, 100%
PASS [psram_full_range_wr_test]

psram_string_wr_test: String r/w example
String: read after write: string @offset 0x24000400 [TEST sTrING@#4512]
String: Read after erase: string @offset 0x24000400 []
PASS [psram_string_wr_test]

Total time=41679ms
```

8.1 READ ID Command

The Read ID command is used to enquire basic chip information. For AP Memory PSRAM devices, this command also returns the health of the chip - called KGD id or Known Good ID. You can use this value to check if the chip is good.
To issue a PSRAM command, use FSP APIs:

```
    uint8_t     buf[10];

    memset(buf, 0x0, sizeof(buf));
    buf[0] = QSPI_RAM_COMMAND_READ_ID;
    err = R_QSPI_W_DirectWrite(&g_qspi_ram0_ctrl, &buf[0], 4, true);
    assert(FSP_SUCCESS == err);

    memset(buf, 0x0, sizeof(buf));
    err = R_QSPI_W_DirectRead(&g_qspi_ram0_ctrl, &buf[0], 9);
    assert(FSP_SUCCESS == err);
```

To check if the chip is good, do the following:

```
    mfid = buf[0];
    kgd = buf[1];
    density = buf[2] >> 5;

    /* check if known good die (KGD) : 0b0101_0101=FAIL, 0b0101_1101=PASS
```

```
 * Refer: AP-memory APS6404L-SQRH QSPI PSRAM data-sheet,
 * Section: 10.4 SPI Read ID Operation */
if (kgd != 0x5D) {
    APP_PRINT_ERR("PSRAM Failed to detect, BAD KGD(Known-Good-Die) "
     "value(0x%02X)\n\r", kgd);
    return FSP_ERR_INVALID_DATA;
}
```

8.2 Coding Guidelines

8.2.1 System Verification

PSRAM write succeeds even if no hardware is present. It does not raise a segmentation fault either. You can only detect an issue if you read back and compare. You can use the code checks from Section 8.1 READ ID Command.

8.2.2 Working with continuous memory

To use the entire PSRAM block, load the predefined QSPI RAM address and access it through a pointer.

```
#define SZ_SRAM ((QSPI_W_DEVICE_END_ADDRESS - QSPI_W_DEVICE_START_ADDRESS) / 0x1U)
uint32_t i;
volatile uint8_t *t_address  = (uint8_t *) (QSPI_W_DEVICE_START_ADDRESS);

for (i = 0; i < SZ_SRAM; i++) {
    t_address[i] = (i % 256);
}

/* Read Back */
for (i = 0, j = 0; i < SZ_SRAM; i++) {
    if (t_address[i] != (i % 256)) {
        APP_PRINT_ERR("FAILED!: data mismatch %lu [%d != %lu]\n\r", i,
        t_address[i], (i % 256));
        return false; // FAIL
    }
}
```

8.2.3 Working with Strings

To work with strings, use regular C syntax:

```
/* Random  String load test */
const char t_sting[] = "TEST sTrING@#4512";
uint8_t *t_address = (uint8_t *)(QSPI_W_DEVICE_START_ADDRESS + 1024U);

strcpy((char *)t_address, t_sting);
APP_PRINT_INFO("String: read after write: string @offset %p [%s]\n\r",
            t_address, t_address);

if (strcmp((const char *)t_address, t_sting))
    return false; //FAIL

memset(t_address, 0x00, 1024U);

if (strcmp((const char *)t_address, t_sting) >= 0)
```

```
        return false; //FAIL
```

The code examples in Section 8.2.2 Working with continuous memory and Section 8.2.3 Working with Strings show that to use the PSRAM you do not need to issue QSPI read/write commands listed in Table 1.

9. Revision History

Revision	Date	Description
1.01	Jan 21, 2026	Updated link for QSPI PSRAM Example application in references.
1.0	Nov 30, 2025	First version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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