RAA227063 Application Overview

This application note explains the typical application of the RAA227063, and it includes a schematic, an external components guide, block diagrams, and recommendations for facilitating a robust motor control. Use this document with the RAA227063 datasheet for detailed IC information.

The design examples in this application note are a guide and should only be used after thoroughly evaluating the RAA227063.

Contents

1. Typical Application Circuit

1.1 Motor Control System Block Diagram

Figure 1 shows a typical motor control system block diagram. RAA227063 can work with various MCUs to drive 3-phase BLDC motor, either sensorless or with Hall Sensor or Encoder. It can also be used to drive a single-phase or 2-phase DC motor.

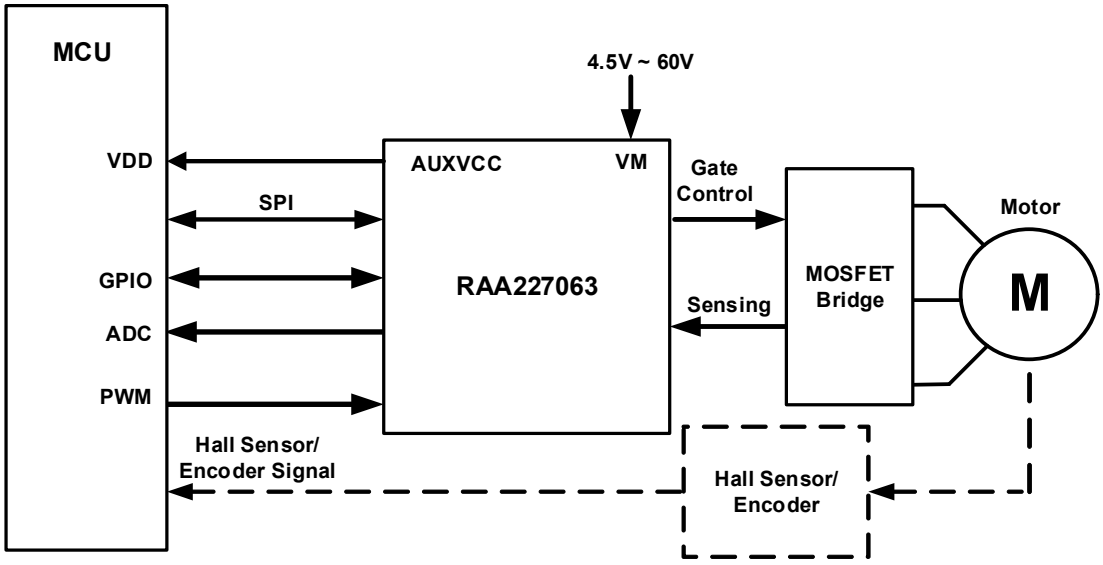

Figure 1. Typical Motor Control Block Diagram

RAA227063 receives PWM signals from MCU for driver control. The signals are for high-side and low-side driver control for each phase, HIx and LIx (x = A, B, C). When the device is configured in 3-phase HI/LI Mode, both side driver control signals need to be input from the MCU. When the device is configured in 3-phase PWM Mode, only high-side driver control signals need to be input from the MCU, which can save three MCU I/O ports. **Note:** The HIx and LIx (x = A, B, C) pins have internal pull-down resistance. However, when connected to MCU I/O ports, it is critical to initialize these MCU ports to low before enabling RAA227063. Enabling the device with the PWM output pins of the MCU in an undefined state can cause immediate part damage.

RAA227063 integrates three half-bridge smart gate drivers that are capable of driving up to three external N-channel MOSFET bridges and supports bridge voltage from 4.5V to 60V. GHx (x = A, B, C) pins (Pin 26, 31, and 37) output driver signals to control high-side FET gates, GLx pins (Pin 28, 33, and 38) output driver signals to control low-side FET gates. SHx pins (Pin 27, 32, and 36) connect to the switching nodes, which are the source of high-side FET, drain of low-side FET, in addition to motor phase winding.

RAA227063 has integrated buck-boost regulator that provides the gate driver voltage configurable from 5V to 15V. Its charge pump circuitry provides drive voltage for high-side FETs. It also provides power to the MCU through AUXVCC pin (Pin 44) that is configurable from 1.2V to 5V. Its 5V VCC pin (Pin 48) can also directly provide power to the MCUs that operate at 5V.

RAA227063 can support up to 3-phase shunt resistor current sensing with four amplifier gain settings, in addition to back-EMF sensing for sensorless motor control.

It has a Serial Peripheral Interface (SPI) to allow the MCU to program the device for all available settings. It also supports a Hardware Interface configuration that does not need any SPI programming from the MCU, which simplifies the system design and firmware development. See the datasheet for more details.

1.2 Application Circuit Example

1.2.1 System Schematic

Figure 2 shows a typical 3-phase motor control system schematic.

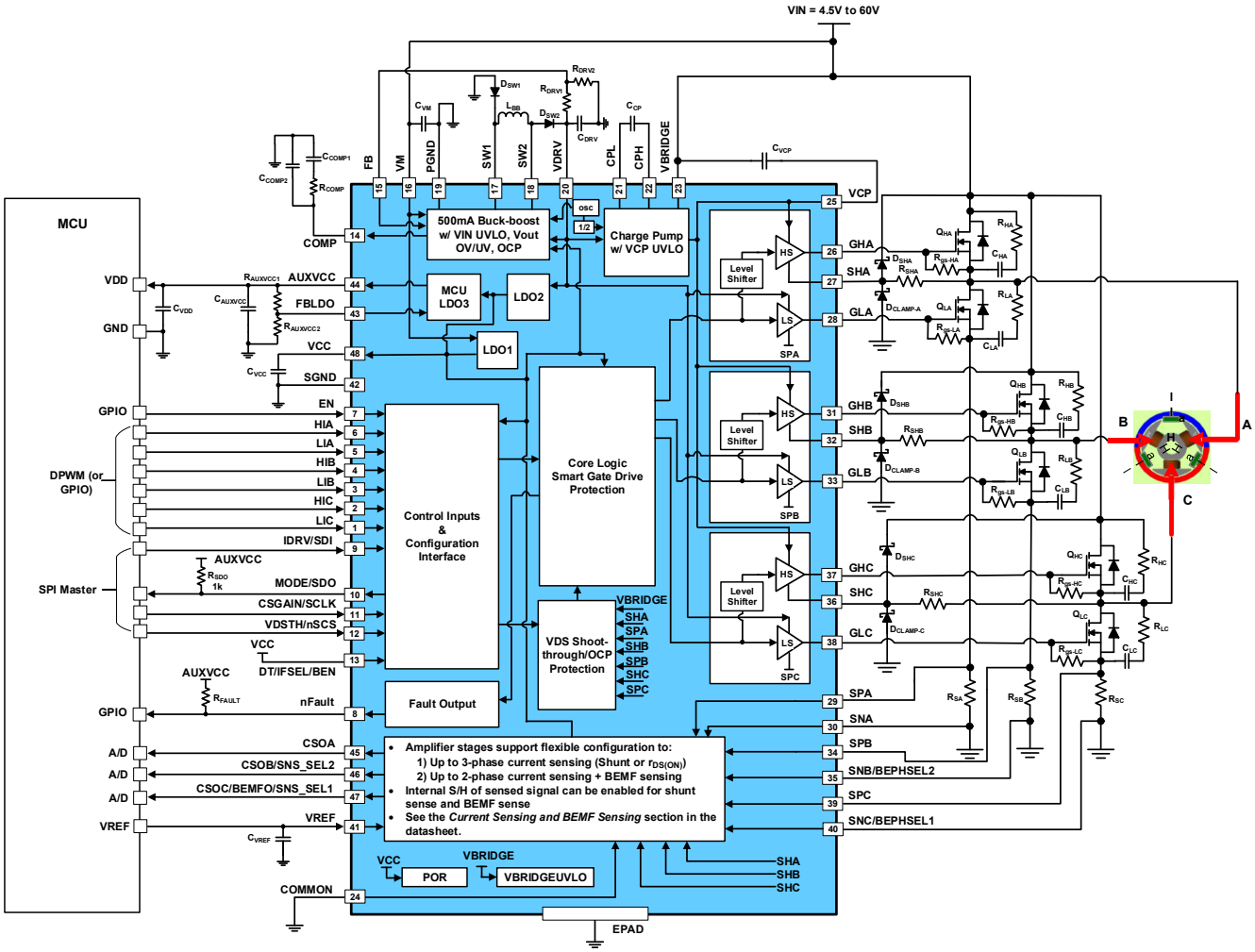

Figure 2. Typical 3-Phase Motor Control Schematic with RAA227063

1.2.2 Motor Phase Voltage Sensing Circuit

Motor phase voltage over the motor center tap, the Back Electromotive Force (BEMF) signal is needed for sensorless motor control. RAA227063 has a BEMF sensing feature with four configurable gain settings and Sample and Hold (S/H) time logic. The conditioned signal outputs to the MCU ADC through the CSOC/BEMFO/SNS_SEL1 pin (Pin 47).

You also have the option to directly connect the motor phases to the MCU ADC ports for BEMF sensing, as typically the motor center tap reference is grounded. Figure 3 shows a sample circuit that connects the motor phase node SHx (x = A, B, C) to the MCU ADC port. The sample resistor divider shown in the figure attenuates the phase voltage to 4.753%; therefore, for a 3.3V MCU application, the supported phase voltage covers the full RAA227063 operation range (up to 60V). Select the resistor divider ratio based on the operating voltage and the MCU ADC range in application. The capacitor helps filter out high frequency noise and the diode array protects the ADC port from out-of-range voltage levels.

The similar circuit can also be used for the MCU to sense system power (VM).

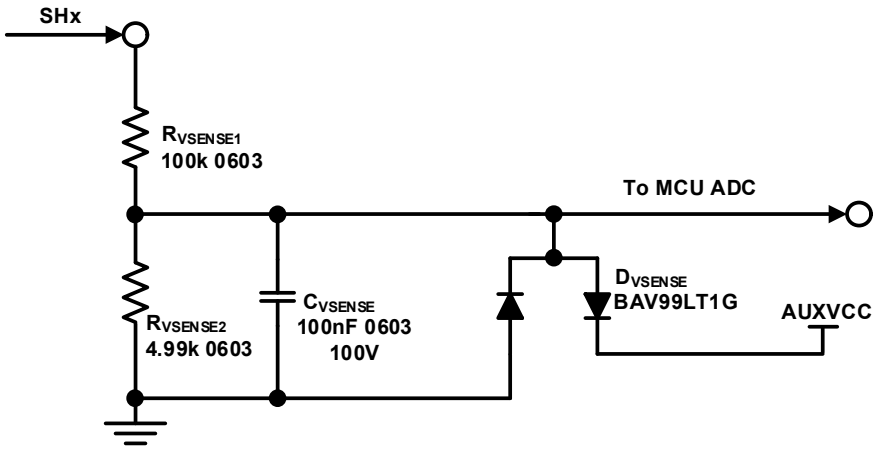

Figure 3. Direct Motor Phase Voltage (BEMF) Sensing Circuit Example

2. Configurations

2.1 Serial Peripheral Interface (SPI) and Hardware (HW) Interface

The RAA227063 works in either SPI or HW Interface. For the SPI configuration, all the parameters can be set through the SPI Bus, which allows finer configuration resolutions and better monitoring. For a HW Interface configuration, key driver operating parameters can be set using external resistor pin-straps.

To select the SPI configuration, connect the DT/IFSEL/BEN pin (Pin 13) directly to VCC. The RAA227063 SPI uses a 4-wire serial peripheral interface: nSCS (chip select, active low), SCLK (clock), SDI (data input), and SDO (data output). The SPI block of device only works in slave mode. In SPI configuration, the IDRV/SDI pin (Pin 9) is the data input pin for the device, the MODE/SDO pin (Pin 10) is the data output pin for the device, the CSGAIN/SCLK pin (Pin 11) is the SPI clock input pin, and the VDSTH/nSCS pin (Pin 12) is the SPI chip select pin. See the register map in the datasheet for the configuration through SPI Bus.

To select the HW Interface, connect the DT/IFSEL/BEN pin (Pin 13) directly to SGND or through a resistor. The resistor values decide the dead time (DT) configuration, and whether to enable the BEMF sensing feature. See the datasheet for detail settings.

In the HW Interface configuration, the IDRV/SDI pin (Pin 9) is used to configure driver peak source current (I_{src}). The MODE/SDO pin (Pin 10) is used to configure the device in the 3-phase PWM Mode or HI/LI Mode, and the current sensing configuration. The CSGAIN/SCLK pin (Pin 11) is used to select the shunt amplifier sensing gain. The VDSTH/nSCS pin (Pin 12) is used to select the VDS OCP threshold. See the datasheet for detail settings.

2.1.1 Handling an 8-Bit SPI Format

The RAA227063 SPI is designed in a 16-bit data format as described in the datasheet. However, it is possible to work with MCUs that only support 8-bit SPI data format. It can be done by sending/reading the 16-bit data as two 8-bit data through back-to-back two data transmissions with the clock not toggling between the two transmissions. The firmware can assemble the high 8-bits and low 8-bits back to 16-bit data.

2.1.2 SDO Pull-Up Resistor

Renesas strongly recommends using a pull-up resistor for the SDO line to AUXVCC for reliable communication, especially in higher clock applications. Ensure the SDO signal rising time is fast enough for correct data capturing at the clock being used. Figure 2 shows a 1kΩ R_{SDO} as an example in typical applications.

2.1.3 Multiple Devices on SPI Bus

When there are other slave device(s) sharing the SPI bus with the RAA227063, Renesas recommends adding a serial resistor (such as 500Ω) at each device SDO terminal to minimize interference. Another safer way is using a nSCS signal to logically disconnect the SCLK signal to each device.

2.2 Different Sensing Configurations

The RAA227063 supports both ground-side shunt current sense and low-side $r_{DS(ON)}$ current sense, and BEMF sensing. There are three differential amplifiers (CSA, CSB, and CSC) that can separately support current sensing up to three phases. For BEMF sensing, the Phase C current sense amplifier (CSC) and another two dedicated amplifiers (A1 and A2) form the BEMF sensing signal chain. They are shown in Figure 4.

The motor BEMF can detect rotor position without the need for an encoder or hall sensor for cost savings. In a typical trapezoidal BLDC operation, only two phase bridges are energized at a given time. The third phase is in high-impedance state (both high-side and low-side MOSFETs are turned off). By sensing this phase node voltage and subtracting the motor center tap voltage from it, you can measure the BEMF signal of this third phase, which allows you to estimate the rotor position relative to this third phase. The point of interest is the zero-crossing of the BEMF, which is approximately halfway through one commutation period if the motor is running at a constant speed with no phase advance.

The device has built-in Sample and hold (S/H) function for all three amplifiers (CSA, CSB, and CSC) for current and BEMF sensing. They can be programed to suit the specific requirements of applications. Up to two phases of current sensing S/H can be triggered simultaneously. See the Sample and Hold Timing Logic section in datasheet.

If using the SPI configuration, there are nine current sensing and BEMF sensing configuration options you can choose from. They are selected by setting device registers. The options are limited to four if using the HW Interface. They are selected by the MODE/SDO and DT/IFSEL/BEN pin (Pin 10 and 13) configurations. They are detailed in datasheet.

2.2.1 Sensing Configuration 6

The following is an example of using Configuration 6, which is available in both the SPI and HW Interface configurations. In this sensing configuration, 3-phase current sensing are used without internal S/H. All three sensed signals are output continuously through the CSOA, CSOB/SNS_SEL2, and CSOC/BEMFO/SNS_SEL1 pins (Pin 45, 46, and 47) to the MCU ADC ports. The BEMF sensing support of the IC is disabled.

Figure 4 shows the high signal flow for Configuration 6, where the switches colored in red are ON (closed) permanently, and the switches in black are OFF (open) permanently. This allows CSA, CSB, and CSC amplifiers to sense Phase A, B, and C current through the shunt.

If using the SPI configuration (DT/IFSEL/BEN pin (Pin 13) is connected to VCC), set these register bit values through the SPI: BEMF_EN = 0b, CS_MODE = 0b, and CS_SH_EN = 0b. **Note:** These bit settings are actually all default settings, which means as soon as the device detects an SPI configuration at power up, it automatically sets at Configuration 6 by default.

If using the HW Interface configuration (DT/IFSEL/BEN pin (Pin 13) is not connected to VCC), connect the DT/IFSEL/BEN pin (Pin 13) to SGND through a 60.4kΩ or 120kΩ resistor. A 60.4kΩ resistor connection sets the Dead Time as 250ns and a 120kΩ resistor sets the Dead Time as 450ns. Also, connect the MODE/SDO pin (Pin 10) directly to VCC or to SGND. A connection to VCC sets the device in a 3-phase PWM Mode and a connection to SGND sets the device in a 3-phase HI/LI Mode.

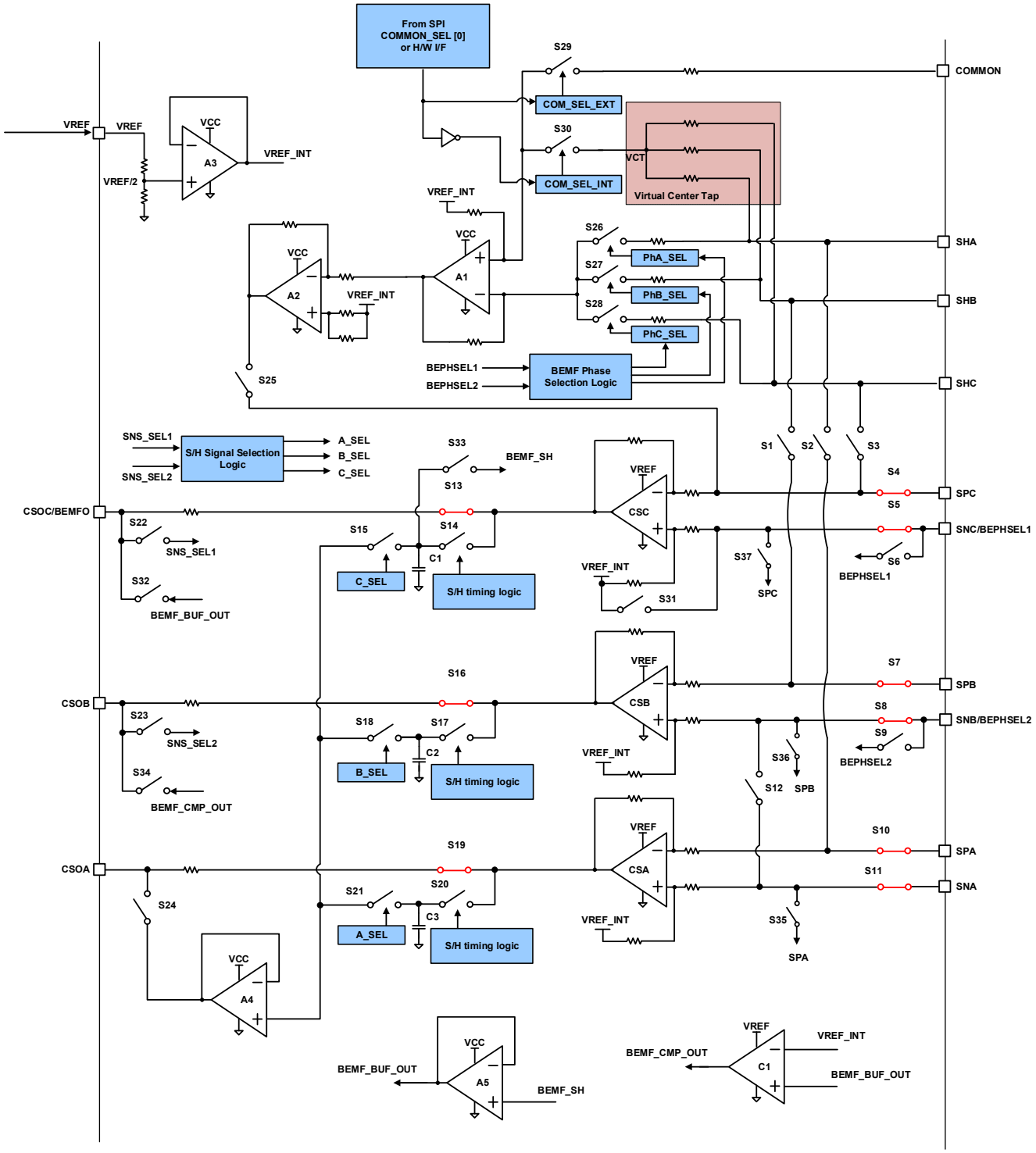

Figure 4. Signal Flow of Sensing Configuration 6

2.2.2 Sensing Signal Noises

Pay attention to the sensing signal noise level and apply a low-pass filter, if necessary. But also confirm the extra delay introduced by the filter is not causing a system response time issue. Figure 5 shows a low-pass filter example to reduce noises on the current sensing signal. Select the resistance and capacitance values for an appropriate cut-off frequency and acceptable delay.

During board layout design, make the SPx and SNx signal pair lines side by side as close as possible, and match their wire length to minimize their differential noises.

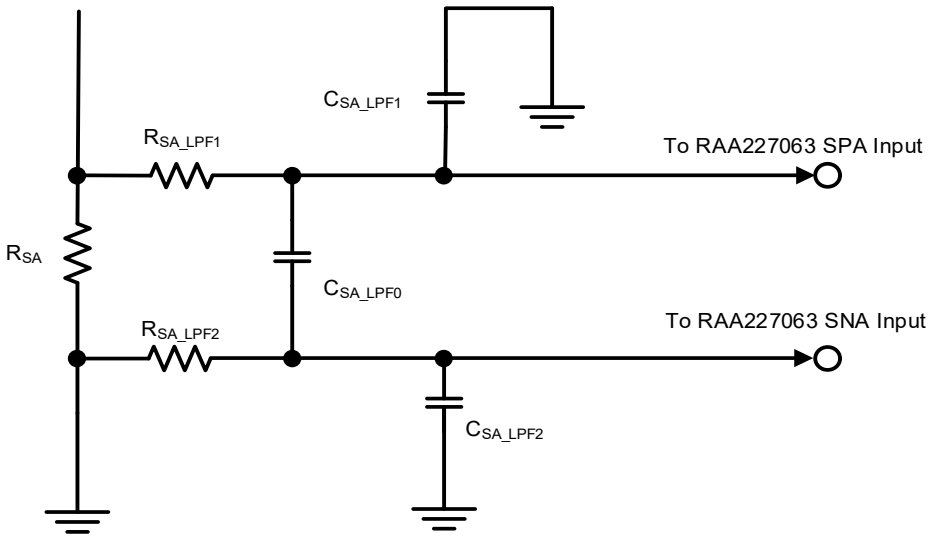

Figure 5. Low Pass Filter Example for Current Sensing

2.3 Field Oriented Control (FOC) Application

Field Oriented Control (FOC), also called vector motor control, gives the best motor control performance in terms of power efficiency. The RAA227063 fully supports FOC applications. For an MCU with a 3-channel simultaneous S/H ADC circuit (three shunt method), such as the Renesas RX family MCU, the RAA227063 can provide continuous three shunt resistor sensing signal through CSOA, CSOB, and CSOC pins (Pin 45, 46, and 47) directly to the MCU ADC inputs. Use the sample circuit shown in Figure 3 for BEMF sensing and Sensing Configuration 6 as described in section Sensing Configuration 6. For the MCU without a 3-channel simultaneous S/H feature, the RAA227063 can support up to two shunt simultaneous S/H for ADC in FOC implementation, or a 3-phase S/H with additional timing gap compensation in firmware.

Figure 6 shows a sample waveform of using the RAA227063 for FOC motor driving, where the motor phase current is showing nice sinusoidal shape.

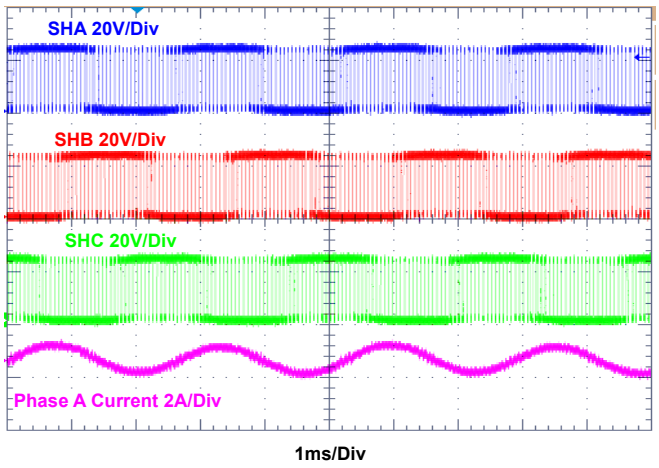

Figure 6. BLDC Motor Commutation with FOC, VM = 24V

3. Power Functions

3.1 Reverse Battery Protection

A reverse battery protection circuit is recommended in applications where the battery could possibly be accidentally connected in reverse polarity. Select and verify an appropriate protection circuit as necessary.

3.2 VM Capacitor Selection

A power source line needs capacitors to provide a low-impedance path for high frequency currents, in addition to stiffening the DC bus. It also prevents sharp voltage transient at system power-up. Larger capacitance can reduce the ripple so usually is preferred but it leads to large size and cost that are not wanted. The proper capacitance selection needs to consider the factors including but not limited to motor system operation voltage, switching frequency and required current capability, tolerable power source ripple, the type of motor, and its start/stop method.

As frequency goes up, the battery and cable parasitic inductance cause the impedance to increase. The local capacitor impedance goes down so it becomes the preferable path for high frequency AC to circulate. Select capacitor(s) based on the ripple current, bus voltage, resonant frequency, packaging, and cost constraints. Check analytically and run simulation to ensure that the capacitance meets the DC bus voltage ripple requirements.

In typical applications, place large electrolytic bulk capacitor(s) near DC power input, in addition to several MLCCs near IC VM and the VBRIDGE pins (Pin 16 and 23). Just as a reference, the Renesas evaluation board uses two 330µF 100V electrolytic capacitors at the DC power input, three 4.7µF 100V 1210 and one 0.1µF 100V 0603 in parallel at the VM pin, and one 4.7µF 100V 1210 and one 0.1µF 100V 0603 in parallel at the VBRIDGE pin.

3.3 VCC and AUXVCC Current Capacity and Configuration

The RAA227063 VCC is a 5V internal LDO output that supplies IC analog and logic bias. At startup, before the IC is enabled, VCC is powered by the LDO1 from VM. When the IC is enabled and the buck-boost regulator is running, VCC is obtained from LDO2 fed by VDRV. Renesas recommends placing a 10µF MLCC decoupling capacitor as close as possible between the VCC pin (Pin 48) and SGND. The VCC current limit is 220mA when the IC is enabled. **Important:** Pay attention to the current limit when the IC is not enabled, it is only 39mA.

AUXVCC is sourced from VCC so it has the same current limit as VCC in both the IC enable and sleep mode. In applications that intend to power the MCU and other circuits from VCC or AUXVCC when the RAA227063 in sleep mode, ensure the current requirement is not close to the sleep mode current limit of VCC/AUXVCC mentioned above.

AUXVCC can be configured from 1.2V to 5V (slightly lower). For an MCU using 5V, it is preferred to directly use VCC. To configure AUXVCC in different voltages, select a feedback resistance ratio at FBLDO ($R_{AUXVCC1}$ and $R_{AUXVCC2}$) to satisfy for Equation 1. The connection can be seen in Figure 2.

(EQ. 1) $$V_{AUXVCC} = V_{REF} \bullet \left(1 + \frac{R_{AUXVCC1}}{R_{AUXVCC2}}\right)$$

where:

- V_{REF} = 1.2V
- $R_{AUXVCC1}$ = High-side resistor divider
- $R_{AUXVCC2}$ = Low-side resistor connected from FBLDO to SGND

For example, if AUXVCC = 3.3V, select $R_{AUXVCC1}$ = 160kΩ and $R_{AUXVCC2}$ = 91kΩ. Larger feedback resistance leads to smaller sleep mode current, but generally it should stay below 1.5MΩ. One option for minimizing sleep mode current is to use an external circuit to disconnect resistor $R_{AUXVCC2}$ in sleep mode.

3.4 VDRV Voltage Configuration

VDRV is the output of the buck-boost switching regulator. It is the low-side driver supply and also supplies 200mA VCC LDO in operation mode. Its adjustable voltage range is 5V to 15V. The voltage is adjusted by external feedback resistors ratio (R_{DRV1} and R_{DRV2}) at the FB and VDRV pins (Pin 15 and 20), as shown in Figure 2. The resistor values can be selected using Equation 2 for the desired VDRV voltage.

(EQ. 2) $$V_{DRV} = V_{FB} \bullet \left(1 + \frac{R_{DRV1}}{R_{DRV2}}\right)$$

where:

- V_{FB} = 0.8V
- R_{DRV1} = High-side resistor divider
- R_{DRV2} = Low-side resistor connected from FB to SGND

As examples, for V_{DRV} = 12V, select R_{DRV1}= 48.7kΩ and R_{DRV2} = 3.48kΩ. For V_{DRV} = 8V, select R_{DRV1} = 47kΩ and R_{DRV2} = 5.23kΩ.

Note: Low VDRV voltage setting (such as 8V) is recommended for driving MOSFET with large input capacitance or any high voltage (30V and above), large power motor applications.

3.5 Buck-Only Application

The RAA227063 integrates a 500mA buck-boost switching regulator that generates drive voltage from 5V to 15V. It automatically switches between buck mode and boost mode based on input voltage VM minus output voltage V_{DRV}. When VM minus V_{DRV} difference is greater than 1.9V (buck to boost mode transition threshold), the regulator operates in buck mode. When VM minus V_{DRV} difference is smaller 1.6V (boost to buck mode transition threshold), the regulator operates in boost mode.

In applications that VM minus V_{DRV} difference is guaranteed greater than 1.9V (plus some margin), a buck-only configuration can be adopted to save the external buck diode. Figure 7 shows an example of buck-boost regulator external circuit. For buck-only application, the buck diode D_{SW2} between SW2 (Pin 18) and the VDRV pin (Pin 20) can be removed. The inductor L_{BB} can be directly connected between SW1 (Pin 17) and the VDRV pin. Renesas recommends grounding the SW2 pin, which is shown as the red lines in the figure.

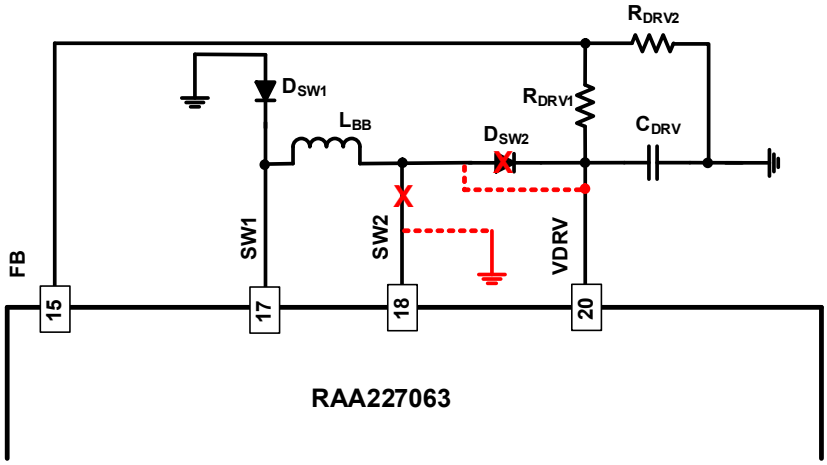

Figure 7. Circuit Example for Buck-Only Application

Figure 8 gives a waveform sample of V_{DRV} (12V) and SW1, with SW2 pin grounded and VM = 17V.

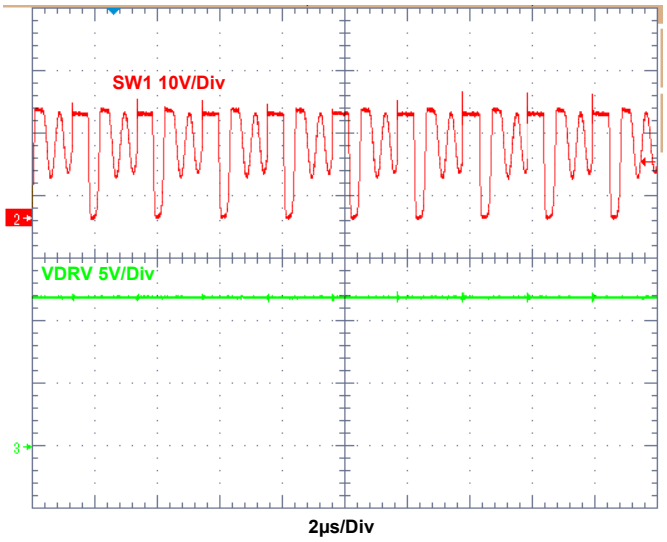

Figure 8. Buck-Only Operation with SW2 grounded, VM = 17V

4. Extra Protection Circuit Examples

4.1 Motor Phase Resistor Diode Clamp

During motor operation, gate switching dead time is applied to prevent both high-side and low-side FETs from being turned on at the same time (shoot through). After high-side FET is off but before low-side MOSFET is on, current from the motor flows through low-side FET body diode and causes negative voltage spike on the motor phase nodes. Figure 9 shows a sample waveform of switching motor phase voltages. Large negative spikes are observed at the falling edge. The RAA227063 has the negative voltage rated on SHx (x = A, B, C) pins (Pin 27, 32, and 36) as -5V. The negative spikes presented can exceed the negative voltage rating and cause damage.

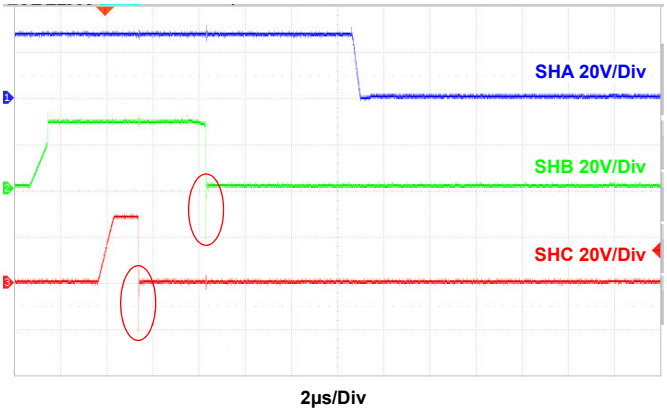

Figure 9. Switching Phase Voltage With Large Negative Spikes, VM = 24V

The negative spike magnitude is system dependent that can be affected by many factors including operating voltage, dead time, slew rate, component parameters of MOSFET, sensor resistor, and motor, in addition to the PCB layout. To avoid large negative spikes exceeding the rated negative voltage of the IC, a resistor diode clamp on the motor phase is necessary to reduce negative spikes during gate switching. Figure 10 shows the example circuit for phase A, which consists of one resistor R_{SHA} and one Schottky diode $D_{CLAMP-A}$. Adjust the resistor values for better result. Apply the same circuit to Phase B and C as necessary.

Place the clamp diode and resistor close to the IC on the PCB during layout design. Adding an extra Schottky diode close to FET is also beneficial.

An extra diode from the motor phase to VBRIDGE (D_{SHA} as shown in Figure 10) can prevent large positive spikes. Use this protection when necessary.

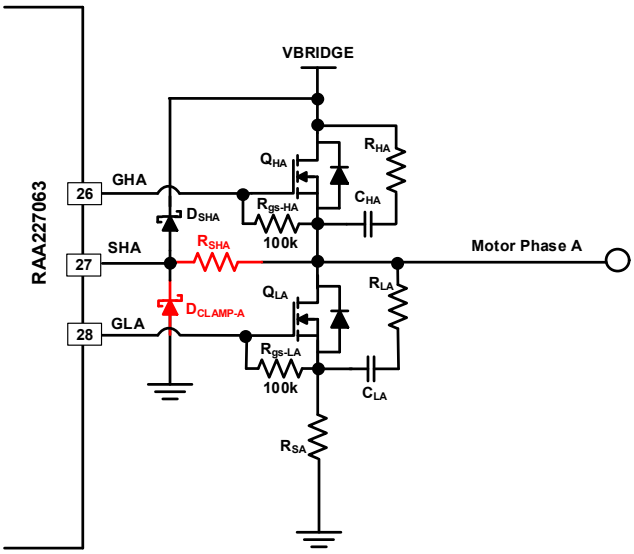

Figure 10. Resistor Diode Clamp on Motor Phase

Figure 11 shows a sample waveform of switching motor phase voltages, when the large negative spike issue is solved.

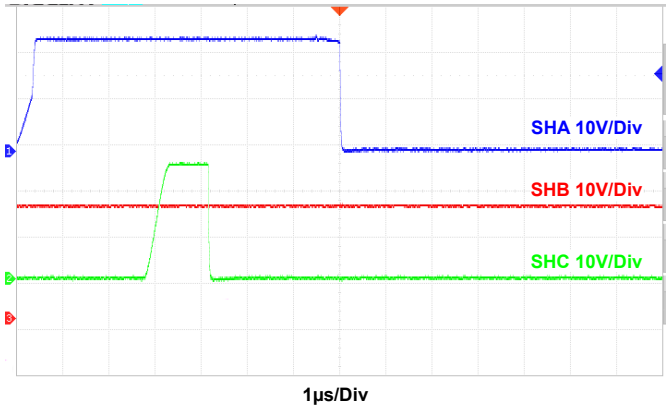

Figure 11. Switching Phase Voltage With Large Negative Spike Issue Solved, VM = 24V

4.2 MOSFET Gate Source Bypass Resistors

To allow quick discharge of the gate source voltage (V_{gs}) when MOSFET is tuning off, external gate source bypass resistors are recommended for MOSFET with larger input capacitance Ciss, and/or there are extra capacitances on the gate line. Potential shoot through event may occur if the input capacitance are holding V_{gs}.

Figure 12 shows an example of external 100kΩ gate source bypass resistors R_{gs} for Phase A MOSFETs. Apply same circuit to Phase B and C as necessary.

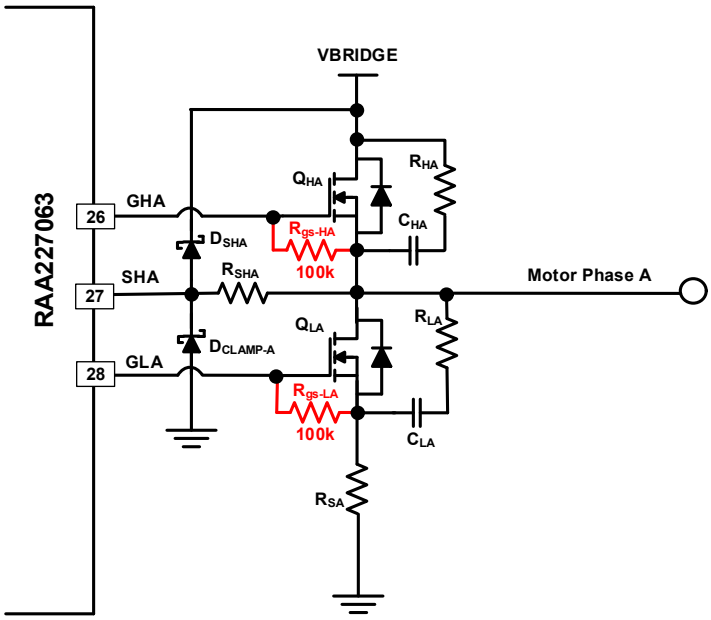

Figure 12. External Gate Source Resistor for the MOSFETs

4.3 MOSFET Snubber Circuit

Snubber circuits suppress transient voltages that occur during MOSFET turning off. Usually, a simple RC snubber shown in Figure 13 connected in parallel with the MOSFET serves the purpose. Apply the snubber to switching MOSFETs as necessary.

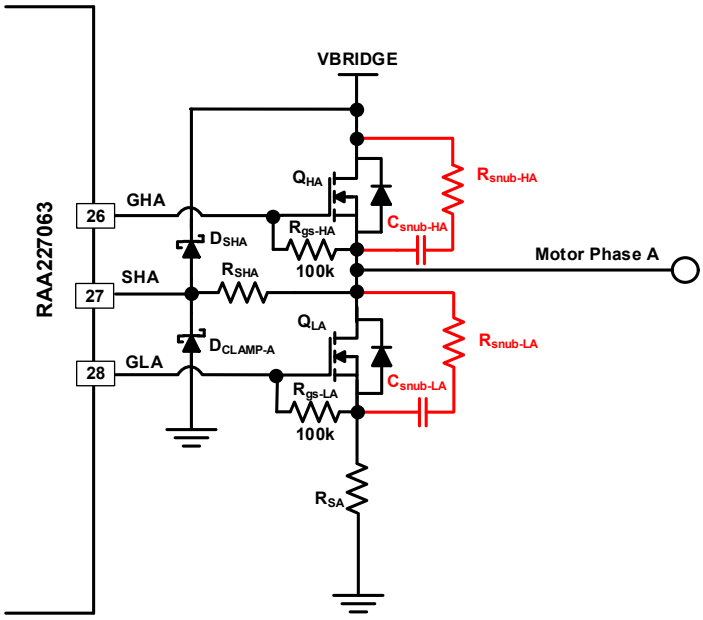

Figure 13. RC MOSFET Snubber Circuit

Note: The snubber circuit induces extra power loss because of the snubber capacitance being charged and discharged every switching cycle. Pay extra attention in power sensitive applications and only use the snubber, if needed. In many cases, a proper layout that minimizes the loop inductance can avoid using a snubber to suppress the transient.

5. Components and Parameters Selection Guide

5.1 Charge Pump Capacitors Selection

The charge pump output voltage VCP is the high-side gate driver supply. An external capacitor is needed between the CPL and CPH pins (Pin 21 and 22) as the flying capacitor for the charge pump operation, the C_{CP} shown in Figure 2. A 0.22µF MLCC allows the charge pump to supply up to 50mA that can cover the majority types of MOSFETs. A smaller C_{CP} causes more VCP voltage drop at a high load. Ensure the voltage drop at maximum load is acceptable for the motor operation if using smaller capacitance. Consider the required VCP capacity for the MOSFETs being used when selecting the capacitor value.

Equation 3 can be used to estimate the MOSFET drive current requirement (I_{VCP}) for 120° trapezoidal commutation, where Q_g is MOSFET total gate charge, f_{sw} is the PWM switching frequency.

(EQ. 3) $$I_{VCP} > Q_g \times f_{sw}$$

For 180° sinusoidal commutation, the I_{VCP} needs to be three times larger, as shown in Equation 4.

(EQ. 4) $$I_{VCP} > 3 \times Q_g \times f_{sw}$$

A minimum 1µF 25V MLCC capacitor connected from VCP pin to VBRIDGE pin is also required, shown as C_{VCP} in Figure 2. The recommended C_{VCP} are 10 to 15 times larger than C_{CP}.

5.2 Buck-Boost Inductor Selection

An external 33µH inductor is recommended for internal buck-boost switching regulator between the SW1 and SW2 pins (Pin 17 and 18). The regulator generates gate drive voltage (5V to 15V adjustable) with switching frequency of 500kHz. Depending on the load requirement and ripple tolerance, different inductor values maybe used, such as 10µH. Use the provided buck-boost regulator characteristics in the datasheet or check the Bode plot for stability if using low inductance.

The inductor value determines the ripple current of the regulator. Choosing an inductor requires a somewhat arbitrary choice of ripple current, ΔI. A reasonable starting point is 30% to 40% of the total load current. The inductor value is calculated using Equation 5, where VM and V_{DRV} are actually the input and output voltage of the regulator, f_{sw} = 500kHz, and L_{BB} is the inductor value for buck-booster regulator.

(EQ. 5) $$L_{BB} = \frac{VM - V_{DRV}}{f_{sw} \times \Delta I} \times \frac{V_{DRV}}{VM}$$

Increasing the value of inductance reduces the ripple current and therefore the ripple voltage. However, the larger inductance value may reduce the response time of the converter to a load transient. Also, the inductor current rating should not saturate in overcurrent conditions.

5.3 MOSFET Selection

The MOSFET is the critical component in motor control systems. Many factors need to be considered in the part selection. Not just MOSFET itself parameters, but also system operation power, efficiency requirement, airflow for heat dissipation, and system budget. For example, lower $r_{DS(ON)}$ is always preferred for better power efficiency. However, part package size, price, and system efficiency requirement also need to be considered. Gate capacitance and charge affect driving current requirement but switching frequency also directly affects the current requirement. MOSFET thermal coefficients affect heat generation but operating power and heat dissipation design also play a role.

To give an example, if f_{sw} = 45kHz, using 180° sinusoidal commutation and I_{VCP} = 30mA, the RAA227063 VCP can support high-side MOSFET with total gate charge Q_g < 222nC. The low-side MOSFET is driven by buck-boost regulator with much higher current capability, so it is less constrained.

5.4 GaN FET Application

Gallium Nitride (GaN) based FETs are significantly faster and smaller than traditional silicon MOSFETs. They can be used in applications aiming for high switching frequency, high power density, and high power efficiency because of low switching loss.

The RAA227063 can be configured to drive a GaN FET. The key factor that needs attention in GaN FET application is the gate drive voltage (V_{gs}), which must below the maximum rated V_{gs} of the FET, typically at 5.5V. Check the FET datasheet carefully. Some GaN FETs have slightly higher maximum V_{gs}. For example, the EPC2218 V_{gs} is rated as 6V maximum. Renesas recommends configuring V_{DRV} at 0.5V below the maximum rating for margin. See VDRV Voltage Configuration for more details with VDRV voltage configuration. A voltage clamp can also be used to limit V_{gs} voltage. Also, an external diode clamp from switching node to ground is needed for GaN FET protection.

5.5 Current Sense Resistor Selection

Current sense resistor accuracy directly affects the driving current measurement, which is a critical information in some applications like FOC. Select the sense resistor with low temperature coefficient, high accuracy (such as ±1%), and low inductance. Low inductance resistors, such as some long-side terminal ones, are beneficial to minimize switching noises and transients. **Note:** Pay attention to the layout from the sense resistor to IC. Use a low-pass filter as necessary for high frequency noise. However, do not use large resistance on the SPx pins (Pin 29, 34, and 39) as they are also the source terminals of the low-side MOSFETs, in addition to the internal ground of the IC for the low-side gate driver.

5.6 Drive Current Strength (Slew Rate) Selection

RAA227063 supports configurable 50mA to 1.1A gate drive sourcing current and 130mA to 2.4A sinking current. In the SPI configuration, there are 16 settings. In the HW Interface configuration, there are 8 settings. This provides flexible adjustment of the MOSFET switching slew rate, which is a critical factor for switching transients such as switching node spikes, system electromagnetic interference (EMI) emission, acoustics, and power efficiency.

The gate drive current strength can be selected based on the gate-to-drain charge of the MOSFETs and the target rise and fall times at the outputs, in addition to the overall system performance regarding the factors previously mentioned. The drive strength setting needs to be high enough to ensure the MOSFET gates are fully turned on and off in each cycle, but not causing any switching transient and EMI concerns. Normally, faster slew rate normally increases power efficiency but also increase system transient noises and EMI emission.

For MOSFETs with known gate-to-drain charge Q_{gd}, the required rise time (t_{rise}), and fall time (t_{fall}), the following equations can be used as guidelines for selecting the source current strength (I_{src}) and sink current strength (I_{snk}).

(EQ. 6) $$I_{src} > Q_{gd} / t_{rise}$$

(EQ. 7) $$I_{snk} > Q_{gd} / t_{fall}$$

5.7 Adaptive Dead Time (Self-Align Dead Time)

The RAA227063 has Adaptive Dead Time, also called a Self-Align Dead Time (SADT) generator, in addition to additional adjustable dead time functions to ensure robustness and flexibility. They prevent shoot-through (short-circuit) events in gate driver.

Adaptive dead time control is implemented by actively monitoring the gate voltage of the MOSFET that is turning off first during the transition. The complementary MOSFET is allowed to start turning on only after it drops below the threshold (1V typical). Do not insert a large resistor on the gate line that may affect threshold detection accuracy. In addition to adaptive dead time, you can add extra dead time (t_{dt}) by setting either through the DT/IFSEL/BEN pin (Pin 13) in the Hardware Interface configuration or through SPI DEAD_TIME[0:1] bits.

When the input PWM signal from MCU has an inserted dead time shorter than a RAA227063 configured dead time, the shorter dead time from the device is the effective dead time.

When the input PWM signal from MCU has an inserted dead time longer than a RAA227063 configured dead time, the longer dead time from MCU is the effective dead time.

5.8 VDS OCP Threshold Setting Selection

The RAA227063 has drive overcurrent protection (OCP) for safe operation. It can be fulfilled either by monitoring the voltage across external current sense resistor or by MOSFET drain and source (VDS) when it is turned on. VDS OCP is mainly for overload. The IC has 16 settings in SPI configuration and 8 settings in HW Interface configuration for VDS OCP threshold setting, range from typical 33mV to 2156mV. The threshold selection can use the following equation as a guideline, where I_{max} is the expected maximum drive current, and $Rdson_{max}$ is the maximum MOSFET $r_{DS(ON)}$.

(EQ. 8) $$VDS\_TH > I_{max} \times Rdson_{max}$$

5.9 CS OCP Threshold Setting Selection

The RAA227063 can monitor the voltage across external current sense (CS) resistor for drive overcurrent protection (OCP). The IC has eight settings in the SPI configuration and one setting in the HW Interface configuration for CS OCP threshold setting. The threshold selection can use the following equation as a guideline, where Rcs_{max} is the maximum current sense resistance.

(EQ. 9) $$CSOCP\_TH > I_{max} \times Rcs_{max}$$

6. Layout Guideline

6.1 Layout Considerations

- Place the input capacitors, buck diode, inductor, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high frequency decoupling ceramic capacitors close to the IC.
- If signal components and the IC are placed in a separate area to the power train, use full ground planes in the internal layers with shared small signal ground (SGND) and power ground (PGND) to simplify the layout design. Otherwise, use separate ground planes for SGND and PGND. Connect the SGND and PGND in single point close to the IC. Do not connect them anywhere else.
- Keep the loop formed by the input capacitor, the top and bottom FET of each motor phase as small as possible.
- Keep the current paths from the input capacitor to the buck diode, the power inductor, and the output capacitor as short as possible with maximum allowable trace widths.

- Place the GLx (x = A, B, C) pins close to the lower FETs. The low-side FETs gate drive connections should be short and wide.
- Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
- Place the VDRV capacitor close to the VDRV pin of the IC and connect its ground end to the PGND pin.
- Connect the PGND pin of the IC to the ground plane using a via. Do not directly connect the PGND pin to the SGND EPAD.
- Place the high-side gate drive components (charge pump capacitor) together near the IC.
- Use copper filled polygons or wide short traces to connect the junction of the upper FET, lower FET, and motor windings. Also, keep the SHx nodes connection to the IC short. Do not oversize the copper islands for SHx nodes. Because SHx nodes are subjected to high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
- Route all high-speed switching nodes away from the control circuitry.
- Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths including feedback resistors, current monitoring resistors and capacitors, loop compensation capacitors and resistors to this SGND plane.
- Use a pair of traces with minimum loop for current sensing connection. Keep these traces separated from gate driver output signals. Route the pairs side by side as close as possible, and match their wire length.
- Ensure the feedback connection to the output capacitor is short and direct.

6.2 Ground and EPAD Layout Guide

Ground and EPAD layout is critical for noise reduction and heat dissipation. The goal of good grounding design is to provide a stable reference without noise and other oscillations for the IC and its surrounding circuits.

A partitioning ground scheme, which means the digital, analog, and high power signals have their own separate ground areas, is preferred in mixed signal system. Those ground can be connected at a single point to ensure same voltage reference level, but can minimize noise coupling.

The RAA227063 PGND pin (Pin 19) is only the internal ground reference for the buck-boost regulator. Both the PGND and SGND (Pin 42) pins are connected to EPAD at the IC bonding. To avoid extra noise coupling into the IC, especially in high power applications, Renesas recommends connecting the PGND, SGND, and EPAD of the IC to quiet ground SGND, not noisy power switching ground PGND.

Renesas recommends using a dedicated continuous ground plane in multiple layer board design. This allows each signal to have the shortest return path and decreases coupling and interference. Renesas recommends minimizing the ground plane discontinuity by carefully routing signal traces, and place vias away from each other to prevent breaks in the plane.

6.3 Switching Noise Reduction

In a motor driving system, the MOSFET switching and motor drive signal ringing are the main source of noise on the PCB. Optimizing the inductance and parasitics of gate drive signal and its return loop is critical for noise reduction. To achieve the lowest inductance in the power loop, observe the symmetry in the component

placement, and to constrain the entire high frequency path in the top and first inner layer of the PCB as shown in Figure 14.

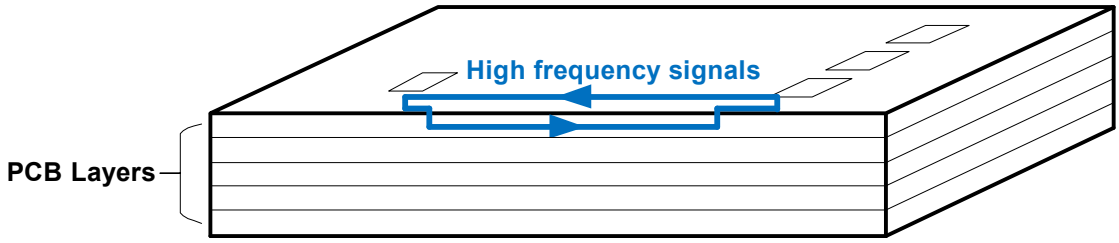

Figure 14. High Frequency Signal Layout Recommendation

6.4 Heat Dissipation

For better heat dissipation of the IC, use as large ground pad as possible for EPAD. Fill the thermal pad area with vias. A typical via array fills the thermal pad footprint so that their centers are three times the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents solder wicking through during reflow.

Connect all vias to the ground plane. The vias must have a low thermal resistance for efficient heat transfer. Ensure a complete connection of the plated through hole to each plane.

Figure 15 shows an example of how to use vias to remove heat from the IC.

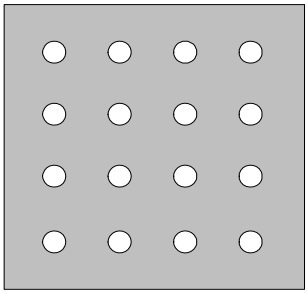

Figure 15. PCB EPAD Pattern

The typical thermal resistance coefficient of the IC is θ_{JA}= 25°C/W. This can be used to estimate the IC temperature rise based on system operation power. The drive power for each MOSFET is calculated using Equation 10:

(EQ. 10) $$P_{DRV} = Qg \times fsw \times V_{DRV}$$

As an example, for MOSFET with maximum total gate charge as Qg = 200nC, gate drive voltage V_{DRV} = 12V, and switching frequency of f_{SW} = 40kHz, the drive power for each MOSFET can be estimated as 0.096W. Multiply number of MOSFET that may be driven simultaneously, say 3, then total drive power of 0.288W can lead to 7.2°C temperature rise of the IC above the operating ambient temperature.

MOSFET can generate excessive heat due to conduction power loss plus the switching power loss. The conduction power loss is $r_{DS(ON)}$ multiplies square of RMS current through the MOSFET. The switching power loss is a function of switching frequency f_{SW}, MOSFET drain source current and voltage, MOSFET gate source and gate drain charges, and gate current. Its heat dissipation needs extreme attention. Select MOSFET package carefully based on power estimation, and reserve space for external heat sink if necessary when design component placement during layout.

6.5 EMI Reduction

Board layout and the electrical connection between the components affect the electromagnetic interference (EMI) performance in both radiated emission and conducted emission. In AC/DC power supply applications, both radiated and conducted emission need to meet the industry electromagnetic compatibility (EMC) standards. For battery operated applications, only radiated emission needs attention.

For conducted emissions, CEI EN 55022 standard specifies the limits for both class A (products marketed for commercial or industrial use) and class B (product marketed for residential or domestic use) devices in the 150kHz to 30MHz frequency range. The conducted emissions are usually measured in terms of proportional noise voltages and the standard limits. Conducted emissions are measured using a line impedance stabilization network (LISN) in series with power cord.

Radiated emissions are measured in terms of disturbance power. CEI EN55014-1 standard specifies the limits and the measurement methods of the disturbance power in the 30MHz to 300MHz frequency range for both quasi-peak and average values.

The power stage of the Motor control system involves high frequency switching, which is usually the major contributor to EMI. PCB layout aspects such as track length and width, circuit area, routing of the traces, arrangement of the components, and grounding scheme, can affect the EMI and need to be considered at board design. Reduce the EMI issues and voltage spikes because of parasitic inductances along the PCB traces. Minimize the switching nodes ringing is critical. Use a snubber circuit as described in MOSFET Snubber Circuit if necessary and select appropriate switching slew rate as discussed in Drive Current Strength (Slew Rate) Selection.

7. Revision History

Revision	Date	Description
1.01	May 25, 2022	Updated the Motor Control System Block Diagram section. Added the Multiple Devices on SPI Bus section to address multiple SPI slave devices application. Added the Sensing Signal Noises section. Updated the Layout Considerations section. Updated the VDRV Voltage Configuration section.
1.00	Aug 23, 2021	Initial release

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