RAA230161GSB Operation Manual

24V input, USB Voltage Supply for Power Delivery

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Description

RAA230161 (USB Voltage Supply) is the power supply IC for the power supply application with USB power delivery. This IC provides 5.3V to 20V power supply which are required in USB power delivery system. Power MOSFETs are included and maximum output power is 60W (20V, 3A). Various protection circuits are included to design safe system easily. The output voltage can be selected by I2C and the IC status can be monitored. The design of the power supply system with USB power delivery becomes easy by this IC.

Figure 1 shows the block diagram, and table 1 shows the pin description.

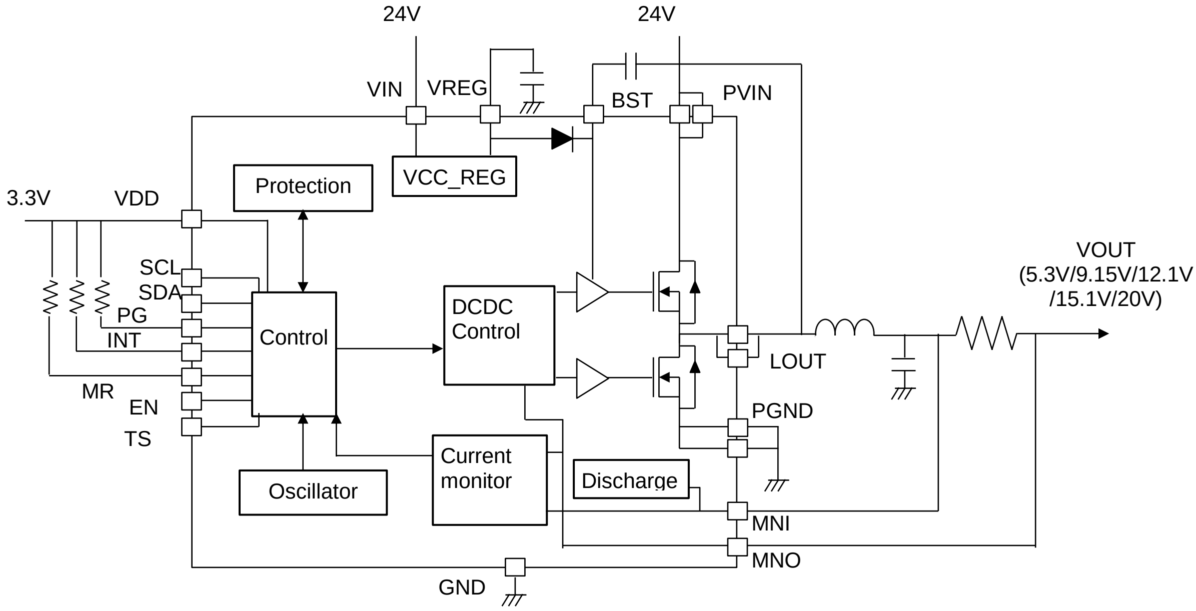

Figure.1 Block Diagram

Table.1 Pin Description

Pin No.	Symbol	I/O	Function
1	VIN	I	Power supply
2	VREG	I	Internal power supply output (For 1uF capacitor connection)
3	VDD	I	Power supply for I2C
4	GND	I/O	Ground
5	TS	I/O	Test pin
6	MNO	I	Monitor pin for controlling DCDC converter output voltage.
7	MNI	I	Monitor pin for DCDC converter output current.
8	EN	I	Device enable Note : Integrated pull down resister
9	SDA	I/O	I2C Data input and output
10	SCL	I	I2C Clock input
11	PG	O	Power good output Note : Open drain
12	MR	O	Reset signal output for microcontroller (Low active) Note : Open drain
13	INT	O	Status output (Low active) Note : Open drain
14	PGND	I/O	Power ground for DCDC converter
15	PGND	I/O	Power ground for DCDC converter
16	LOUT	O	DCDC converter output
17	LOUT	O	DCDC converter output
18	BST	I/O	Bootstrap pin
19	PVIN	I	Power supply for DCDC converter
20	PVIN	I	Power supply for DCDC converter

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1. Basic function

1.1 Connection diagram of power supply system

Figure 1.1 shows an example of power supply system using a power delivery controller and RAA230161GSB. RAA230161 operates as a slave. It requires a controller (PDC: Power Delivery Controller) as a master.

The system receives DC24 V as the input voltage from the primary power supply. A DCDC (other IC) generates 3.3V for the controller and VDD in RAA230161GSB. This 3.3 V (= VDD) is shared with the controller (master) for communication. RAA230161GSB controls VOUT output by EN control signal and I2C control signal, and outputs PG / INT / MR signal to the master as status monitor signal (safety function signal).

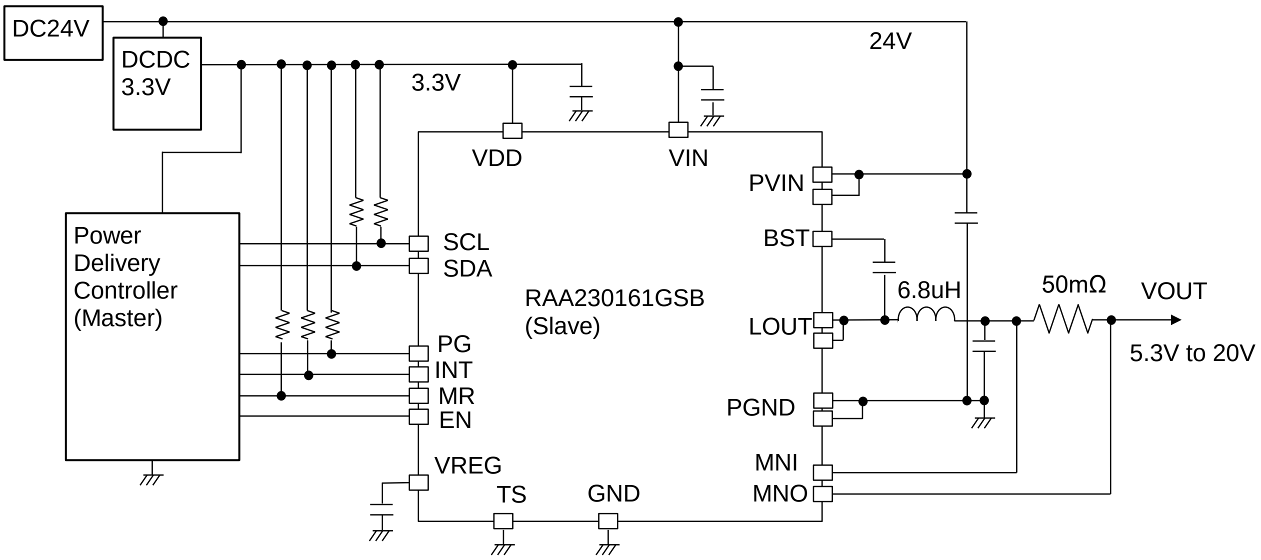


Figure 1.1 Connection of power supply system

1.2 Operation Mode

RAA230161GSB has 3 operation modes. The modes are decided by the DCON register status in the DCDC_ON register controlled by the I2C signal and the EN terminal input(Table 1.1).

Table 1.1 Operation Mode

Mode	INPUT		OUTPUT		
	EN terminal	DCON setting (DCDC_ON[D7])	VREG (IC internal power supply)	PG terminal status (Pulled up to VDD)	VOUT
OFF Mode	Low	I2C unavailable	OFF	High	OFF
STBY Mode	High	Low	ON	Low	OFF
ON Mode	High	High	ON	High (Low during output changing)	ON

<OFF Mode>

When EN = "Low", RAA230161GSB is OFF Mode. The IC internal power supply (VREG) doesn’t operate, so the I2C communication is unavailable and the internal register is cleared.

<STBY Mode>

When EN = "High", RAA230161GSB becomes STBY Mode. When VREG operates and the IC internal state stabilizes, the PG terminal outputs “Low” and I2C communication is available.

<ON Mode>

When EN = “High” and the DCON bit is “High”, RAA230161GSB becomes ON Mode. When the DCDC ON register is set by I2C, VOUT is changed to the set voltage. While the VOUT is being changed, the PG terminal outputs “Low”. The PG terminal outputs “High” when the VOUT stabilizes at the set voltage.

1.3 I2C register

Table 1.2 shows the register map of RAA230161GSB.

Table 1.2 Register Map of RAA230161

Address Name	Address Data [A7:A0]	Data Name								Function (*1)	Reset (*2)
		D7	D6	D5	D4	D3	D2	D1	D0		
DCDC_ ON	0000,0001	0(*3)	ISEL2	ISEL1	ISEL0	VSEL2	VSEL1	VSEL0	DCON	BBBBBBBB	00000000
Protect Flag	0000,0010	-	OVP_F	SCP_F	UVLO_F	-	OCP_F	OTP_F	WDT_F	- BBB- BBB	-000-000
Protect Status	0000,0011	-	-	-	-	-	-	-	PG	-RRRRRRR	-0000000
WDT SET	0000,0100	-	0	0	1	-	WDT1	WDT0	WDT_S	-RRR-BBB	-001-000
WDT RESET	0000,0101	-	-	-	0(*3)	-	-	-	WDT_R	- - - B - - - B	- - - 0 - - - 0
TEST-MODE	0000,0110	-	OVP_M	SCP_M	UVLO_M	0(*3)	OCP_M	OTP_M	0(*3)	-BBBBBBB	-0000000

*0) Slave Address = 1101111

*1) B：Write & Read bit ， R：Read only bit

*2) Initial value of the register

*3) Be sure to write "0"

1.3.1 Register and Bit data

- DCDC_ON(0×01) Register

This register controls VOUT. When "1" is written to the DCON bit (D0), VOUT starts up, and when "0" is written, VOUT stops. The VOUT voltage is set by the VSEL* bits (D3, D2, D1) and the maximum current of VOUT is set by the ISEL * bit (D6, D5, D4). Details of the setting are shown in Table 1.4 and Table 1.5.

Note : The D7 bit is the dedicated bit for test mode. Be sure to write "0".

Table 1.3 DCDC_ON Register

Address Name	Address Data [A7:A0]	Data Name								Function	Reset
		D7	D6	D5	D4	D3	D2	D1	D0		
DCDC_ON	0000,0001	0	ISEL2	ISEL1	ISEL0	VSEL2	VSEL1	VSEL0	DCON	BBBBBBBB	00000000

Table 1.4 VOUT maximum current setting (ISEL *)

ISEL Name	ISEL2 (D6)	ISEL1 (D5)	ISEL0 (D4)	VOUT Current Select
I005	0	0	0	0.5A
I010	0	0	1	1.0A
I015	0	1	0	1.5A
I020	0	1	1	2.0A
I025	1	0	0	2.5A
I030	1	0	1	3.0A

Table 1.5 VOUT voltage setting (VSEL*)

VSEL Name	VSEL2 (D3)	VSEL1 (D2)	VSEL0 (D1)	VOUT Voltage Select
V05	0	0	0	5.3V
V09	0	0	1	9.15V
V012	0	1	0	12.1V
V015	0	1	1	15.1V
V020	1	0	0	20V

- Protect Flag (0×02) Register

When the IC protection function operates, "1" is automatically written to the bits of each protection function, at the same time "0" is written to the DCON bit in the DCDC_ON register. Then VOUT stops. Table 1.7 shows a list of protect functions.

Table 1.6 Protect Flag Register

Address Name	Address Data [A7:A0]	Data Name								Function	Reset
		D7	D6	D5	D4	D3	D2	D1	D0		
Protect Flag	0000,0010	-	OVP_F	SCP_F	UVLO_F	-	OCP_F	OTP_F	WDT_F	-BBB- BBB	-000-000

Table 1.7 List of protect function

Data Name	Protect Function / Detection Condition	Operation status at protection			Reset
		Common circuit	DC/DC	Signal output terminal	
OVP_F (D6)	Over voltage protection VOUT > VSEL setting × 110%	Operation	Stop (Latch)	INT=L	By I2C
SCP_F (D5)	Short circuit protection VOUT < VSEL setting × 80%	Operation	Stop (Latch)	INT=L	By I2C
UVLO_F (D4)	Under voltage lockout VIN < 5.7V	Stop	Stop	-	Recover automatically as STBY mode when VIN >6.2V and EN="H"
OCP_F (D2)	Over current protection IOUT > ISEL setting × 120%	Operation	Stop (Latch)	INT=L	By I2C
OTP_F (D1)	Over temperature protection Tj > 165 ˚C	Operation	Stop (Latch)	INT=L	By I2C
WDT_F (D0)	Watch dog timer No reset signal input within WDT setting time	Operation	Stop (Latch)	Output single "L" pulse from MR terminal	By I2C

- Protect Status (0×03) Register

The same state as the PG terminal is written to the PG (D0) bit. PG terminal status can be monitored by reading the bit.

Table 1.8 Protect Status Register

Address Name	Address Data [A7:A0]	Data Name								Function	Reset
		D7	D6	D5	D4	D3	D2	D1	D0		
Protect Status	0000,0011	-	-	-	-	-	-	-	PG	-RRRRRRR	-0000000

- WDT SET (0×04) Register

This register controls the start-up of the watchdog timer (WDT). When “1” is written to the WDT_S bit (D0), the WDT counter starts counting. WDT stops when “0” is written to the bit.

The WDT reset time is set by the WDT * bit (D2, D1) in the register. Table 1.10 shows the details of reset setting time.

Table 1.9 WDT SET Register

Address Name	Address Data [A7:A0]	Data Name								Function	Reset
		D7	D6	D5	D4	D3	D2	D1	D0		
WDT SET	0000,0100	-	0	0	1	-	WDT1	WDT0	WDT_S	-RRR-BBB	-001-000

D6, D5, D4 bit are the internal management number

Table 1.10 WDT reset setting time (WDT*)

WDT Name	WDT1 (D2)	WDT0 (D1)	WDT Reset Time Select
W008	0	0	8.2ms
W033	0	1	32.8ms
W131	1	0	131ms
W524	1	1	524ms

- WDT RESET (0×05) Register

The WDT timer is reset by writing "0" to the WDT_R (D0) bit.

Note : The D4 bit is the dedicated bit for test mode. Be sure to write "0".

Tale 1.11 WDT RESET Register

Address Name	Address Data [A7:A0]	Data Name								Function	Reset
		D7	D6	D5	D4	D3	D2	D1	D0		
WDT RESET	0000,0101	-	-	-	0	-	-	-	WDT_R	- - - B - - - B	- - - 0 - - - 0

- TEST-MODE (0×06) Register

Each protection function is stopped by writing "1" to each bit in this register. Be careful to use the register because the protection circuit doesn’t operate.

Note : The D0 bit and the D3 bit are the dedicated bit for test mode. Be sure to write "0".

Table 1.12 TEST-MODE Register

Address Name	Address Data [A7:A0]	Data Name								Function	Reset
		D7	D6	D5	D4	D3	D2	D1	D0		
TEST-MODE	0000,0110	-	OVP_M	SCP_M	UVLO_M	0	OCP_M	OTP_M	0	-BBBBBBB	-0000000

1.4 I2C Data transfer

1.4.1 I2C Data transfer format

The maximum clock frequency of the I2C is 1.0MHz. Figure 1.2 shows the transfer data format, and Figure 1.3 shows the typical waveform.

<Data transfer from a master-transmitter>

S (Start Condition)
P (Stop Condition)
A (Acknowledge)

Write data transfer

S	SLAVE ADDRESS [1101 111]	R/W [0]	A	REGISTER ADDRESS [A7:A0]	A	WRITE DATA [D7:D0]	A	P

Read data transfer

S	SLAVE ADDRESS [1101 111]	R/W [0]	A	REGISTER ADDRESS [A7:A0]	A	S	SLAVE ADDRESS [1101 111]	R/W [1]	A	READ DATA [D7:D0]	A	P

Figure 1.2 I2C Data transfer format

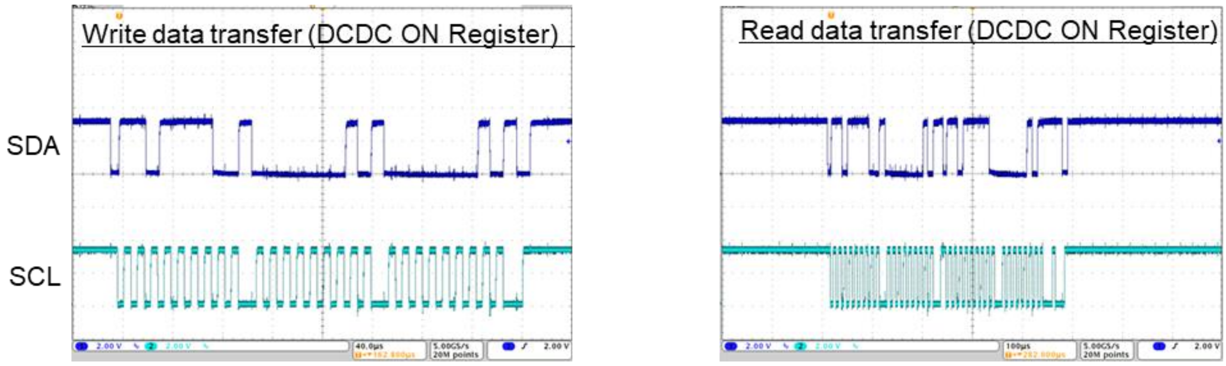


Figure 1.3 I2C reference waveform

1.4.2 I2C bus free characteristic in OFF Mode

Figure 1.4 shows the internal circuit of the SDA terminal. The drive MOS of the SDA output is an open drain configuration and bus free when the STBY Mode / ON Mode (EN = High). When OFF Mode (EN = Low), the VREG power supply disappears and the internal circuit becomes indefinite, which may affect the bus line (SDA signal becomes dull).

Note : Start I2C communication after the EN terminal becomes “High” and PG terminal becomes “Low”. If PG terminal status cannot be monitored, wait 50ms after EN terminal becomes “High”.

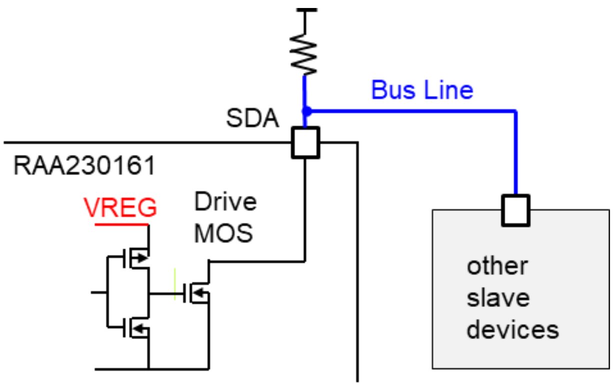


Figure 1.4 Internal circuit of the SDA terminal

2. Operation method

2.1 Start-up

Figure 2.1 shows start-up control timing by the controller. When VIN and VDD are applied, RAA230161 becomes OFF mode. When EN terminal becomes "High", the internal power supply (VREG) rises and the I2C register is reset. When I2C communication becomes available, the PG terminal output changes from “High” to “Low” and the IC becomes STBY Mode.

Note : When transiting from OFF mode to STBY mode, input “High” to the EN terminal once to initialize RAA230161GSB internal register. After that, input “Low” to the EN terminal, and re-input “High” to transit to STBY mode.

After entering STBY Mode, check the state of Protect Flag register by I2C (1). If "1" is in the Protect Flag register, RAA230161 doesn’t become ON mode (The protection operates and the DCDC output is latched off). When "1" is in the Protect Flag register, write "0" to the register and clear it. If there is no "1" in the Protect Flag register, write "1" to the WDT?S bit(D0) in the WDT SET register(0x04) and operate the watchdog timer (2). Then, if the WDT_R bit(D0) in the WDT RESET register(0x05) is not cleared within the WDT reset timing (set in the WDT SET register), the WDT stops RAA230161. When not using WDT function, write "1" to WDT_R bit.

When not using other protection functions(OVP, SCP, UVLO, OCP, OTP), write "1" to each bit in the TEST-MODE register.

After setting is completed, 5.3 V is output from VOUT by writing "1" to the DCON bit in the DCDC ON register (3). When the VOUT output stabilizes at 5.3 V, the PG signal changes from “Low” to “High”. After confirming that the PG terminal output changes to “High”, set the output voltage and the maximum output current in the DCDC ON register (4). When RAA230161 receives the voltage changing order, the PG output changes from “High” to “Low”, and the IC starts to change the output voltage to the set voltage. When the set voltage stabilizes, the PG changes from “Low” to “High”, and the master can detect VOUT change by monitoring the PG terminal.

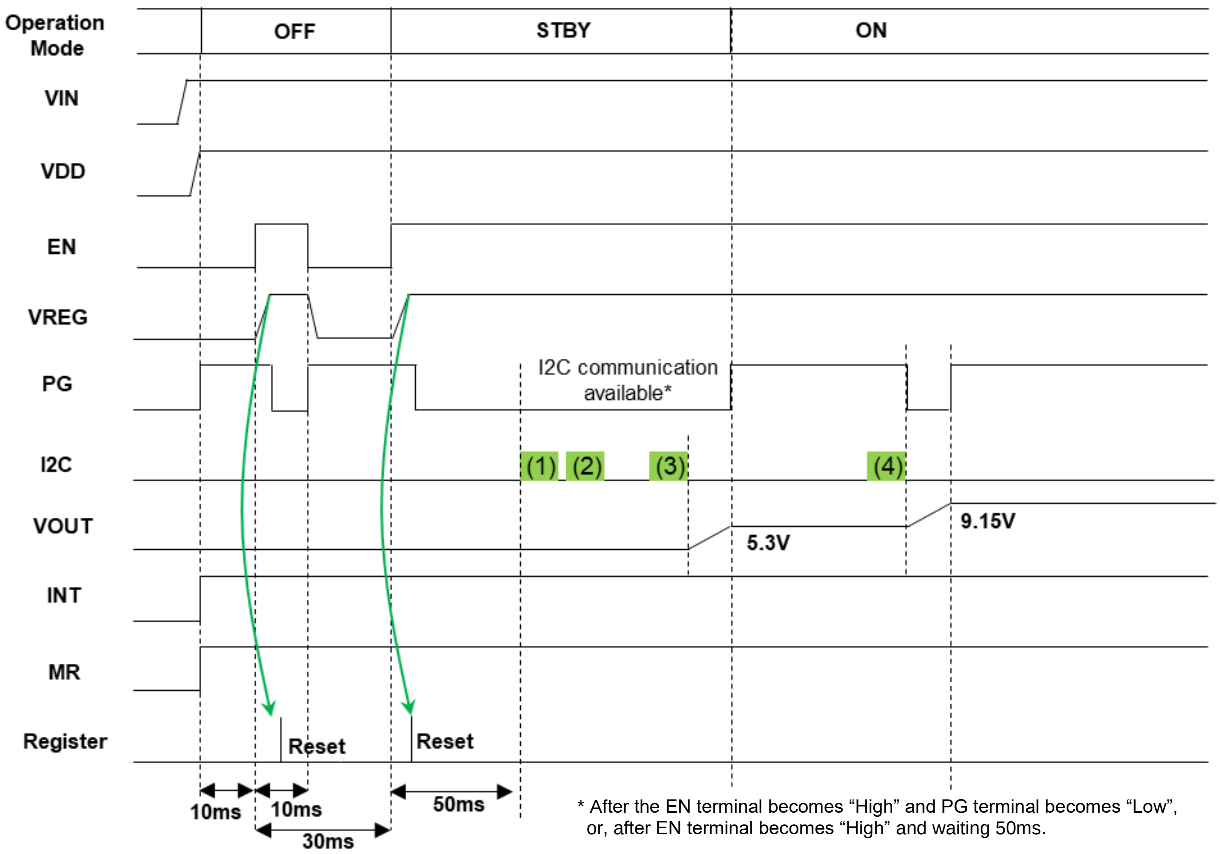


Figure 2.1 Start-up Timing

2.2 Stop 1(ON Mode to STBY Mode)

Figure 2.2 shows the transition timing from ON Mode to STBY Mode. By writing "0" to the DCON bit in the DCDC ON register at ON mode, VOUT stops and is discharged through the built-in discharge circuit (1). The discharge circuit operates until the VOUT drops to 0.4 V(typ.). When it becomes 0.4 V(typ.) or less, the discharge stops and VOUT becomes HiZ.

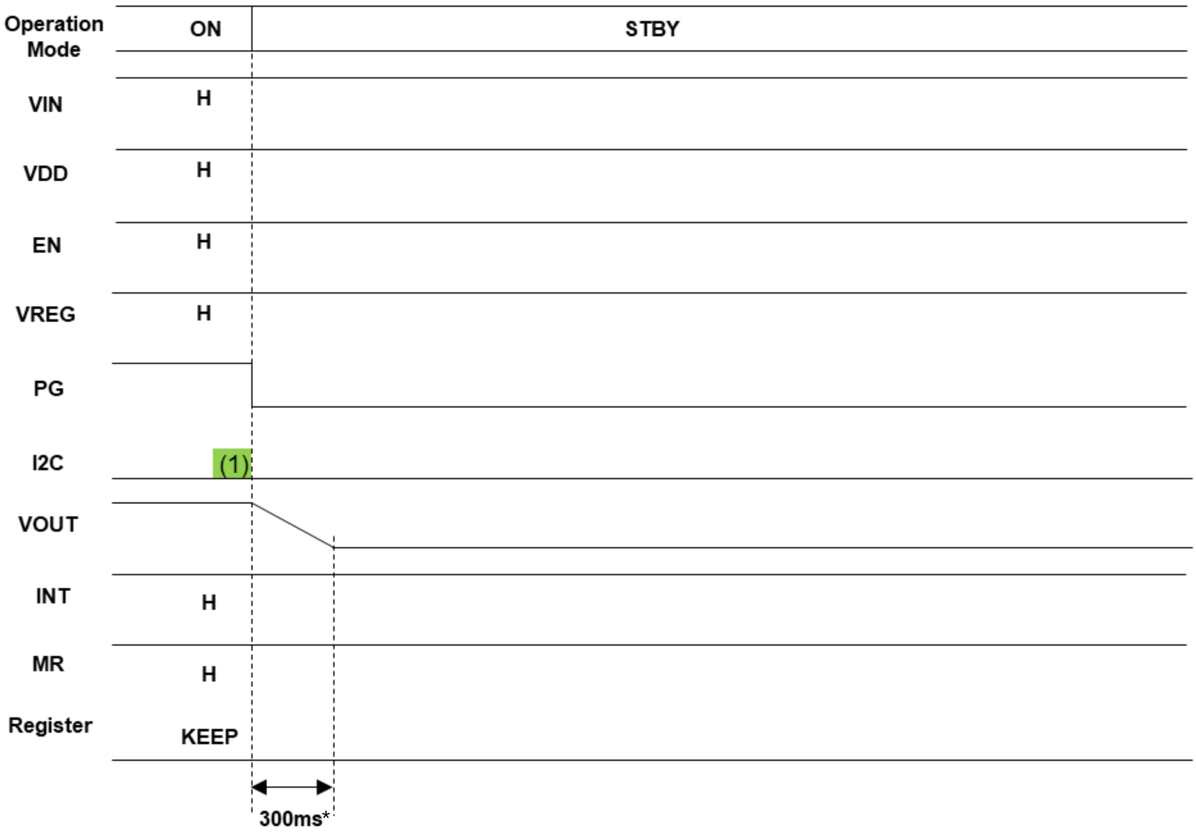


Figure 2.2 Stop Timing (ON to STBY)

*Reference value : Typical discharge time when the output capacitor effective value =44uF, VOUT drops from 20V to 0.4V

2.3 Stop 2(ON Mode to OFF Mode)

Figure 2.3 shows the transition timing from ON Mode to OFF Mode. By inputting "Low" to the EN terminal at ON mode, VOUT stops and is discharged through the built-in discharge circuit (1). The discharge circuit operates until the VOUT output voltage drops to 0.4 V(typ.). When it becomes 0.4 V(typ.) or less, the discharge stops and VOUT becomes HiZ. At this time, the VREG also stops, and the register information in RAA230161GSB is also cleared. When restarting, set the register again.

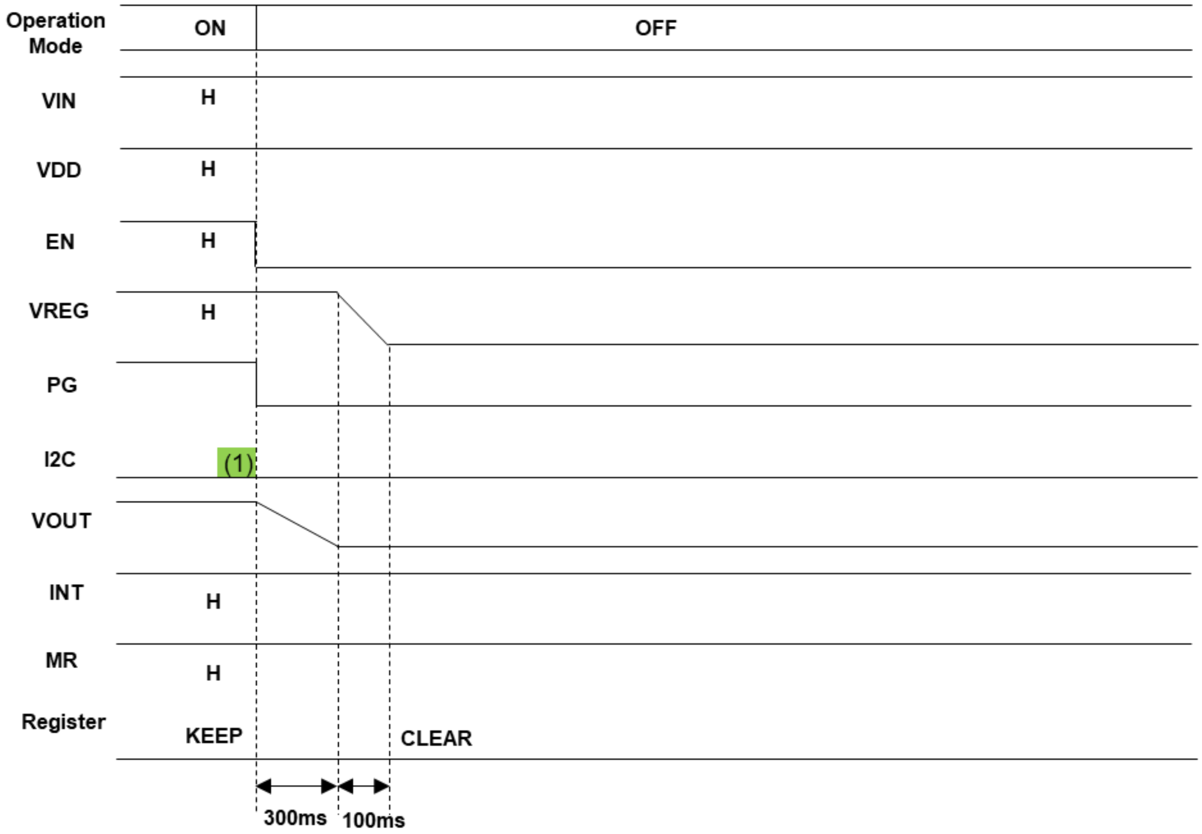


Figure 2.3 Stop Timing (ON to OFF)

2.4 Protection Function 1 (OVP, SCP, OCP, OTP)

Figure 2.4 shows the control timing by the protection circuits (OVP, SCP, OCP, OTP). When each protection circuit detects, RAA230161GSB stops VOUT output, starts discharging and transits from ON Mode to STBY Mode. At the same time, the INT terminal output changes from "High" to "Low" and clears the DCON bit in the DCDC ON register. The operating protection circuit is identified by reading the Protect Flag register(1). Then, the DCDC circuit is latched off. To restart VOUT (release the latch), write "0" to the Protect Flag register by I2C. When the latch is released, the INT terminal changes from "Low" to "High"(2). The master device can know releasing the latch by seeing the INT status. The IC becomes STBY Mode. To re-output VOUT, follow the startup sequence.

The DCON bit in the DCDC ON register is cleared, but the other bits are not cleared. Be careful when changing VOUT output voltage and maximum VOUT output current.

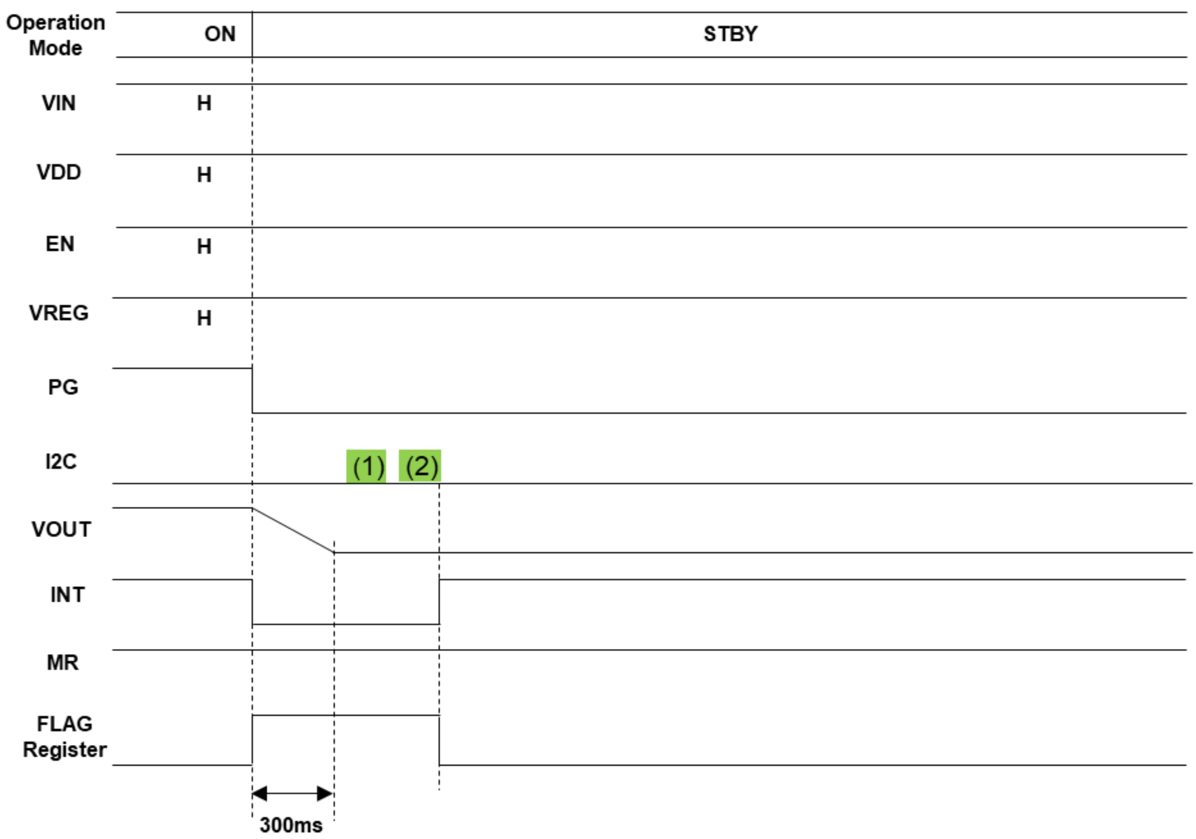


Figure 2.4 Protection function timing 1

2.5 Protection function 2 (WDT)

Figure 2.5 shows the control timing of the WDT protection. When the WDT is not reset within the reset time, the DCON bit automatically becomes “0”, the DCDC circuit stops, VOUT is discharged and RAA230161GSB transits the STBY Mode. The IC outputs a low-level one shot pulse from the MR terminal. At this time, the EN terminal doesn’t accept any signal. Reset the master device in order to return to the normal state.

After the master device restarts, the operating protection circuit is identified by reading the Protect Flag register(1). For VOUT restart, input “High” to the EN terminal and write "0" to the Protect Flag register by I2C. The latch off state is released and RAA230161GSB transits STBY Mode (2).

If the abnormal state at the master device continues, the latch off state is not released unless VIN drop off.

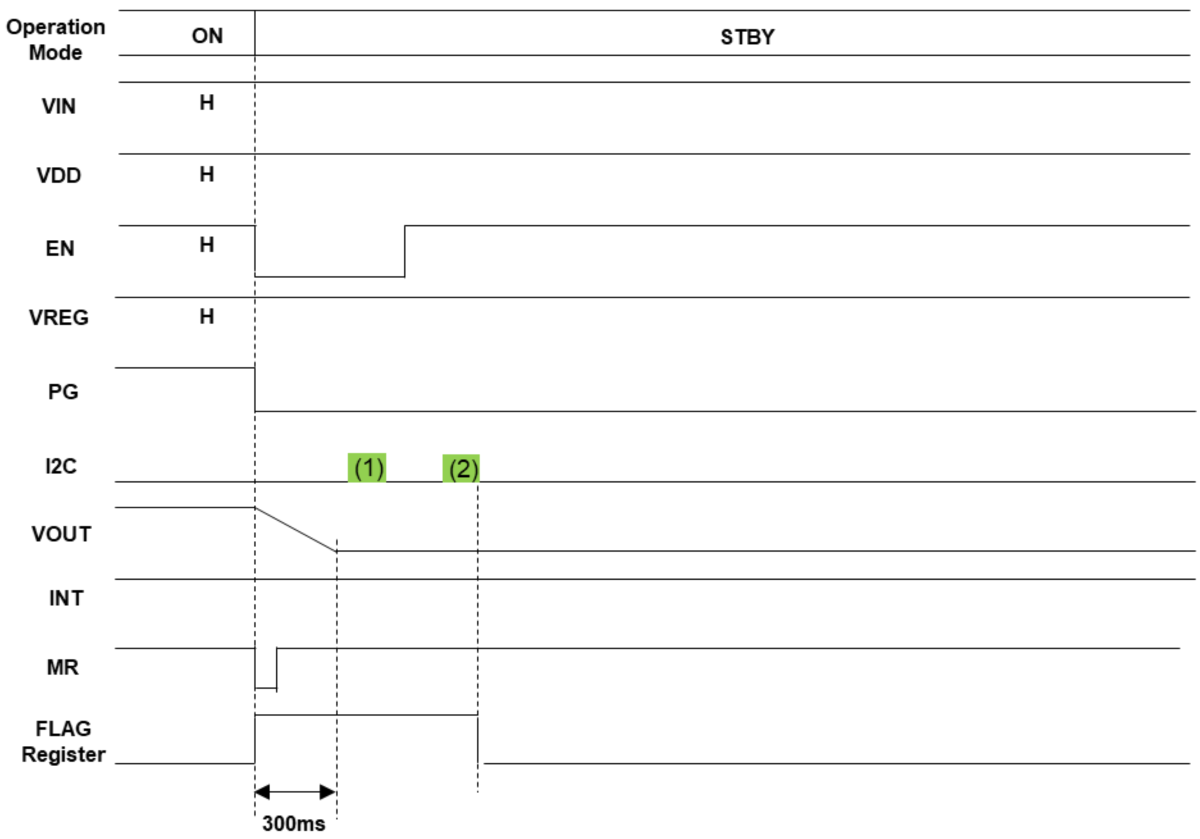


Figure 2.5 Protection function 2 (WDT detect)

3. Peripheral parts

Figure 3.1 shows the application diagram, and Table 3.1 shows the list of the external parts examples.

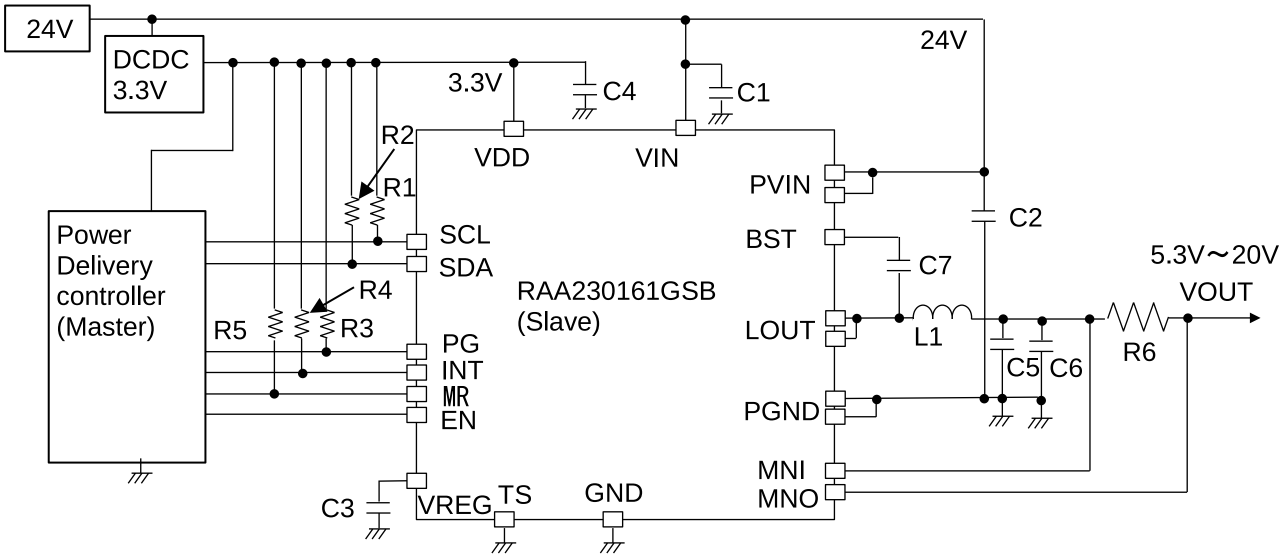


Figure 3.1 Application diagram

Table 3.1 Peripheral parts list

Part	No.	value	size	Part number	Note
Inductor	L1	6.8uH	10145	NS10145T6R8NNA	Inductor
Capacitor	C1/C2	10uF/35V	3225	GRM32ER71H106KA12L	VIN/PVIN input capacitor
	C3	1uF/25V	1608	GRM188R71E105KA12D	VREG capacitor
	C4	10uF/20V	20125	GRM21BC71E106KE11L	VDD input capacitor
	C5/C6	22uF/35V	7563	C7563X7S1H226MT	VOUT output capacitor
	C7	0.1uF/50V	1608	GRM188B11E104KA01D	Bootstrap capacitor
Resistor	R3/R4/R5	100kΩ	1608	-	EN/PG/INT/MR pull-up resistor
	R1/R2	2.2kΩ	1608	-	I2C signal pull-up resistor
	R6	50mΩ/1W	6232	ERJL1WKF50MU	Current sense resistor for OCP

3.1 Inductor

The inductor should be chosen so that the inductor ripple current (ΔIL) is within 10 to 40% of IOUT(max). When ΔIL increases, the inductor current peak raises, so the ripple of VOUT gets larger and the power loss increases. On the other hand, the large size inductor is required to lower ΔIL. ΔIL can be calculated by an equation below.

$$\Delta \mathrm{IL} = \frac{(Vin - Vout)}{L} \times \frac{Vout}{Vin} \times \frac{1}{f_{SW}}$$

fsw=0.5MHz

The inductor peak current (ILpeak) can be calculated by an equation below.

$$IL_{Peak} = I_{OUT}(MAX) + \frac{\Delta IL}{2}$$

Choose the inductor which saturation current is higher than ILpeak.

Table 3.1 Inductor example

Inductance [H]	Part number	Manufacture	DC Resistance [Ω]	I_{TEMP} [A]	I_{SAT} [A]	Size (L×W×T) [mm]
4.7u	NS10145T4R7NNA	TAIYO YUDEN	17.3m	5.03	6.69	10.1×10.1×4.85
6.8u	NS10145T6R8NNA	TAIYO YUDEN	24m	4.22	5.05	10.1×10.1×4.5
10u	NS10155T100MNA	TAIYO YUDEN	24m	4.4	4.49	10.1×10.1×5.5

Note ITEMP : Rated current by temperature rising

ISAT : Rated current by inductance loss

These inductors are examples. About inductor detail, contact each manufacturer

3.2 Input capacitor

Connect the input capacitor between VIN pin and GND pin, PVIN pin and GND pin. Use over 10uF. Put the capacitor as close as possible to the pins. Low ESR (equivalent series resistance) capacitor like a ceramic capacitor is recommended to reduce the input ripple voltage. Capacitance of a ceramic capacitor decreases in actual use because of DC bias effect, so choose a ceramic capacitor which capacitance maintains over 10uF in the application operation condition.

3.3 Output capacitor

RAA230161GSB has phase compensation circuit which is optimized to DC/DC operation. In order to operate stably with the phase compensation, choose the output capacitor over 22uF. Low ESR capacitor like a ceramic capacitor is recommended to reduce the output ripple voltage. Capacitance of a ceramic capacitor decreases in actual use because of DC bias effect, so choose a ceramic capacitor which capacitance maintains over 22uF in the application operation condition. To reduce the mounting area, it is possible to use multiple small capacitance capacitors in parallel.

3.4 Current sense resistor

The over current protection circuit (OCP) in RAA230161GSB uses the current sense resistor between MNI pin and MNO pin. Use 50mΩ(typ). Recommended power rating of the resistor is 1W.

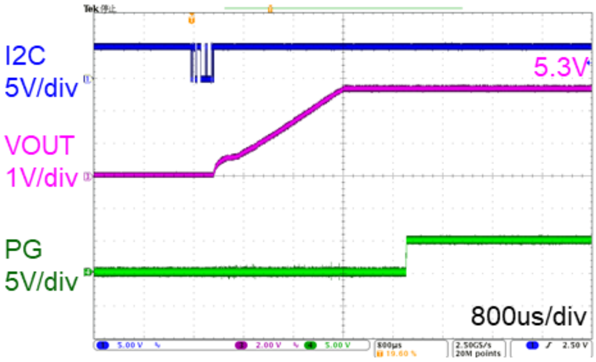
4. Reference data

Reference waveforms on Renesas RAA2230161GGSB evaluation board.

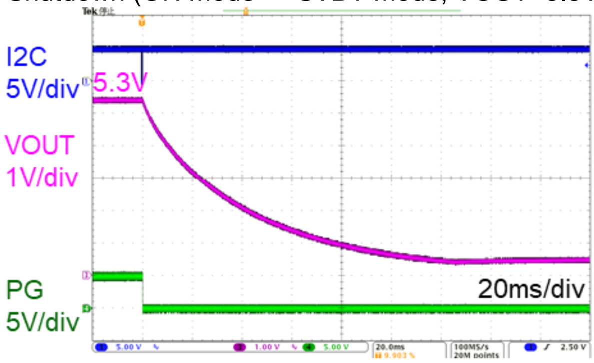
Condition : VIN = PVIN = 24V, VDD=3.3V, No load, TA = 25˚C   Using the parts on the page 16

4.1 Start-up / Shutdown Waveforms

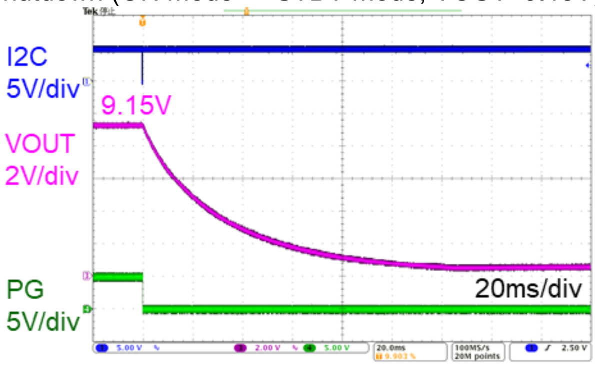
Start-up (STBY mode → ON mode)



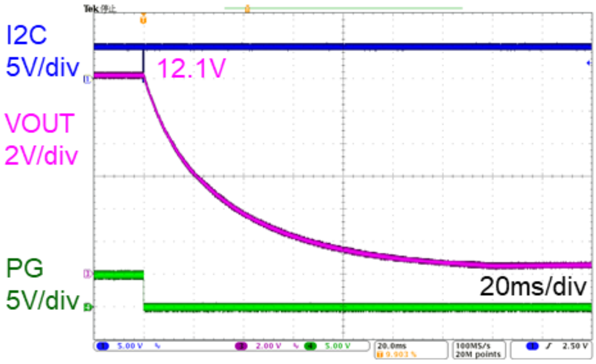
Shutdown (ON mode → STBY mode, VOUT=5.3V)



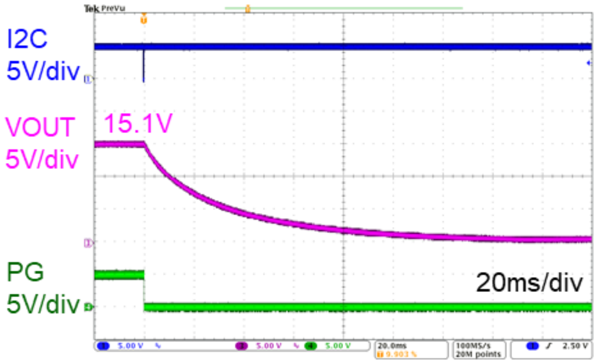
Shutdown (ON mode → STBY mode, VOUT=9.15V)



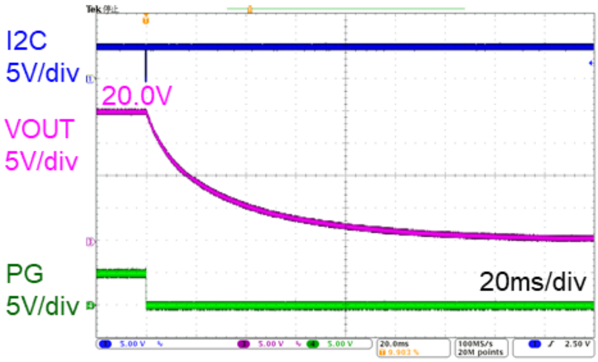
Shutdown (ON mode → STBY mode, VOUT=12.1V)



Shutdown (ON mode → STBY mode, VOUT=15.1V)

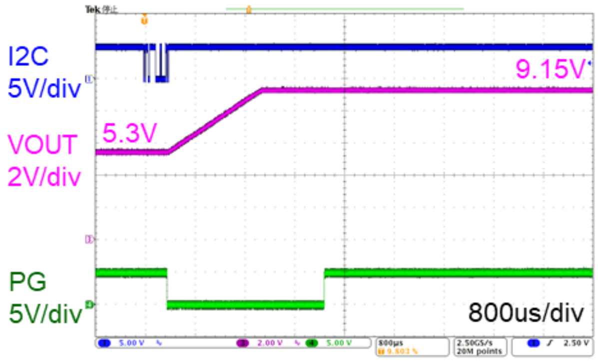


Shutdown (ON mode → STBY mode, VOUT=20V)

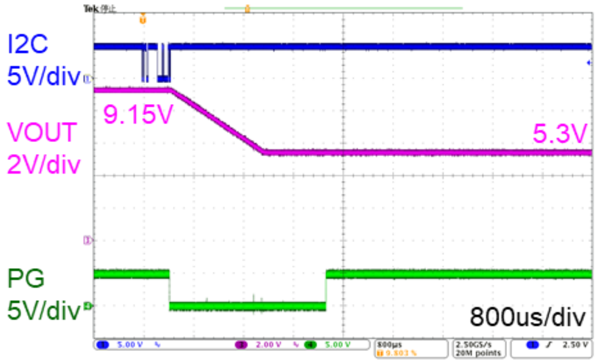


4.2 Output Voltage Changing Waveforms

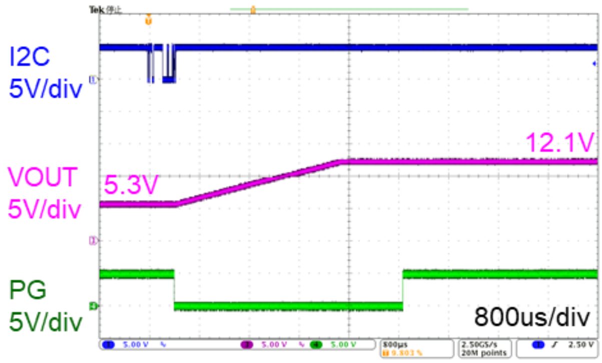
VOUT : 5.3V to 9.15V



9.15V to 5.3V



VOUT : 5.3V to 12.1V



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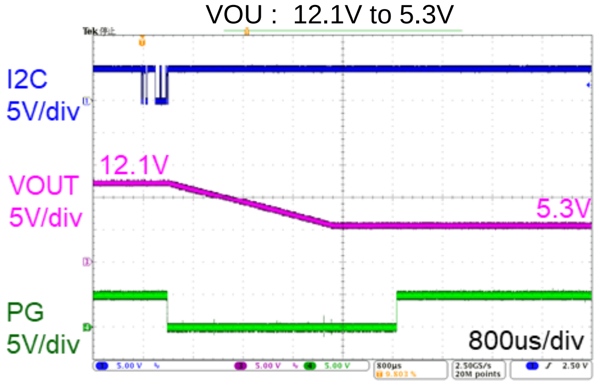

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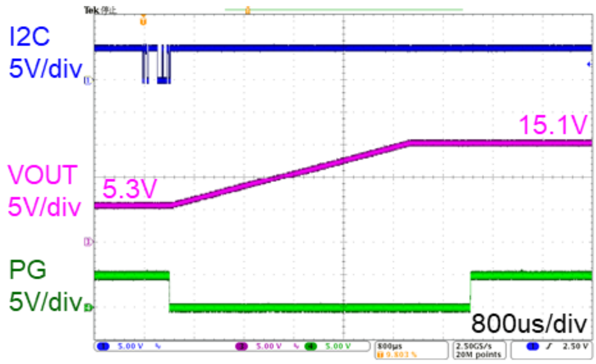

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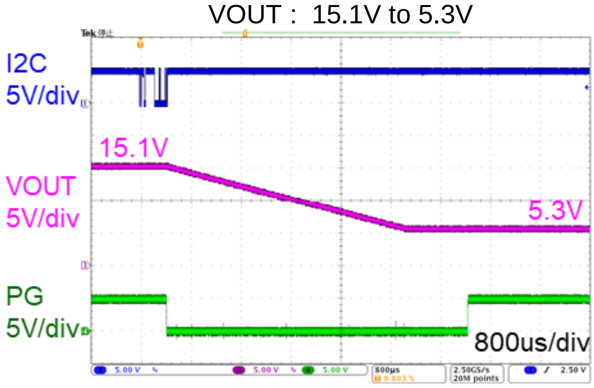

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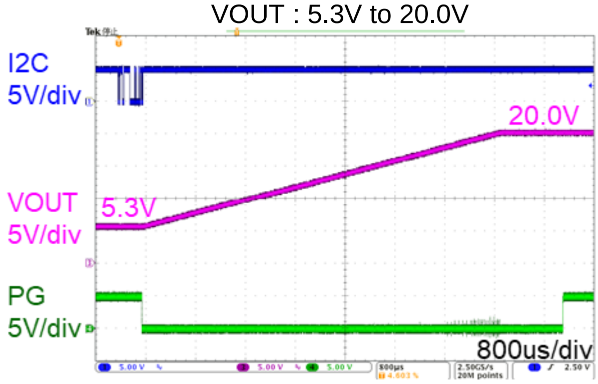
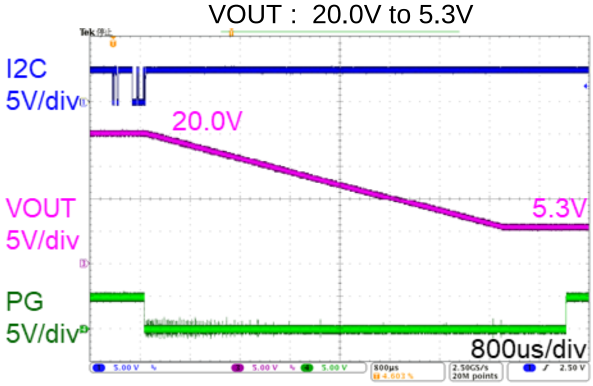


VOUT : 20.0V to 5.3V



Website and Support

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http://www.renesas.com/

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May 15,2018	-	First Edition issued.

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