

RAA271005: The Design of the Power-Supply Circuit for the R-Car S4

This document gives guidelines for designing power-supply circuits for the R-Car S4 products by using the RAA271005 Power-Supply IC to implement standard control operations such as the sequences of turning the power on and off.

Also, additional details on the power sequence for the R-Car S4 is referred to in the *R-Car S4 Hardware User's Manual* and *Power Sequence Guide*.

Target Device

- RAA271005

Target SoCs

- R-Car S4-8, R-Car S4-4, R-Car S4N-8, R-Car S4N-4

Note: The R-Car series products listed above are hereinafter collectively referred to as "SoC".

Reference Document

- *RAA271005 Datasheet*
- *RAA271005 Safety Application Note (SAN)*
- *RAA271041 Datasheet*
- *R19UH0161EJ0100, R-Car S4 Series User's Manual: Hardware*
- *R01AN7078EJ0100, R-Car S4 Power Sequence Guide*

Note: References are for the latest published version, unless otherwise indicated.

Contents

1. Overview	2
1.1 Block Diagram of a System Using SoC	2
1.2 I/O Configuration	4
1.2.1 Protection GPIO	5
1.2.2 ADC3-5 Inputs	6
2. RAA271005 Power On/Off Requirements	7
2.1 Power-On Requirements	7
2.2 Power Off Requirements	9
3. RAA271005 PIN Connection	10
3.1 Connection of Buck1 Remote Sense Pins with SoC	10
3.2 Recommended Handling of Unused Pins	10
3.2.1 GPIO Pins (IO3-5)	10
3.2.2 IRQ# Pin(IO14)	10
3.2.3 ADC Pins	10
3.2.4 LDO Power Output Pins	11
3.2.5 GC Pin	11
4. Revision History	11

1. Overview

1.1 Block Diagram of a System Using SoC

The RAA271005 contains five DC/DC switching regulators and six low-drop out linear regulators (LDO). These outputs are controlled by EN and PWR_CTL1(PWRCTL_MCUPLL), PWR_CTL2(PWRCTL_SOCISO) from the SoC. Figure 1 shows an example of connection with the SoC and the RAA271041 as the primary power supply.

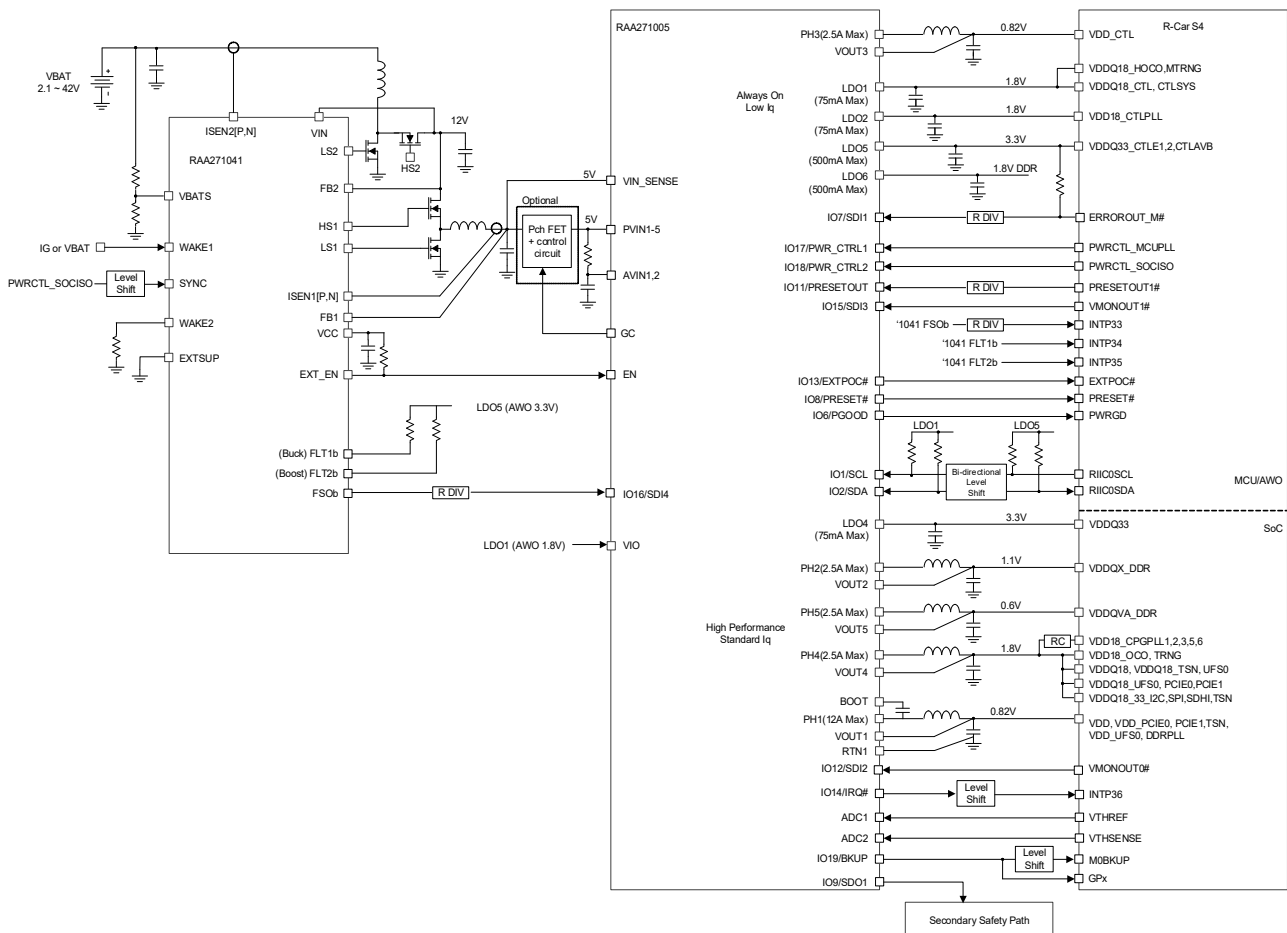


Figure 1. Block Diagram of a System Using SoC and RAA271041 (Example)

Table 1 shows an example of the Allocation of Power Supplies between the SoC and the RAA271005.

Table 1. The Allocation of Power Supplies between the SoC and the RAA271005 (Example)

Buck/LDO Output Name	Buck/LDO Output Voltage ^[1]	Power Group	SoC Pin Name	Other Connection
VOUT1	0.82V	PWRCTL2	VDD, VDD_PCIE0, PCIE1, TSN, VDD_UFS0, DDRPLL	-
VOUT2	1.1V	PWRCTL2	VDDQX_DDR	LPDDR4X
VOUT3	0.82V	AWO	VDD_CTL	-
VOUT4	1.8V	PWRCTL2	VDD18_CPGPLL1,2,3,5,6 VDD18_OCO, TRNG VDDQ18, VDDQ18_TSN, UFS0 VDDQ18_UFS0, PCIE0, PCIE1 VDDQ18_33_I2C, SPI, SDHI, TSN	NOR Flash, eMMC
VOUT5	0.6V	PWRCTL2	VDDQVA_DDR	LPDDR4X
LDO1	1.8V	AWO	VDDQ18_HOCO, MTRNG VDDQ18_CTL, CTLSYS	-
LDO2	1.8V	PWRCTL1	VDD18_CTLPLL	-
LDO3	-	-	-	-
LDO4	3.3V	PWRCTL2	VDDQ33	eMMC
LDO5	3.3V	AWO	VDDQ33_CTLE1,2, CTLAVB	-
LDO6	1.8V	PWRCTL2	-	LPDDR4X

1. The Buck/LDO output voltages do not take into voltage drop on a wiring of PCB from ball of RAA271005 or inductor to ball of SoC. These voltage drops should be considered by system.

1.2 I/O Configuration

The I/O supply voltage in RAA271005 is set by VIO, and the typical VIO voltage is 1.8V or 3.3V. Some I/O pins (IO6 to IO19) require a level shifter to align with the voltage of the SoC I/O pins.

Table 2. I/O Connections

RAA271005		SoC		Level Shifter ^[1]	
IO Number	Pin Name	Pin Name	Power Domain	VIO = 1.8V	VIO = 3.3V
IO6	PGOOD	PWRGD	VDDQ18_CTLSYS		X
IO7	SDI1	ERROROUT_#M	VDDQ33_CTLE2	X	
IO8	PRESET#	PRESET#	VDDQ18_CTLSYS		X
IO9	SDO1	-	-	Depends on system	
IO10	SDO2	-	-		
IO11	PRESETOUT	PRESETOUT0	VDDQ33	X	
IO12	SDI2	VMONOUT0	VDDQ18		X
IO13	EXTPOC#	EXTPOC#0	VDDQ18_CTLSYS		X
IO14	IRQ#	INTP36	VDDQ33_CTLE1	X	
IO15	SDI3	VMONOUT1	VDDQ18_CTLSYS		X
IO16	SDI4	-	-	Depends on system	
IO17	PWR_CTL1	PWRCTL_MCUPLL	VDDQ18_CTLSYS		X
IO18	PWR_CTL2	PWRCTL_SOCISO	VDDQ18_CTLSYS		X
IO19	BKUP	M0BKUP	VDDQVA_DDR	X	X

1. The X symbol indicates that a level shifter is required.

1.2.1 Protection GPIO

The GPIOs (IO7-IO12, 15, 16) are implemented in the Protection block. The OTP setting in Protection GPIOs (except PRESET) are initialized to default at Deep Stop mode, and the GPIOs in Protection (except PRESET) set the input and the no internal PU/PD resistor setting.

External pull-up or pull-down resistors are required to avoid floating on output pins in Deep Stop and Suspend-to-RAM modes (if applicable) and to ensure the VIO current consumption is within target.

Table 3. Regulation and Protection GPIO

Location	Pin Name	Pin Mode: 0x0	Pin Mode: 0x1
Regulation	IO1	SCK	SCL
	IO2	SS_B2	SDA
	IO3	SS_B	GPIO
	IO4	MOSI	GPIO
	IO5	MISO	GPIO
	IO6	PGOOD	PGOOD
Protection	IO7	SDI1	SDI1
	IO8	PRESET#	PRESET#
	IO9	SDO1	SDO1
	IO10	SDO2	SDO2
	IO11	PRESETOUT	PRESETOUT
	IO12	SDI2	SDI2
Regulation	IO13	EXTPOC#	EXTPOC#
	IO14	IRQ#	IRQ#
Protection	IO15	SDI3	SDI3
	IO16	SDI4	SDI4
Regulation	IO17	PWR_CTRL1	PWR_CTRL1
	IO18	PWR_CTRL2	PWR_CTRL2
	IO19	BKUP	BKUP

1.2.2 ADC3-5 Inputs

The RAA271005 uses a sophisticated multi-channel 12-bit SAR ADC to continuously monitor all output rails.

The monitoring system also measures up to 16 external signals by using 5 dedicated ADC pins. These ADC pins can be configured either as all analog inputs (ADC1-5), or ADC3-5 can be configured as an output that uses external multiplexers.

Protection register 0x135 - ADCMON_EXT_CFG can be used to configure the external mux options. Refer to section 6 in the *RAA271005 Datasheet* for more detail on ADC monitoring.

ADC3-5 are forced to become outputs, and the outputs are low during the CVM test in SoC activation regardless of ADCMON_EXT_CFG. Refer to section 7 in the *RAA271005 SAN* for more detail on the CVM test or SoC activation. If any output on external devices connects with ADC3-5 and no external mux option, the output of the external device conflicts to the output of ADC3-5 during CVM test.

Do not connect with an output of external devices to ADC3-5 without a resistor. The resistor value should be set by the system.

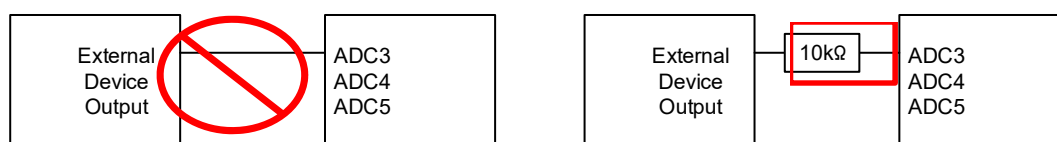


Figure 2. ADC3-5 Connection with External Devices

2. RAA271005 Power On/Off Requirements

2.1 Power-On Requirements

The RAA271005 has requirements for the power-on sequence:

- To set On delay and slew rate of each Buck and LDO so that the internal PGOOD goes High after a protection BIST(T_{BIST}). The protection BIST starts with EN at cold start or with PWR_CTL2 at warm start (see [Figure 3](#) and [Figure 4](#)).
- To set 1ms delay (IO_GPIO_2_DATAOUT_UP_DLY) in PGOOD to be high after the ADC detection results stabilize. (IIR = 1/16 case)
- To set On delay and slew rate of each Buck and LDO to complete the power-up of all Buck and LDO within 64ms of P/U timer (TIMEOUT_PUSEQ_ST).
- Refer to the *Sequence of Turning On/Off Power Supplies in R-Car S4 Series User's Manual*.
- Refer to the power-up/down sequence in the *LPDDR4X Datasheet*.

Note: The slew rate of each Buck and LDO should be set appropriately to prevent overcurrent detection because of an inrush current at power-up.

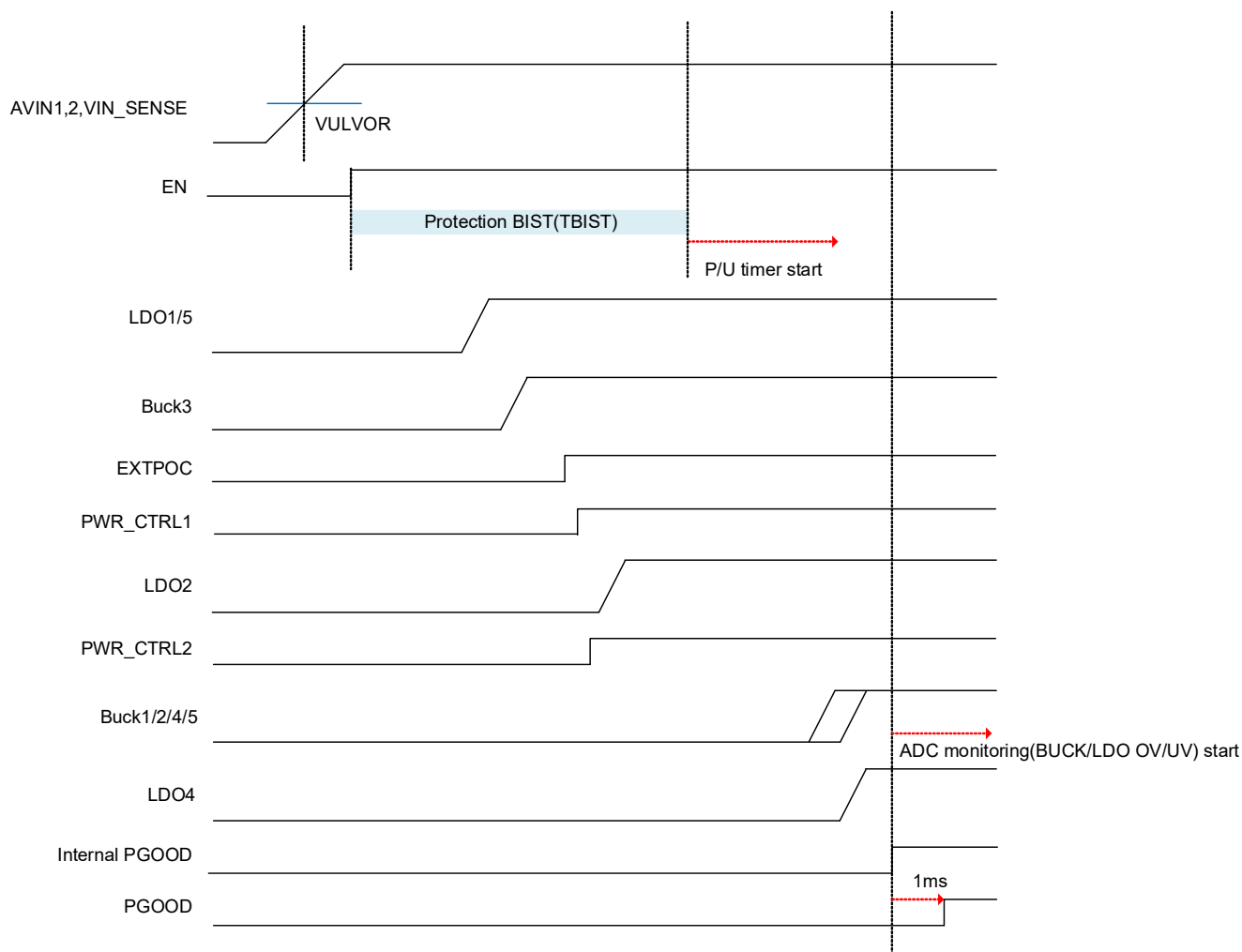


Figure 3. Power Off to Full Run (Cold Start)

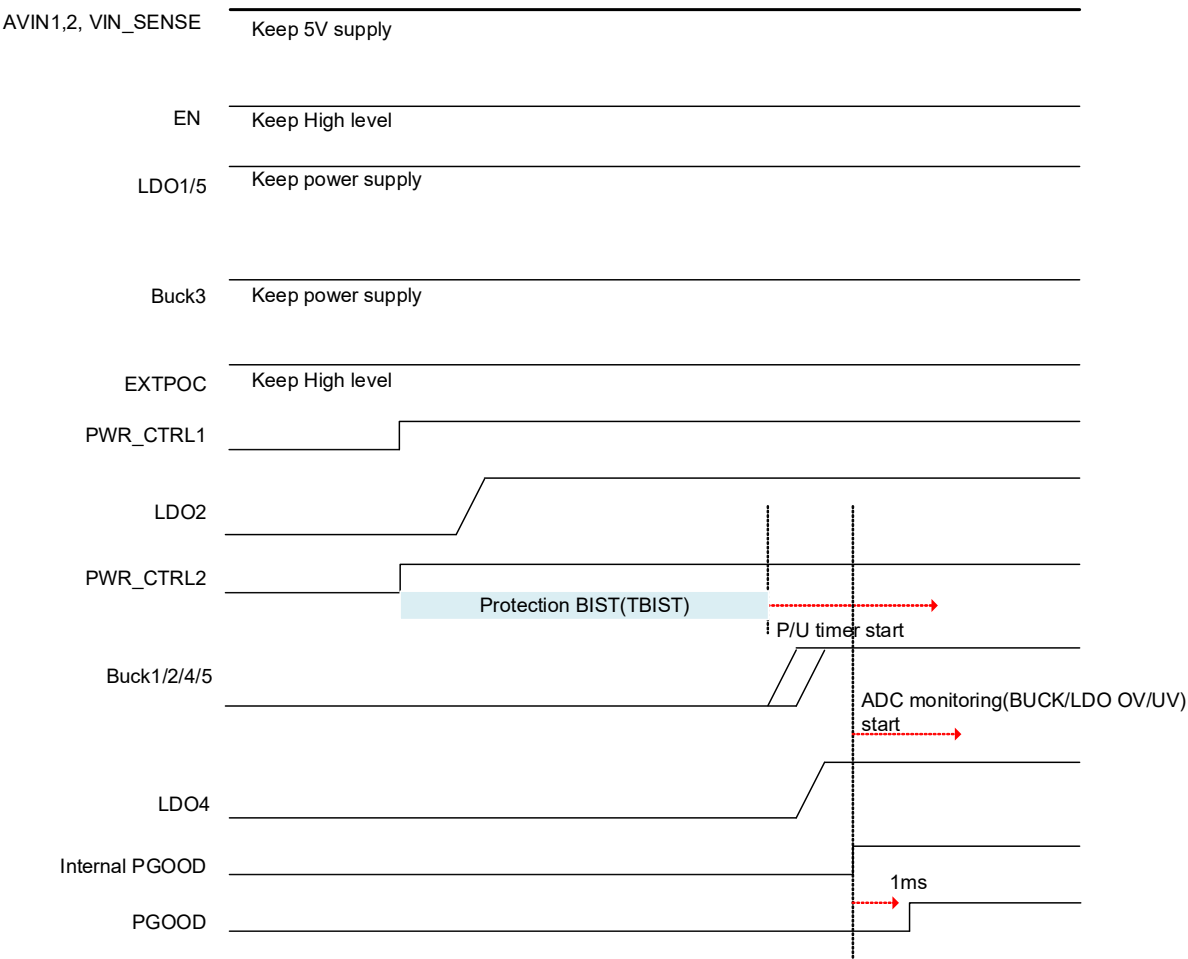


Figure 4. DeepStop to Full Run (Warm Start)

2.2 Power Off Requirements

The SoC requires that all power supplies are discharged below 0.2V at power off before restarting the rails. In RAA271005, set the discharge level (BUCKx_DISC_VTH/LDOx_DISC_VTH) to 150mV to ensure that the voltages are below 0.2V.

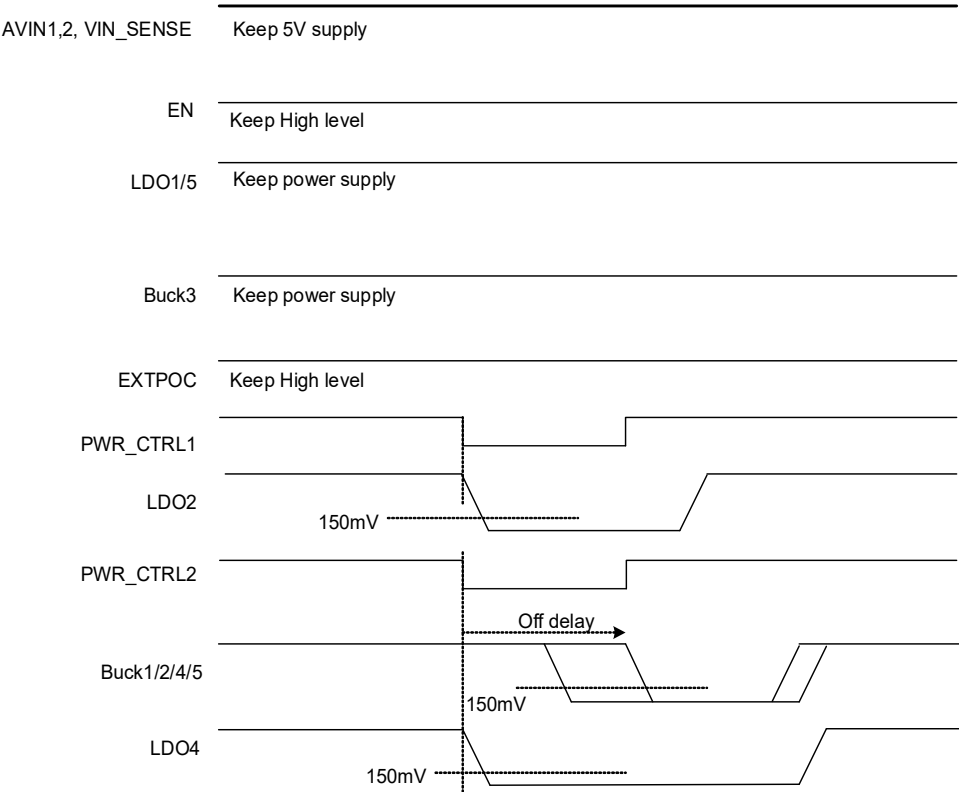


Figure 5. Discharge Behavior at Power Off

3. RAA271005 PIN Connection

3.1 Connection of Buck1 Remote Sense Pins with SoC

When Buck1 is used for the core voltage of SoC, the Buck1 remote sense pins VOUT1 and RTN1 should connect as follows.

Connect the VOUT1 and RTN1 to SoC's VDD and VSS, respectively, and locate them around the center of the chip.

Important: Limit the PCB wiring resistance between VOUT1 and VDD (R_{pcb}) to less than 0.6Ω .

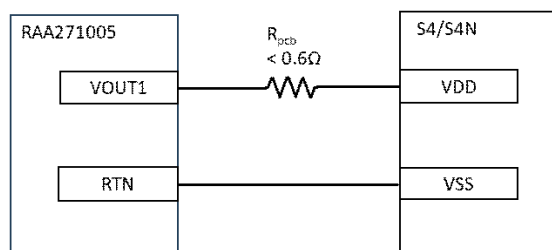


Figure 6. Connection of Buck1 Remote Sense Pins

3.2 Recommended Handling of Unused Pins

The following sections and tables describe the recommended handling of unused pins.

3.2.1 GPIO Pins (IO3-5)

The IO3-5 pins can be configured as GPIO (General-purpose I/O).

The recommended unused GPIO pin connection is different according to the GPIO direction setting.

Table 4. Handling of Unused GPIO Pins

Pin Name	GPIO Direction	Recommended Handling of Unused Pin
GPIOx (x:1-3)	Input	Connect to ground
	Output	Open

3.2.2 IRQ# Pin(IO14)

Table 5. Handling of Unused IRQ# Pin

Pin Name	Pin Type	Recommended Handling of Unused Pin
IRQ#	Output	Open

3.2.3 ADC Pins

Table 6. Handling of Unused ADC Pins^[1]

Pin Name	Pin Type	Recommended Handling of Unused Pin
ADCx (x:1-5)	Input	Connect to ground

1. ADC3-5 can be configured to digital output to control external multiplexer.

3.2.4 LDO Power Output Pins

The LDO configuration needs to set disable by OTP when it is unused.

Table 7. Handling of Unused LDO Power Output Pins

Pin Name	Pin Type	Recommended Handling of Unused Pin
LDOOx (x:1-6)	Output	Open

3.2.5 GC Pin

Table 8. Handling of Unused GC Pin

Pin Name	Pin Type	Recommended Handling of Unused Pin
GC	Output	Open

4. Revision History

Revision	Date	Description
1.03	Aug 26, 2026	Updated Figure 1.
1.02	Nov 7, 2025	Updated Figure 1.
1.01	Nov 25, 2024	Updated Table 1. Updated Power-On Requirements.
1.00	Oct 2, 2024	Initial release

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Disclaimer Rev.5.0-1)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/