RAA271005 OTP Creator Guide

R-Car Series, 4th Generation

This application note serves as a comprehensive guide for using the OTP (One-Time Programmable) Creator with the RAA271005 PMIC, a device for the 4th generation R-Car System-on-Chips (SoCs) by Renesas. This guide is crafted to assist developers, engineers, and enthusiasts in harnessing the full potential of the RAA271005 PMIC, enabling seamless integration and optimal performance within automotive applications powered by the advanced 4th generation R-Car platforms. By leveraging the unique features and customization options offered by the OTP functionality, this guide aims to empower users to configure the PMIC settings precisely to application requirements ensuring efficiency, reliability, and flexibility.

Target SoCs

Note: In this document, the following R-Car series products are collectively referred to as SoCs.

- R-Car S4
- R-Car V4H
- R-Car V4M

Target Power-Supply ICs

- RAA271005 – PMIC for 4th Generation R-Car SoCs

Contents

1. OTP Creator Guide

The RAA271005 OTP Creator allows the user to view and select OTP settings designed for their specific platform. This guide reviews each group of selectable options with an explanation of the feature.

The OTP Creator is separated by four tabs, the **Instructions**, **Approval**, **Regulation**, and **Protection** tabs (see Figure 1).

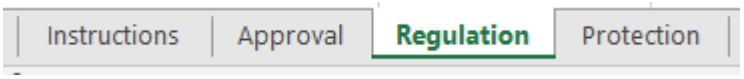


Figure 1. RAA271005 OTP Creator – Tabs

1.1 Instructions Tab

The **Instructions** tab provides a quick guide for using the OTP creator with a timing diagram of a startup and shutdown delay. Review the **Instructions** tab before selecting OTP settings. Also, this guide provides more detail for each group of selectable options. The following are useful instructions:

- Only yellow cells are allowed to be modified.
- If the cell has a dropdown menu, only use the selectable option in the dropdown menu.
- Do not copy and paste cells as that could change the formula in the cell.
- Cells that are highlighted red could mean an issue with the selected setup. Review the highlighted red cells with a representative from Renesas.

1.2 Approval Tab

After each party agrees on the OTP setting, the **Approval** tab is used to sign off and finalize the settings. An OTP version ID is provided by Renesas to be used for sample requests. If additional changes to the OTP settings are required, a new OTP version ID is assigned, and the approval process is repeated. Figure 2 charts the process for OTP selection, approval, and verification.

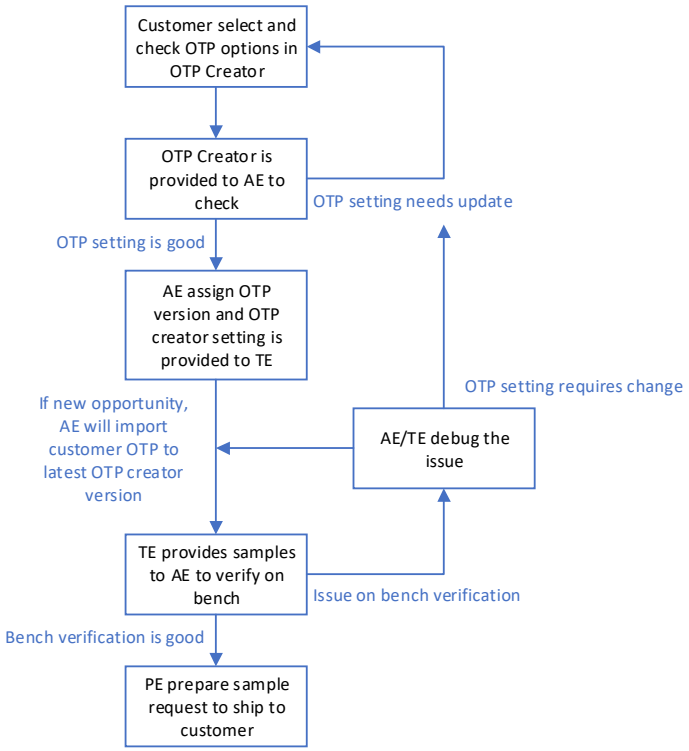


Figure 2. RAA271005 OTP Creator – Flow Chart

1.3 Regulation Tab

In the **Regulation** tab, the user can select required output voltages, sequencing, fault reactions, IO pin settings, pin mode, and others.

1.3.1 Target Application (SoC)

Depending on the application, the OTP setting of each regulator can differ. Select the appropriate application on cell E3. The following are selectable options:

- S4 – When S4 is selected, Buck3 is configured in PFM.
- V4H – When VH4 is selected, all rails are in CCM and no power grouping is required.
- V4M – When V4M is selected, all rails are in CCM and no power grouping is required.
- Generic – When generic is selected, no additional setting is applied to the regulators.

1.3.2 Output Voltage Selection

Each regulator has a settable voltage range. If the regulator is not used, set the voltage value to 0 and set the regulator's "Startup with EN?" to False in column Q.

Table 1. Output Voltage Range

Regulator	Voltage Range	Additional Note
Buck1	0.3V – 3.3V	
Buck2	0.3V – 3.3V	
Buck3	0.5V – 3.3V	
Buck4	0.5V – 3.3V	
Buck5	0.5V – 3.3V	
LDO1	1.8V – 3.3V	UV monitoring only available for 1.8V and 3.3V
LDO2	1.8V – 3.3V	UV monitoring only available for 1.8V and 3.3V
LDO3	1.8V – 3.3V	UV monitoring only available for 1.8V and 3.3V
LDO4	1.8V – 3.3V	UV monitoring only available for 1.8V and 3.3V
LDO5	0.6V – 3.3V	
LDO6	0.6V – 3.3V	

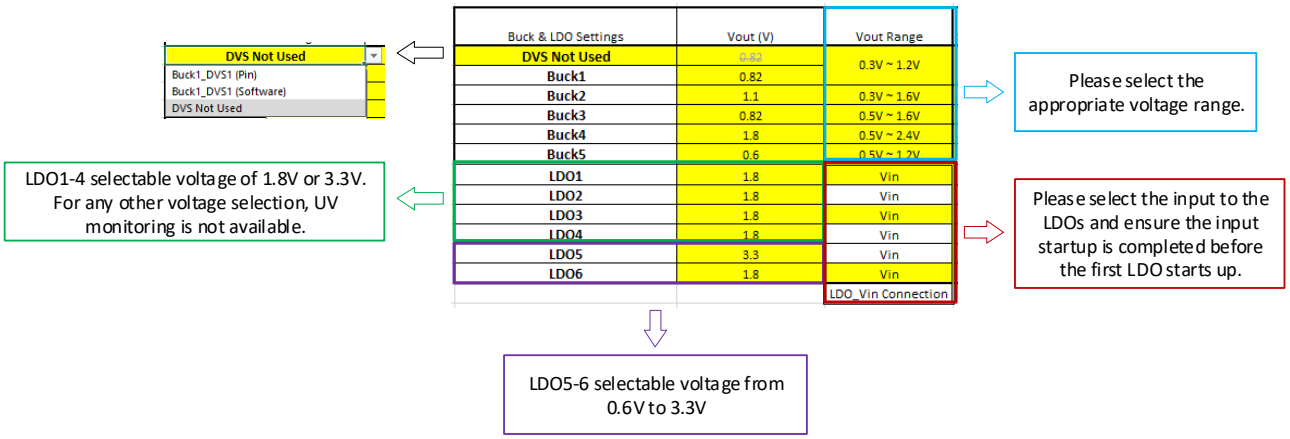


Figure 3. Output Voltage Selection

The VIO voltage must be selected based on the schematic. *Note:* If a PMIC regulator is used for VIO voltage, the selected regulator must be in the Always ON power state. Figure 4 shows the VIO voltage selection.

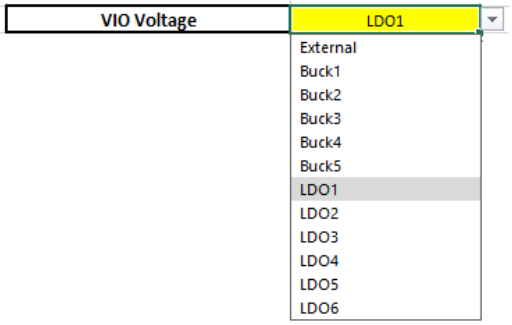


Figure 4. VIO Voltage

1.3.3 Timing Sequence and Power State

For each of the regulator output, the startup delay and shutdown delay are programmable. Each regulator can be set to a different power state (Always ON, PWRCTRL1, PWRCTRL2, and SW Shutdown Group. *Note:* The Always ON group does not have selection for Suspend to RAM as it is always enabled.

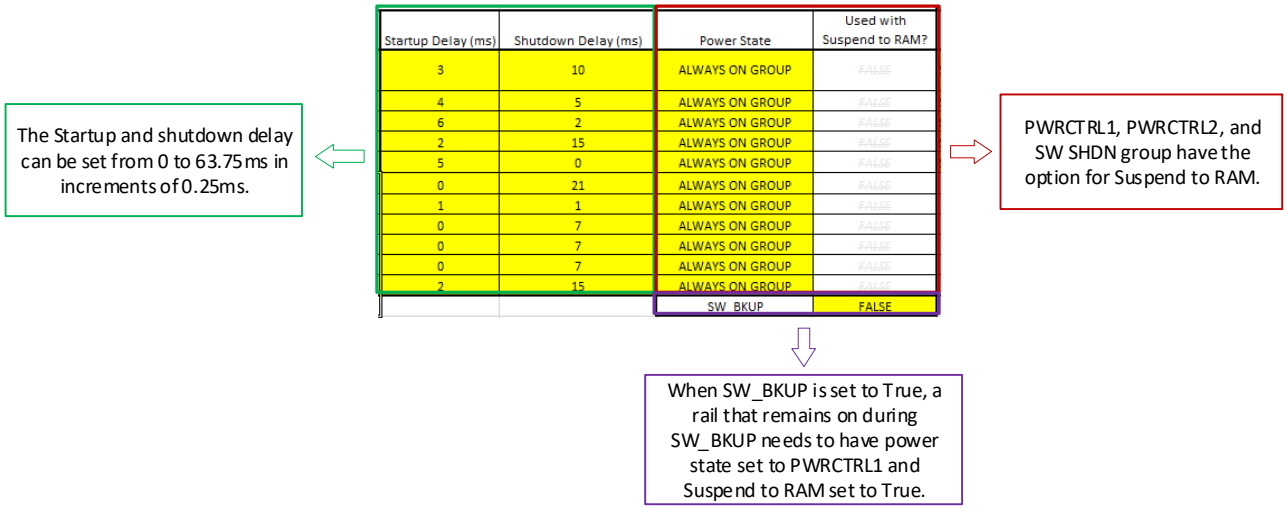
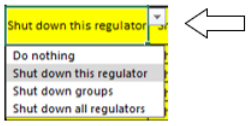


Figure 5. Sequence and Power State Selection

1.3.4 Fault Reactions

For fault reactions, the PMIC has the option to configure a reaction by overvoltage, undervoltage, high-side positive current limit, low-side positive current limit, negative current limit, and regulation thermal shutdown. See Figure 6 for the dropdown menu options.



Fault Reactions					
Over Voltage	Under Voltage	High-Side Pos Current Limit	Low-Side Pos Current limit	Negative Current Limit	Regulation Thermal Shutdown Reaction
Shut down this regulator	Shut down this regulator	Shut down this regulator	Do nothing	Shut down this regulator	Shut down this regulator
Shut down this regulator	Shut down this regulator	Shut down this regulator	Do nothing	Shut down this regulator	Shut down this regulator
Shut down this regulator	Shut down this regulator	Shut down this regulator	Do nothing	Shut down this regulator	Shut down this regulator
Shut down this regulator	Shut down this regulator	Shut down this regulator	Do nothing	Shut down this regulator	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
N/A	Shut down this regulator	N/A	N/A	N/A	Shut down this regulator
The overall fault reaction might be different based on protection block interactions					

Figure 6. Fault Reaction Selection

Note: The Low-Side Positive Current Limit for Buck1 is not available and is set to Do Nothing.

1.3.5 Pin mode and IO Pin Settings

The RAA271005 has two pin mode options, Pinmode 0 and Pinmode 1:

- In Pinmode 0, SPI communication is used which forces set IO3, IO4, and IO5 to SS_B, MOSI, and MISO, respectively. These three IO pins cannot be used as generic GPIO in this mode. See Figure 7.
- In Pinmode 1, I^{2}C communication is used allowing IO3, IO4, and IO5 to be used as generic GPIO. See Figure 8.

IO Pin Settings							
	IO3	IO4	IO5	IO6	IO13	IO14	IO19
Direction	~~Input~~	~~Input~~	~~Input~~	Output	Output	Output	Output
Invert?	~~FALSE~~	~~FALSE~~	~~FALSE~~	FALSE	FALSE	TRUE	FALSE
Output Open Drain?	~~FALSE~~	~~FALSE~~	~~FALSE~~	FALSE	FALSE	FALSE	FALSE
Function*	SS_B	MOSI	MISO	PGOOD_GLB	PGOOD_ALWON	Global Interrupt	BKUP signal
Assert Delay (ms)	~~N/A~~	~~0~~	~~0~~	1	0.25	N/A	N/A
De-assert Delay (ms)	~~N/A~~	~~0~~	~~0~~	0	0	N/A	N/A
Pinmode	0						

Figure 7. IO Pin Setting for Pinmode 0

IO Pin Settings							
	IO3	IO4	IO5	IO6	IO13	IO14	IO19
Direction	Input	Input	Input	Output	Output	Output	Output
Invert?	FALSE	FALSE	FALSE	FALSE	FALSE	TRUE	FALSE
Output Open Drain?	FALSE	FALSE	FALSE	FALSE	FALSE	FALSE	FALSE
Function*	Generic GPIO	Generic GPIO	Generic GPIO	PGOOD_GLB	PGOOD_ALWON	Global Interrupt	BKUP signal
Assert Delay (ms)	N/A	0	0	1	0.25	N/A	N/A
De-assert Delay (ms)	N/A	0	0	0	0	N/A	N/A
Pinmode	1						

Figure 8. IO Pin setting for Pinmode 1

IO14 behaves differently from other IOs for the "Invert?" option:

- If "Invert?" is set to TRUE, the signal is low when there is no fault and high when there is a fault.
- If "Invert?" is set to FALSE, the signal is high when there is no fault and low when there is a fault.

1.3.6 Buck and LDO Ramp Rate

Each regulator has configurable ramp rate options depending on the output voltage range.

- Refer to Table 2 for Buck 1-5 ramp rate options based on selected V_{OUT} range.
- Refer to Table 3 for LDO 1-4 ramp rate options based on output voltage. LDO 1-4 output voltage from 1.8V-1.89V use Ramp Rate 1 while 1.9V-3.3V uses Ramp Rate 2.
- Refer to Table 4 for LDO 5-6 ramp rate options.

Table 2. Buck Startup Ramp Rate Options

V_{OUT} Range Setting	Ramp Selection	Ramp Rate (mV/µS)
Buck 1-2 (0.3-1.2V) Buck 3-5 (0.5V-1.2V)	0	1.2
	1	3
	2	7.1
	3	14.2
	4	6
	5	12
Buck 1-2 (0.3V-1.6V) Buck 3-5 (0.5V-1.6V)	0	1.6
	2	3.2
	4	6.3
	6	12.6
Buck 1-2 (0.3V-2.4V) Buck 3-5 (0.5V-2.4V)	0	1.2
	2	2.4
	4	6
	6	12
Buck 1-2 (0.3V-3.3V) Buck 3-5 (0.5V-3.3V)	0	1.5
	2	3
	4	7.4
	6	14.8

Table 3. LDO 1-4 Startup Ramp Rate Options

Options	Ramp Rate 1 (mV/µs)	Ramp Rate 2 (mV/µs)
0	8.56	15.68
1	4.28	7.84
2	2.14	3.92
3	1.07	1.96
4	0.53	0.98
5	0.27	0.49
6	0.13	0.25

Table 4. LDO 5-6 Startup Ramp Rate Options

Option Number	Ramp Rate (mV/µS)
0	15.4
1	7.7
2	3.9
3	2
4	1
5	0.5
6	0.2

1.3.7 Spread Spectrum

The spread spectrum setting is disabled by default. To enable spread spectrum, select a Direction in cell H74. After a direction has been selected, the Algorithm Type, Algorithm Length, and Amplitude option is available. *Note:* The regulator must be set to Fix Frequency to enable spread spectrum. Figure 9 shows the selection for the Direction while Figure 10 shows the frequency setting.

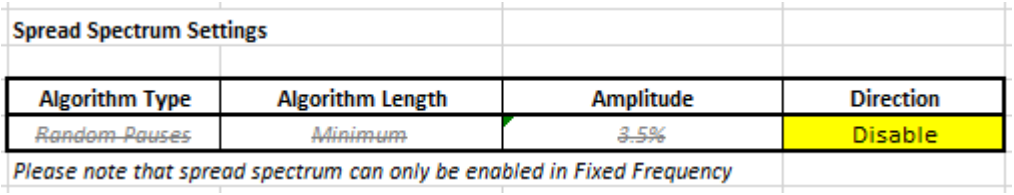


Figure 9. Spread Spectrum Selection

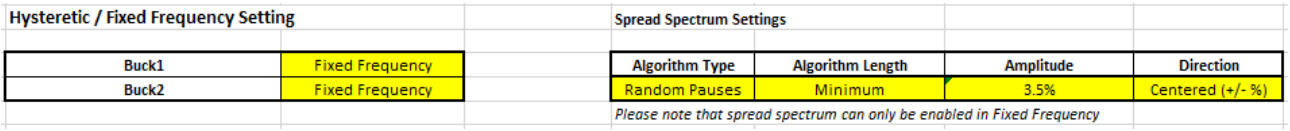


Figure 10. Frequency Setting once Spread Spectrum is Enabled

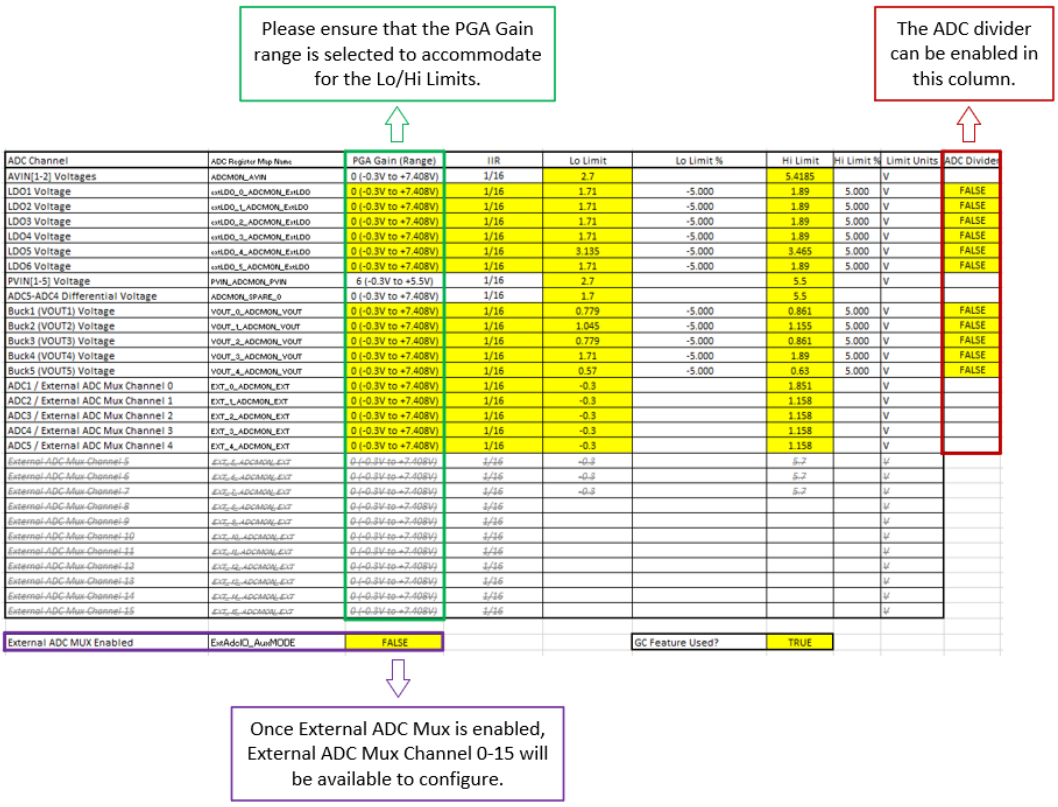
1.4 Protection Tab

1.4.1 ADC Channel Setting

In the ADC channel section, the Lo and Hi limits can be set for each regulator and ADC channel. There are eight PGA gain settings that set the voltage range of the input to the ADC. Table 5 shows the PGA gain options that can be independently set for each ADC channel.

Table 5. PGA Gain Options

Option Number	Input Voltage Range
0	-0.3V to +7.408V
1	-0.3V to +1.851V
2	-0.3V to +0.462V
3	-0.1V to +0.115V
4	-0.3V to +2.780V
5	-0.3V to +1.158V
6	-0.3V to +0.741V
7	-0.3V to +0.659V



ADC Channel	ADC Register Map Name	PGA Gain (Range)	IIR	Lo Limit	Lo Limit %	Hi Limit	Hi Limit %	Limit Units	ADC Divider
AVIN[1-2] Voltages	ADCMON_AVIN	0 (-0.3V to +7.408V)	1/16	2.7		5.4185		V	
LDO1 Voltage	extLDO_0_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
LDO2 Voltage	extLDO_1_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
LDO3 Voltage	extLDO_2_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
LDO4 Voltage	extLDO_3_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
LDO5 Voltage	extLDO_4_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	3.135	-5.000	3.465	5.000	V	FALSE
LDO6 Voltage	extLDO_5_ADCMON_ExtLDO	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
PVIN[1-5] Voltage	PVIN_ADCMON_PVIN	6 (-0.3V to +5.5V)	1/16	2.7		5.5		V	
ADC5-ADC4 Differential Voltage	ADCMON_SPARE_0	0 (-0.3V to +7.408V)	1/16	1.7		5.5			
Buck1 (VOUT1) Voltage	VOUT_0_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	0.779	-5.000	0.861	5.000	V	FALSE
Buck2 (VOUT2) Voltage	VOUT_1_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	1.045	-5.000	1.155	5.000	V	FALSE
Buck3 (VOUT3) Voltage	VOUT_2_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	0.779	-5.000	0.861	5.000	V	FALSE
Buck4 (VOUT4) Voltage	VOUT_3_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	1.71	-5.000	1.89	5.000	V	FALSE
Buck5 (VOUT5) Voltage	VOUT_4_ADCMON_VOUT	0 (-0.3V to +7.408V)	1/16	0.57	-5.000	0.63	5.000	V	FALSE
ADC1 / External ADC Mux Channel 0	EXT_0_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.851		V	
ADC2 / External ADC Mux Channel 1	EXT_1_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.158		V	
ADC3 / External ADC Mux Channel 2	EXT_2_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.158		V	
ADC4 / External ADC Mux Channel 3	EXT_3_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.158		V	
ADC5 / External ADC Mux Channel 4	EXT_4_ADCMON_EXT	0 (-0.3V to +7.408V)	1/16	-0.3		1.158		V	
~~External ADC Mux Channel 5~~	~~EXT_5_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~	~~-0.3~~		~~5.7~~		~~V~~	
~~External ADC Mux Channel 6~~	~~EXT_6_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~	~~-0.3~~		~~5.7~~		~~V~~	
~~External ADC Mux Channel 7~~	~~EXT_7_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~	~~-0.3~~		~~5.7~~		~~V~~	
~~External ADC Mux Channel 8~~	~~EXT_8_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 9~~	~~EXT_9_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 10~~	~~EXT_10_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 11~~	~~EXT_11_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 12~~	~~EXT_12_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 13~~	~~EXT_13_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 14~~	~~EXT_14_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
~~External ADC Mux Channel 15~~	~~EXT_15_ADCMON_EXT~~	~~0 (-0.3V to +7.408V)~~	~~1/16~~					~~V~~	
External ADC MUX Enabled	ExtAdcIO_AuxMODE	FALSE			GC Feature Used?	TRUE			

Figure 11. ADC Channel Setting

For applications where AVIN2 falls below a regulator programmed output voltage, the regulator ADC reading loses headroom because of the reduction in the ADC full scale range. The ADC divider can divide the ADC reading for that channel by half to accurately monitor the voltage of the regulator. For example, if LDO2 = 3.3V and AVIN2 drops to 3V, the ADC is not able to accurately show the LDO2 3V ADC reading, but if the ADC divider setting is enabled, the ADC properly shows 1.5V.

1.4.2 Temperature Setting during Active and SOC Activation

The temperature sensor is monitored by the ADC and temperature thresholds and can be set with a resolution of 0.25˚C. Figure 12 shows the options for the thermal warning and shutdown. The following are requirements:

- The Protection Thermal Warning (during Active) must be less than Protection Thermal Shutdown (during SoC activation).
- The Protection Thermal Shutdown (during Active) must be greater than Protection Thermal Shutdown (during SoC activation).

Temperature Setting During Active			
Protection Thermal Warning	ADCMON_WarnLimitLSB/MSB_Ter	90	°C
Protection Thermal Shutdown*	ADCMON_ShutDNLimitLSB/MSB_T	150	°C
*Note: Both Temp sensor 2 & 4 are controlled by same cell			
Temperature Setting During SOC Activation			
Protection Thermal Shutdown	120	°C	

Figure 12. Protection Thermal Warning and Shutdown

1.4.3 IO Pin Safe State Setting

The IO9 and IO10 pins can be configured to monitor the safe state of the PMIC. Refer to the *Safety Application Note* for more information on each PMIC safe state.

		IO9/SDO1	IO10/SSP
Start	SOC_PIN_DATA3/1	Hi-Z	Hi-Z
Self Diagnostic	SOC_PIN_DATA3/1	Hi-Z	Hi-Z
SoC Activation	SOC_PIN_DATA3/1	Hi-Z	Hi-Z
System Test (optional)	SOC_PIN_DATA3/1	Hi-Z	Hi-Z
Active	SOC_PIN_DATA4/2	Hi	Hi
Reset	SOC_PIN_DATA4/2	Lo	Hi
Error	SOC_PIN_DATA4/2	Hi	Lo
Lock	SOC_PIN_DATA4/2	Lo	Lo
Debug Mode	FUSA_CTRL_MTE	Hi	Hi

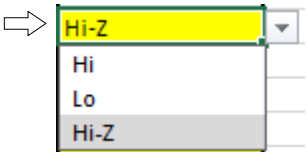


Figure 13. IO9 and IO10 Pin Safe State Setting

1.4.4 Watchdog

The watchdog feature checks if the PMIC is alive and responding correctly during a predetermined pull in interval. This interval can be set using the dropdown menu in Figure 14.

Watchdog					
Watchdog Enable	WDT_WWDT_EN	TRUE			
Advance Mode Q&A Scheme	WDT_WWDT_ADV_16Q	16 QA	WDT Mode Selection	WDT_WWDT_ADV_MO	Q&A
Watchdog Upper Limit (counts)	WDT_ULCNT	7			
Watchdog Lower Limit (counts)	WDT_LLCNT	4			
Watchdog Upper Limit (unit, s)	WDT_ULTICK	1m			
Watchdog Lower Limit (unit, s)	WDT_LLTICK	1m			
Watchdog Error Accumulator Limit	WDT_WWDT_ACC_TH	15			
Watchdog Question	WDT_DIS_LFSR	FALSE			

Figure 14. Watchdog Setting

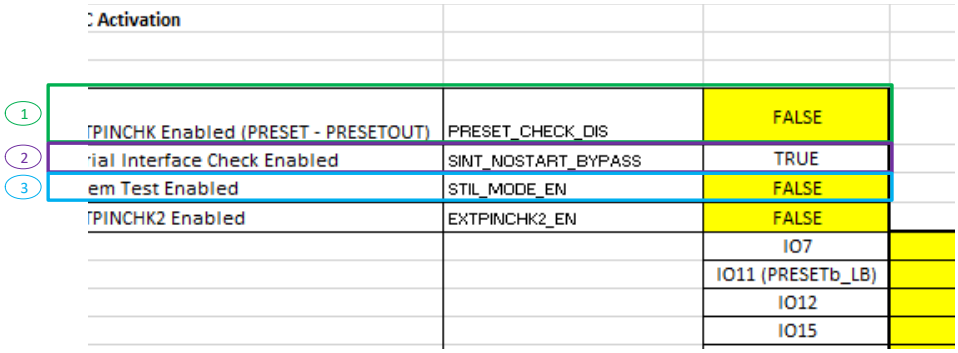
The following are some recommendations on setting up the watchdog:

- When the watchdog is enabled, the PMIC can be set as Q&A mode or Window mode.
- In Q&A mode, select between 16 QA or 4 QA.
- The watchdog upper limit needs to be higher than the lower limit.

1.4.5 SoC Activation and Timeout Setting

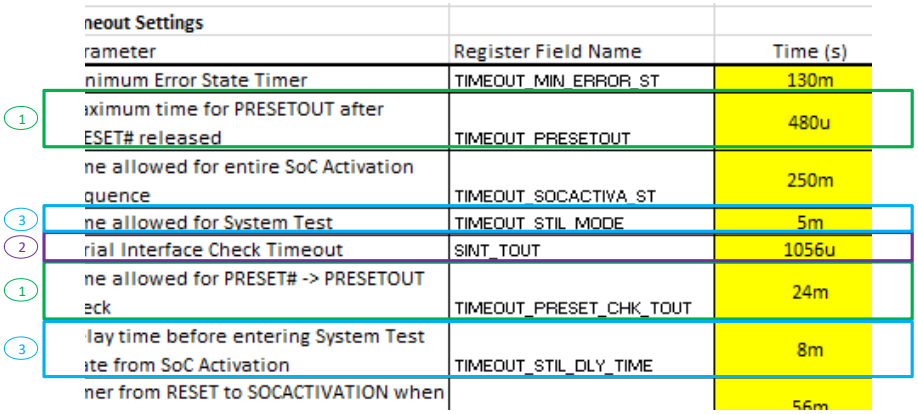
Each SoC Activation sequence test can be independently enabled. Figure 15 shows the configurable options. Refer to the *Safety Application Note* for more details.

The SoC activation timeout and error state timer can be configured to meet the required timing requirements (see Figure 16). When PRESET# Check, Serial Interface Check, or System Test is enabled, ensure the timeout setting is set appropriately. Each timeout setting is color coded to match the SoC Activation Test (see Figure 16).



	: Activation		
1	TPINCHK Enabled (PRESET - PRESETOUT)	PRESET_CHECK_DIS	FALSE
2	rial Interface Check Enabled	SINT_NOSTART_BYPASS	TRUE
3	em Test Enabled	STIL_MODE_EN	FALSE
	TPINCHK2 Enabled	EXTPINCHK2_EN	FALSE
			IO7
			IO11 (PRESETb_LB)
			IO12
			IO15

Figure 15. SoC Activation Test



	neout Settings		
	rameter	Register Field Name	Time (s)
	nimum Error State Timer	TIMEOUT_MIN_ERROR_ST	130m
1	ximum time for PRESETOUT after ESET# released	TIMEOUT_PRESETOUT	480u
	ne allowed for entire SoC Activation quence	TIMEOUT_SOCACTIVA_ST	250m
3	ne allowed for System Test	TIMEOUT_STIL_MODE	5m
2	rial Interface Check Timeout	SINT_TOUT	1056u
1	ne allowed for PRESET# -> PRESETOUT eck	TIMEOUT_PRESET_CHK_TOUT	24m
3	lay time before entering System Test ite from SoC Activation	TIMEOUT_STIL_DLY_TIME	8m
	ner from RESET to SOCACTIVATION when		56m

Figure 16. SoC Activiation Timeout and Error State Timer

1.4.6 Fault Masking

All fault masking options are located at the end of the protection tab. For initial sample testing, mask all faults except for the OV/UV faults and the PVIN fault. This setup allows for the easy verification of the regulators. After the output voltage of each regulator and sequence is confirmed, additional fault reactions can be unmasked for testing.

1.5 Additional Customer Specific Settings

The **Additional Customer Specific Settings** allows register settings that are not listed in the OTP creator to be configured. If required, contact a Renesas representative to help configure these settings.

2. Revision History

Revision	Date	Description
1.00	Nov 22, 2024	Initial release.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Disclaimer Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.