RAA271084 Board Layout Guidelines

Introduction

This application note provides guidelines for the RAA271084 board layout.

The RAA271084 is a general-purpose power management integrated circuit (PMIC) with a high voltage front-end, optimized for providing MCU power in automotive applications. The RAA271084 contains a high voltage primary buck/boost controller, a low voltage synchronous buck controller, and five low-dropout linear regulators (LDO), two of which can be used as trackers. The RAA271084 is available in a 48-lead SCQFN or 48-lead LQFP-EP. Proper PCB layout is an important design practice to ensure a satisfactory electrical and thermal performance.

Contents

1. RAA271084 Pinout and PCB Footprint

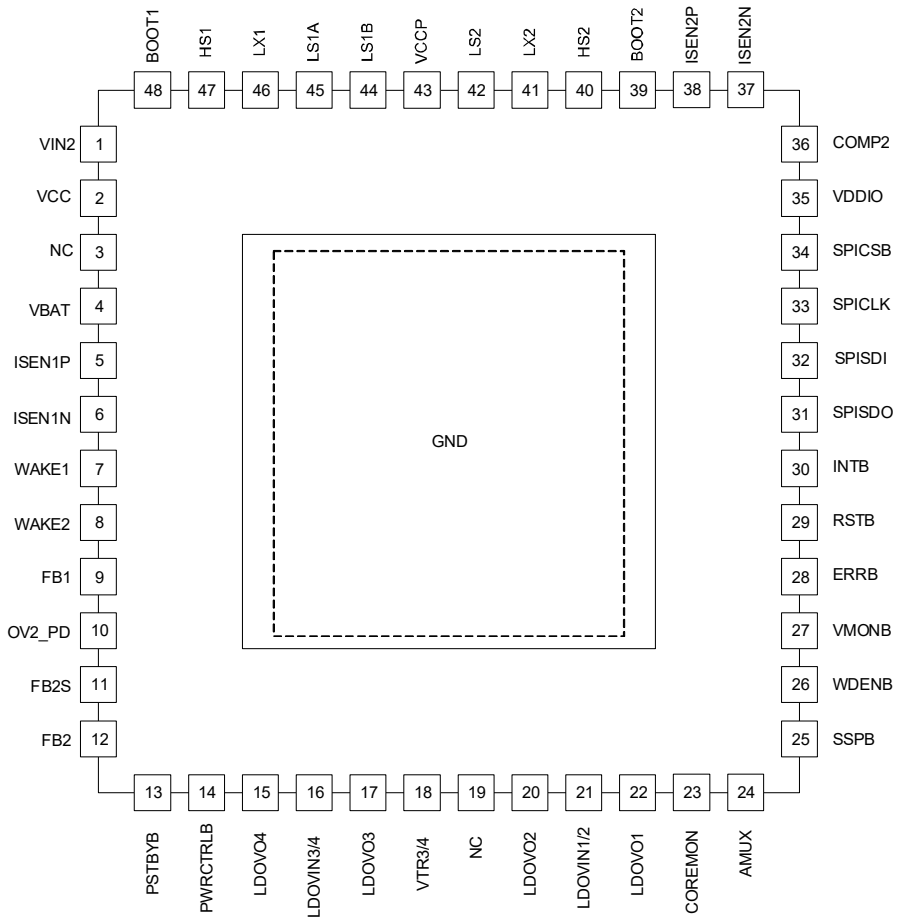


Figure 1. Pin Assignments - Top View

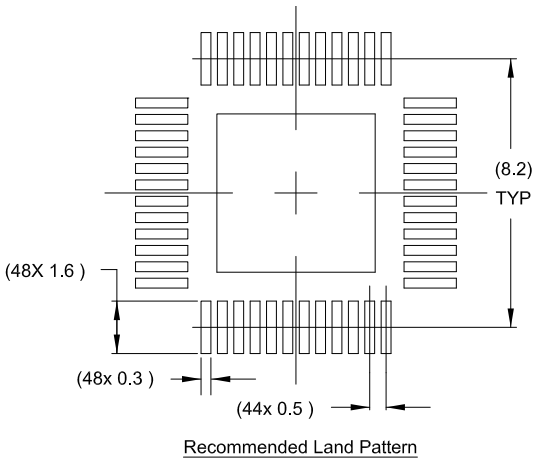


Figure 2. Recommended Land Pattern – Q48.7x7D

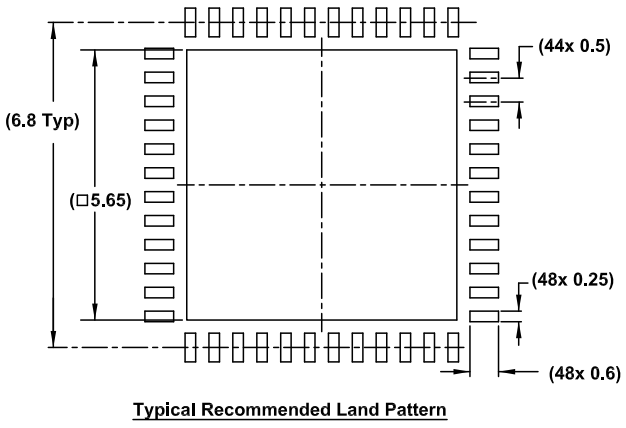


Figure 3. Typical Recommended Land Pattern – L48.7x7N

2. RAA271084 PCB Layout Guidelines

For the DCDC1 and DCDC2 switching regulators, the power delivery loop consists of the input capacitors C_{IN}, the MOSFETs, the LX switching node pin, the inductor L, the output capacitor C_{OUT}, and the GND pin. As Figure 1 illustrates, it is important to make the power delivery or current flow loop as small as possible. The PCB connecting traces among those components and pins should be direct, short, and wide. The PCB copper should be wide enough to minimize the current conduction loss and the parasitic inductance. Multiple solid ground layers are helpful to reduce the current flow resistance, have better thermal dissipation, and for a good EMI performance. Use enough vias to connect all the GND layers.

2.1 DCDC1 and DCDC2 Power Stage Components

Figure 4 illustrates a typical power stage components placement and layout pattern with respect to RAA271084. Dual FETs in one package can be used while the illustration uses single/standalone FET. The components are arranged to minimize the current flow path/loop, with the input capacitor, low side MOSFET, and the output capacitor connected with low impedance ground copper plane. A solid ground plane is helpful for a good EMI performance, current conduction, and thermal dissipation. Even if the DCDC1 and DCDC2 components cannot be placed close to each other, their placement should follow the illustrated pattern in Figure 5, as shown in the pink dot line frame.

- The input capacitor, low-side FET, and output capacitor should have low impedance ground connection.
- Use the wide and/or multiple layer ground copper plane to create low impedance current flow path.
- Minimize the copper area connecting to the inductor two terminals.
- Use the wide copper plane for the MOSFET to reduce the PCB parasitic and to have better thermal dissipation for the MOSFET.
- If there are multiple ground layers, use enough vias connecting them together.

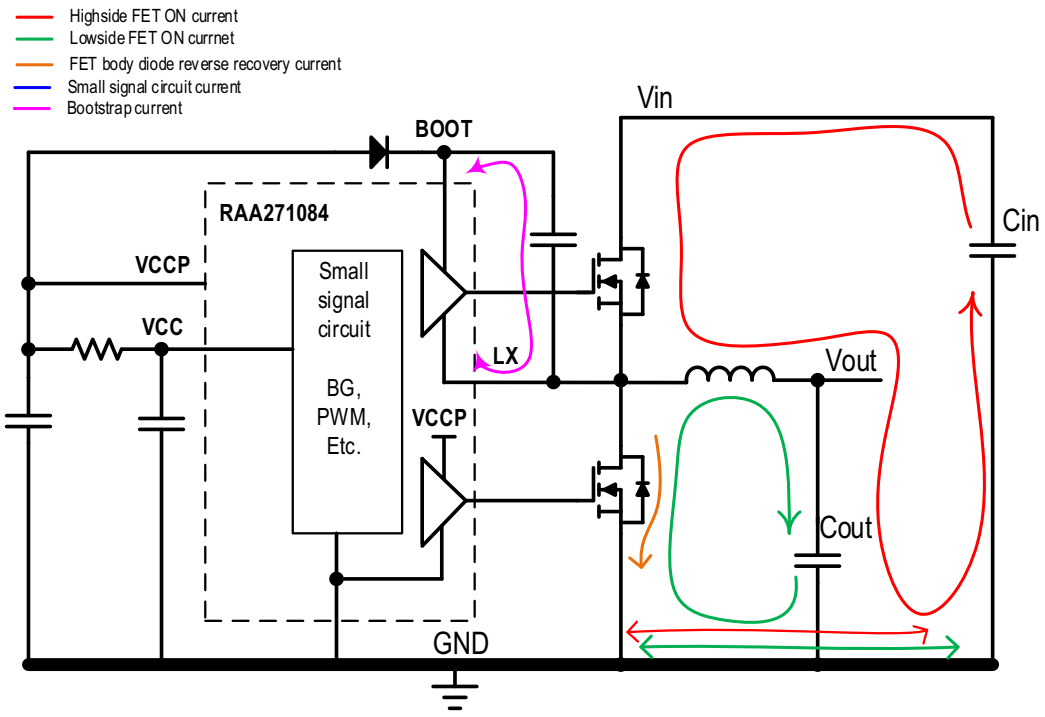


Figure 4. Component Placement and Layout Pattern

2.2 MOSFET Gate Drive Traces

Run MOSFT gate drive traces on a dedicated layer.

- For DCDC1, run HS1 and LX1 traces in parallel.
- For DCDC2, run HS2 and LX2 traces in parallel.

Use at least 10mil width for these traces. For all other signals, use ground copper to shield them from or keep distance from HS, LS, and LX via/trace/copper because they are noisy.

2.3 DCDC1 and DCDC2 Bootstrap Components

Place the bootstrap capacitor (and the resistor in series if any) close to BOOT pin and LX pin. Minimize the loop and PCB trace of Boot pin > Boot trace > Cboot > LX trace.

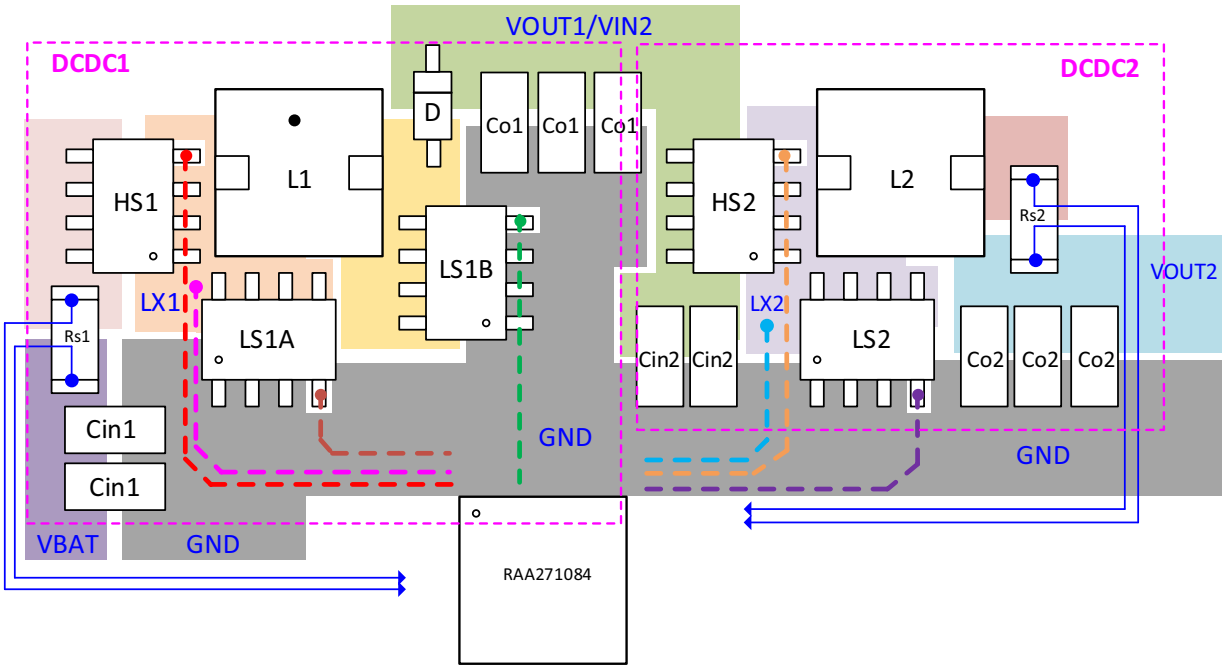
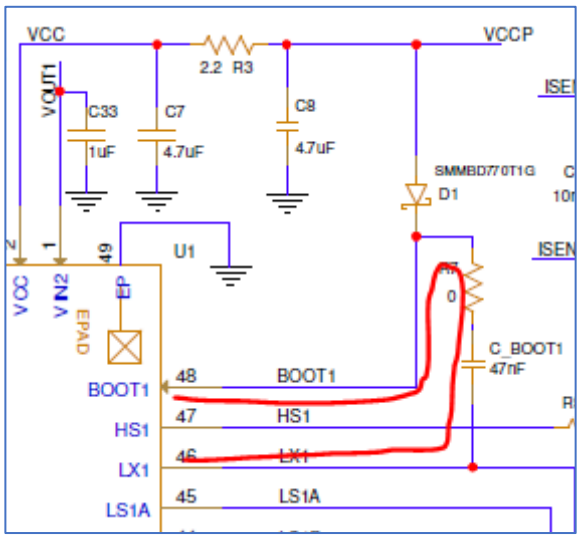


Figure 5. Bootstrap Components (1 of 2)

Use at least 10mil width trace for the Boot trace and LX trace to conduct the high-side FET driving current.

For all other signals, use ground copper to shield them or keep distance from VCCP, BOOT, and LX traces, because they carry the high-side FET driving current and are noisy.



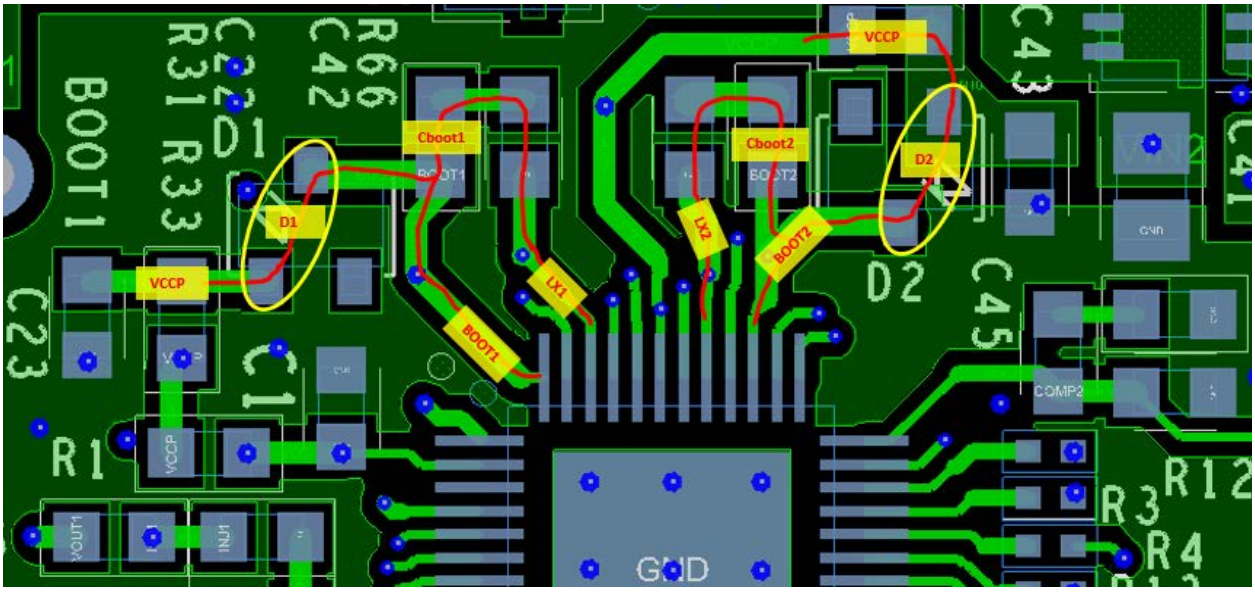


Figure 6. Bootstrap Components (2 of 2)

2.4 DCDC1 and DCDC2 Current Sensing

Run the current-sensing traces ISEN1P/ISEN1N (or ISEN2P/ISEN2N) from the current-sensing shunt resistor to RAA271084 in parallel. Shield them with ground copper. Place the RC filter resistor and capacitor close to the RAA271084 package.

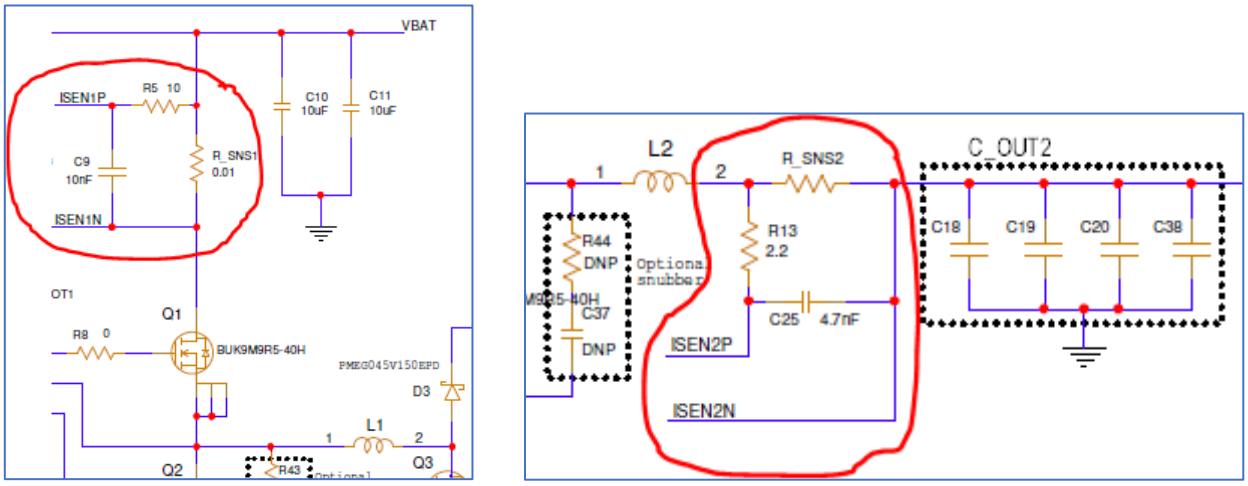


Figure 7. Current-Sensing Traces

2.5 RAA271084 Ground

Use multiple vias connecting the RAA271084 ground pad to the internal ground copper plane for lower ground impedance and better thermal dissipation.

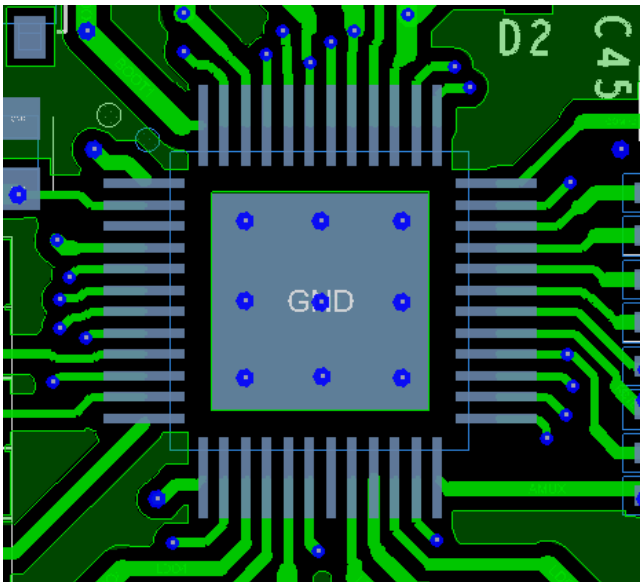


Figure 8. Ground Pad

2.6 Output Voltage Feedback Traces

Run the FB1 and FB2/FB2S output voltage feedback away from the FET gate drive related traces (HS, LS, LX, BOOT, VCCP). Also, stay away from any high-speed digital signals such as SPI communication lines. Shield them with ground copper. Place the FB2/FB2S voltage divider resistors close to RAA271084 package.

2.7 Other Components and PCB Routing

- Place the decoupling capacitors close to VBAT, VCC, VCCP, VIN2, VDDIO, VTR3/4, LDOIN1/2, and LDOIN3/4 pins with a good ground copper connection.
- Place DCDC2 loop compensation components close to the COMP2 pin, with good ground copper connection.
- All other digital or logic signals such as WAKE1/2, SSPB, RSTB, and INTB are not a big concern in the PCB layout.

As shown in Figure 9, place the resistors and capacitors close to RAA271084, connect them to the ground copper surrounding the RAA271084, and connect the ground copper to the ground copper on other layers multiple vias.

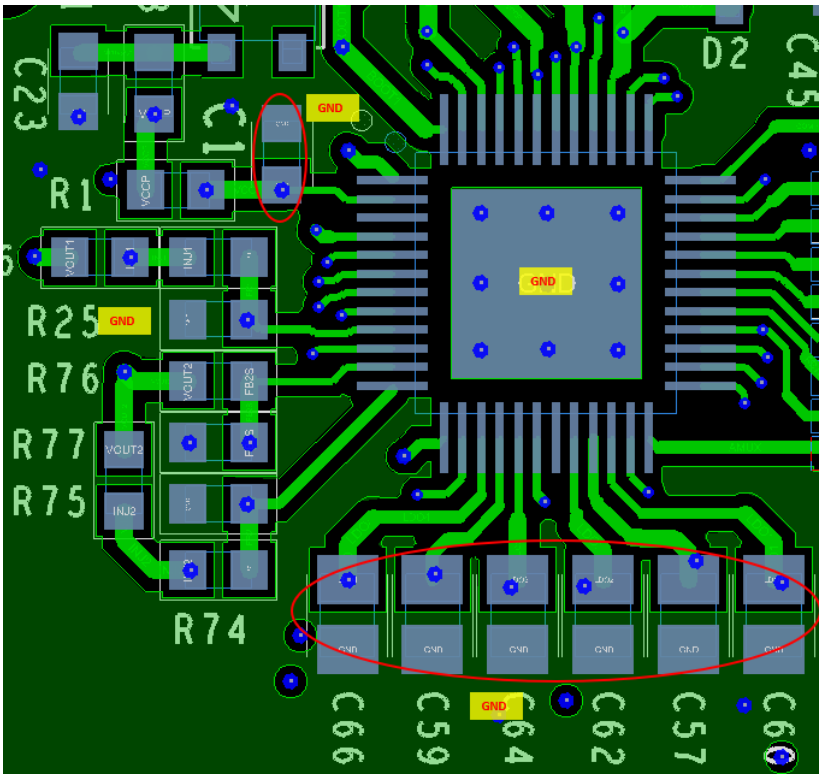


Figure 9. PCB Routing

3. Quick Summary of the PCB Layout Practice

1. Place the DCDC1 and DCDC2 power stage components in a compact fashion with low impedance copper plane and good ground connection.
2. Route FET gate drive related traces with short, wide traces, and avoid any sensitive signals.
3. Route output voltage feedback sensing traces to the load point and the high frequency ceramic bank to minimize the feedback noise. Shield or stay away from the switching related signals.
4. Route the current sensing traces in parallel and shield with ground copper.
5. Use enough vias connecting to the different layers and enough PCB copper width for low impedance current flow and minimized parasitic inductance

4. Revision History

Revision	Date	Description
1.00	Jun 23, 2025	Initial release.

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