RAA271084 Power Supply Circuit Design for RH850/U2B24

This application note describes how to connect the RAA271084 power management IC (PMIC) with the RH850/U2B24 automotive 32-bit microcontroller (MCU), providing examples and guidelines for power on/off requirements, low power mode supported by the RAA271084, recommendations for unused pins, and OTP settings.

- **Target Device**: RAA271084
- **Target MCU**: RH850/U2B24

Contents

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1. Power Solution Examples

The RAA271084 contains a high-voltage primary buck/boost controller, a low-voltage synchronous buck controller and five low-dropout liner regulators (LDO), two of which can be used as trackers. DCDC switching frequency, output voltage, power-up/down sequence and other features can be configured by OTP.

There are four power solution examples for the RH850/U2B24 using the RAA271084. The main differences in the examples are the MCU SVR function used/unused and SBMD = 0/1. These are described in the following sub-sections.

Example 1 (section 1.1) is a minimum BoM area solution. In this connection, SBMD is set to 0 and the MCU VDD is directly supplied from the RAA271084 DCDC2 regulator output. The LDO1–4 outputs are used to supply other MCU power rails. The direct V_{DD} supply reduces BoM area by eliminating the BoM of the MCU embedded voltage regulator (SVR). For more information on RH850/U2B24 SVR functions, see References item [2].

Example 2 (section 1.2) is minimum BoM area solution. In this connection, SBMD is set to 1 and the MCU V_{DD} is directly supplied from the RAA271084 DCDC2 regulator output. The LDO1–4 outputs are used to supply other MCU power rails. The direct V_{DD} supply reduces BoM area by eliminating the BoM of the MCU embedded voltage regulator (SVR). For more information on RH850/U2B24 SVR functions, see References item [2].

Example 3 (section 1.3) is a flexible power supply solution. In this connection, SBMD is set to 0 and the DCDC2 regulator is used to supply the MCU SVR and other power-rails. Compared with example1, the LDO output can be used for other power rails than those of the MCU.

Example 4 (section 1.4) is a flexible power supply solution. In this connection, SBMD is set to 1 and the DCDC2 regulator is used to supply the MCU SVR and other power-rails. Compare with example2, the LDO output can be used for other power rails than those of the MCU.

Important: When DCDC2 output is set 5V, the switching frequency required is 440kHz. When the DCDC2 output is 3.3V or less, the switching frequency can be 440kHz or 2.2MHz. DCDC1 switching frequency can be 440kHz or 2.2MHz.

1.1 Example 1 – Power Configuration Block Diagram for RH850/U2B24 without SVR (SBMD = 0)

The RAA271084 has two buck controllers and five LDOs. These outputs are controlled by Wake1 and Wake2. Figure 1 shows an example of a connection with the RH850/U2B24 and RAA271084 without SVR (SBMD = 0). While SBMD = 0, AWOVCL should be connected to the 1.09V power rail.

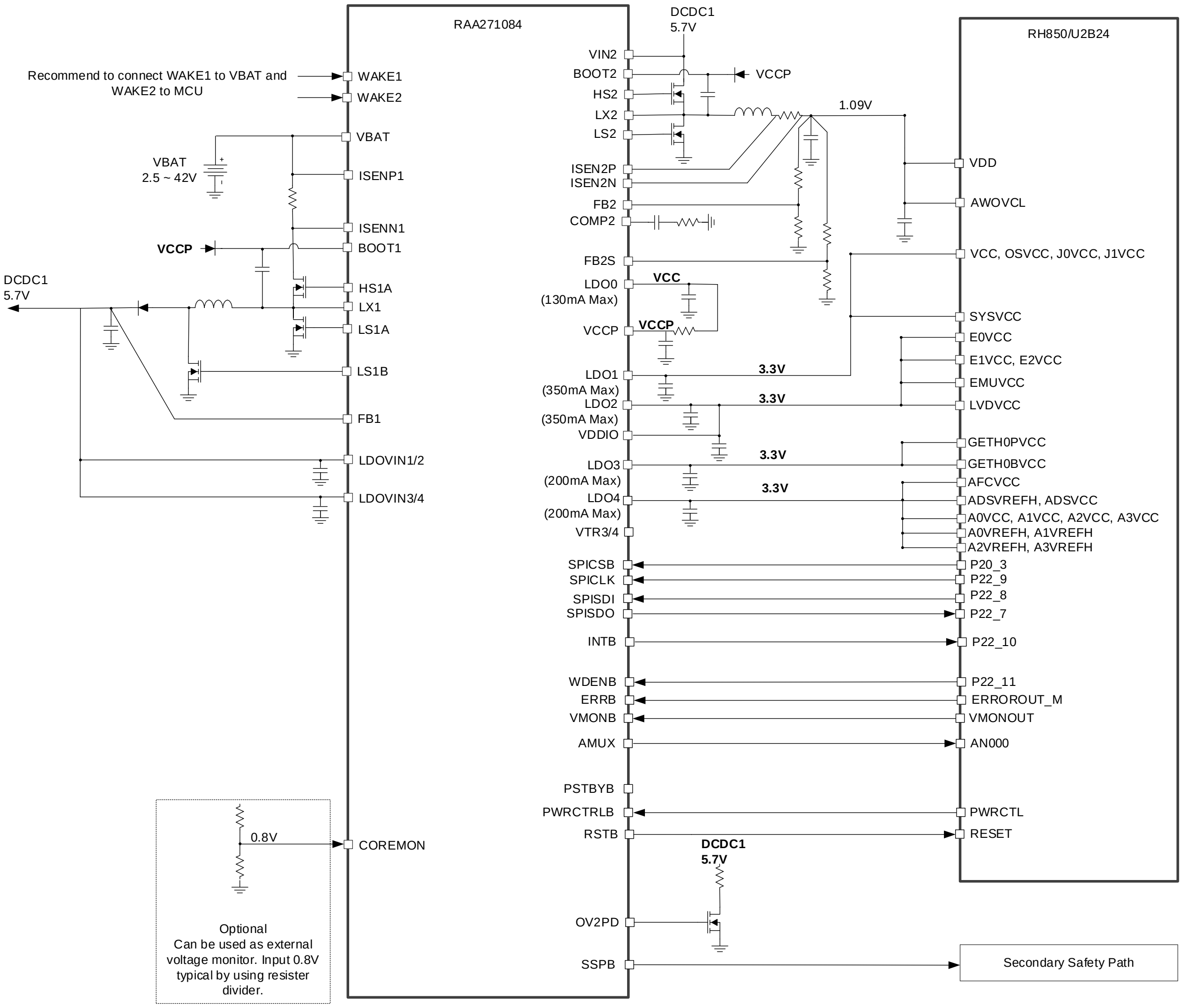

Figure 1. RAA271084 Application Diagram Showing RH850/U2B24 without SVR (SBMD = 0)

Table 1. Regulator Connection for Example 1

Regulators	Output Voltage	PMIC Output Current Capability	Supply for
DCDC1	5.7V	-	VIN2, LDOVIN1/2, and LDOVIN3/4 of RAA271084
DCDC2	1.09V	-	MCU VDD
LDO1	3.3V	350mA	VCC, OSCVCC, J0VCC, J1VCC, SYSVCC of MCU
LDO2	3.3V	350mA	E0VCC, E1VCC, E2VCC, EMUVCC, and LVDVCC of MCU
LDO3	3.3V	200mA	GETH0PVCC, GETH0BVCC of MCU
LDO4	3.3V	200mA	AFCVCC, ADSVREFH, ADSVCC, A0VCC, A1VCC, A2VCC, A3VCC, A0VREFH, A1VREFH, A2VREFH, and A3VREFH of MCU

Regulators	Output Voltage	PMIC Output Current Capability	Supply for
VCC(LDO0)	5V	130mA	VCCP of RAA271084

Table 2. I/O Connections

The RAA271084		The RH850/U2B24
Pin#	**Pin name**	**Pin name**
7	WAKE1	-
8	WAKE2	-
10	OV2_PD	(External FET gate)
13	PSTBYB	-
14	PWRCTLB	PWRCTL
23	COREMON	(Optional, external 0.8V)
24	AMUX	AN000
25	SSPB	(Depends on System)
26	WDENB	P22_11
27	VMONB	VMONOUT
28	ERRB	ERROROUT_M
29	RSTB	RESET
30	INTB	P22_10
31	SPISDO	P22_7
32	SPISDI	P22_8
33	SPICLK	P22_9
34	SPICSB	P20_3

Note: () is not MCU pins.

1.2 Example 2 – Power Configuration Block Diagram for RH850/U2B24 without SVR (SBMD = 1)

The RAA271084 has two buck controllers and five LDOs. These outputs are controlled by Wake1 and Wake2. Figure 2 shows an example of a connection with the RH850/U2B24 and RAA271084 without SVR (SBMD = 1). While SBMD = 1, AWOVCL should be connected to the 1.09V power rail.

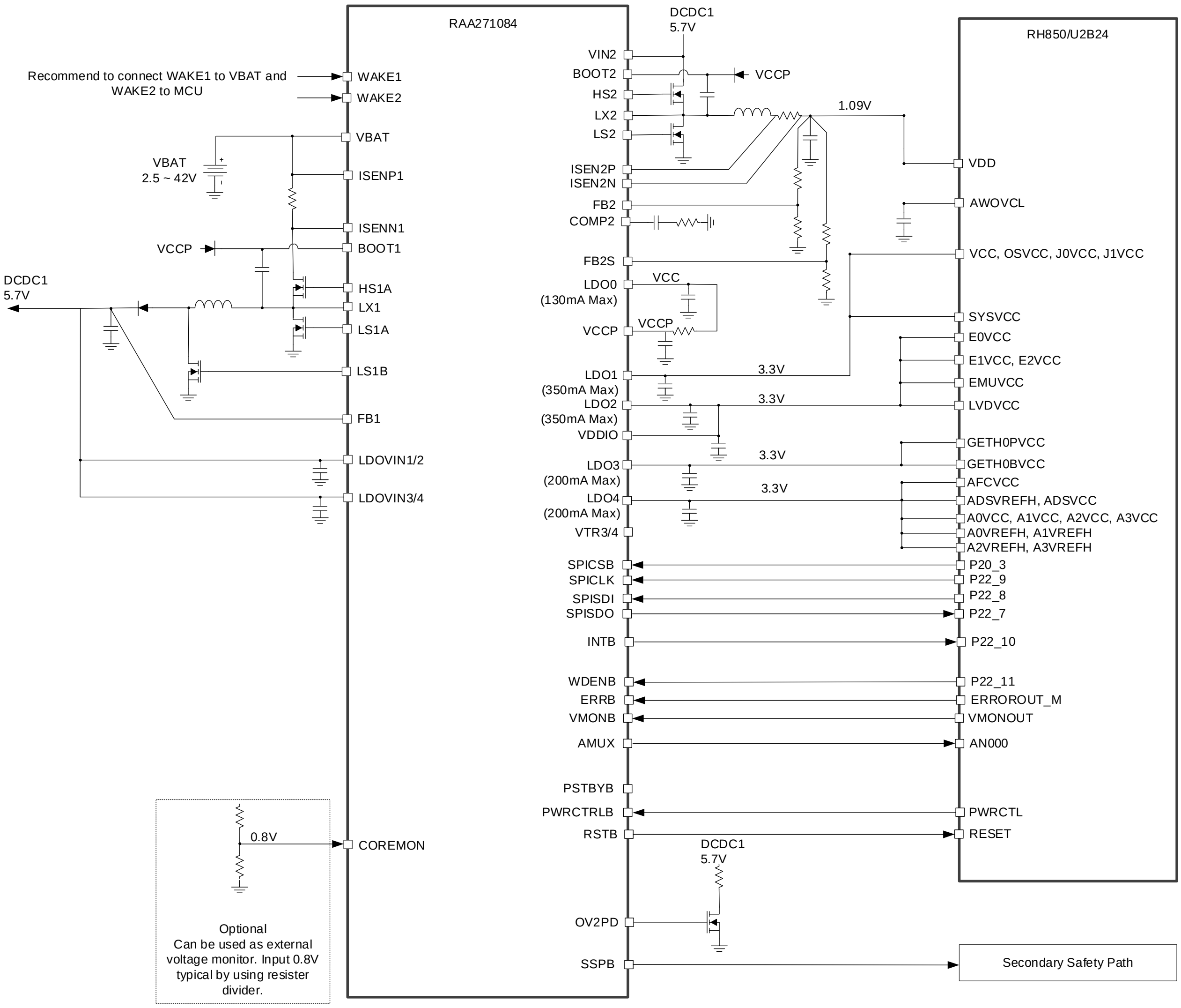

Figure 2. RAA271084 Application Diagram Showing RH850/U2B24 without SVR (SBMD = 1)

Table 3. Regulator Connection for Example 2

Regulators	Output Voltage	PMIC Output Current Capability	Supply for
DCDC1	5.7V	-	VIN2, LDOVIN1/2, and LDOVIN3/4 of RAA271084
DCDC2	1.09V	-	MCU VDD
LDO1	3.3V	350mA	VCC, OSCVCC, J0VCC, J1VCC, SYSVCC of MCU
LDO2	3.3V	350mA	E0VCC, E1VCC, E2VCC, EMUVCC, and LVDVCC of MCU
LDO3	3.3V	200mA	GETH0PVCC, GETH0BVCC of MCU
LDO4	3.3V	200mA	AFCVCC, ADSVREFH, ADSVCC, A0VCC, A1VCC, A2VCC, A3VCC, A0VREFH, A1VREFH, A2VREFH, and A3VREFH of MCU

Regulators	Output Voltage	PMIC Output Current Capability	Supply for
VCC(LDO0)	5V	130mA	VCCP of RAA271084

Table 4. I/O Connections

The RAA271084		The RH850/U2B24
Pin#	**Pin name**	**Pin name**
7	WAKE1	-
8	WAKE2	-
10	OV2_PD	(External FET gate)
13	PSTBYB	RESETOUT
14	PWRCTLB	PWRCTL
23	COREMON	(Optional, external 0.8V)
24	AMUX	AN000
25	SSPB	(Depends on System)
26	WDENB	P22_11
27	VMONB	VMONOUT
28	ERRB	ERROROUT_M
29	RSTB	RESET
30	INTB	P22_10
31	SPISDO	P22_7
32	SPISDI	P22_8
33	SPICLK	P22_9
34	SPICSB	P20_3

Note: () is not MCU pins.

1.3 Example 3 – Power Configuration Block Diagram for RH850/U2B24 with SVR (SBMD = 0)

The RAA271084 has two buck controllers and five LDOs. These outputs are controlled by Wake1 and Wake2. Figure 3 shows an example of a connection with the RH850/U2B24 and RAA271084 with SVR (SBMD = 0); V_{DD} is supplied by SVR. While SBMD = 0, AWOVCL should be connected to the 1.09V power rail.

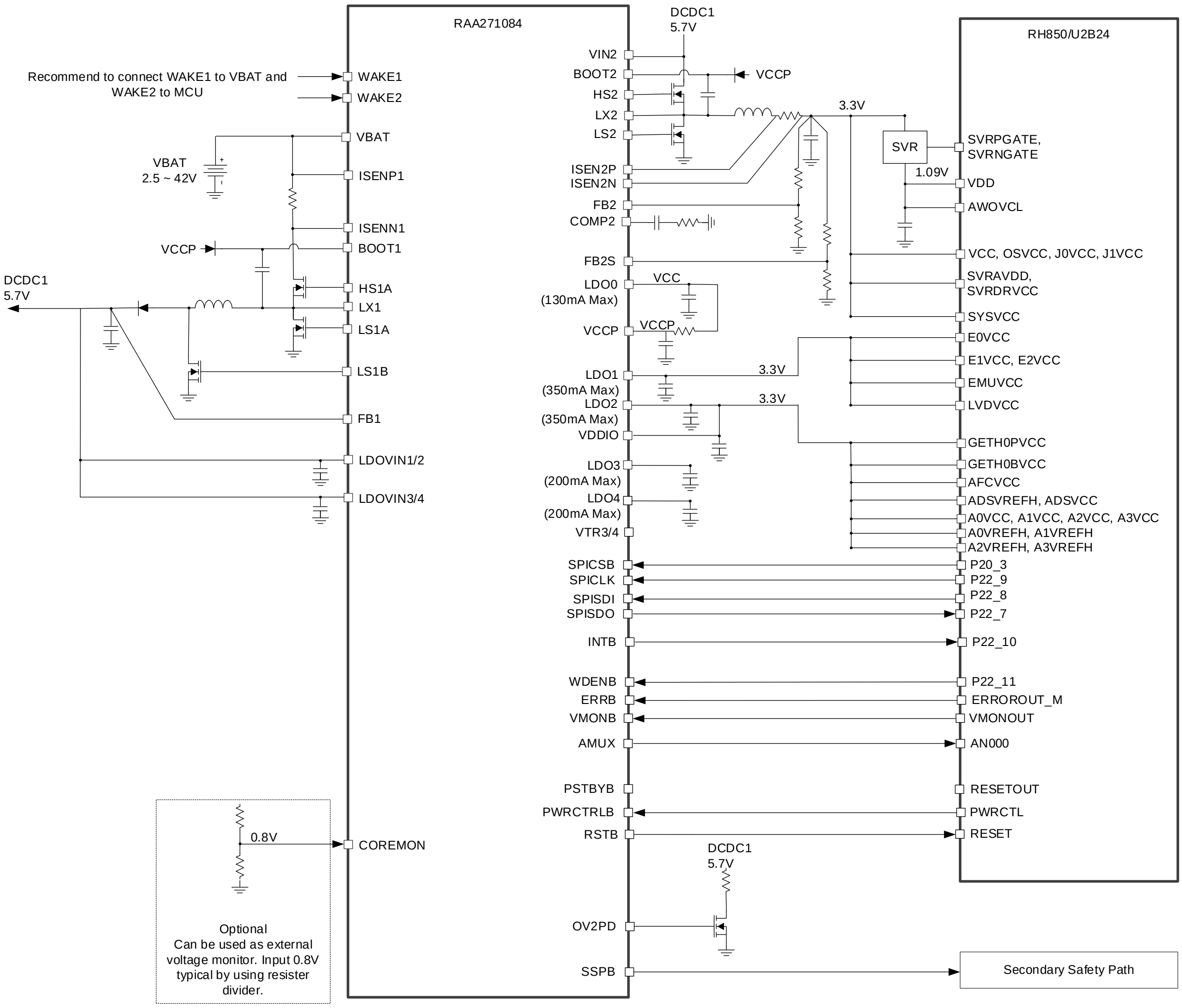

Figure 3. RAA271084 Application Diagram Showing RH850/U2B24 with SVR (SBMD = 0)

Table 5. Regulator Connection for Example 3

Regulators	Output Voltage	PMIC Output Current Capability	Supply for
DCDC1	5.7V	-	VIN2, LDOVIN1/2, and LDOVIN3/4 of RAA271084
DCDC2	3.3V	-	INPUT of SVR
LDO1	3.3V	350mA	VCC, OSCVCC, J0VCC, J1VCC, SYSVCC, SVRAVDD, and SVRDRVCC of MCU
LDO2	3.3V	350mA	E0VCC, E1VCC, E2VCC, LVDVCC, and EMUVCC of MCU
LDO3	3.3V	200mA	GETH0PVCC, GETH0BVCC of MCU

Regulators	Output Voltage	PMIC Output Current Capability	Supply for
LDO4	3.3V	200mA	AFCVCC, ADSVREFH, ADSVCC, A0VCC, A1VCC, A2VCC, A3VCC, A0VREFH, A1VREFH, A2VREFH, and A3VREFH of MCU
VCC(LDO0)	5V	130mA	VCCP of RAA271084

Table 6. I/O Connections

The RAA271084		The RH850/U2B24
Pin#	**Pin name**	**Pin name**
7	WAKE1	
8	WAKE2	
10	OV2_PD	(External FET gate)
13	PSTBYB	RESETOUT
14	PWRCTLB	PWRCTL
23	COREMON	(Optional, external 0.8V)
24	AMUX	AN000
25	SSPB	(Depends on System)
26	WDENB	P22_11
27	VMONB	VMONOUT
28	ERRB	ERROROUT_M
29	RSTB	RESET
30	INTB	P22_10
31	SPISDO	P22_7
32	SPISDI	P22_8
33	SPICLK	P22_9
34	SPICSB	P20_3

Note: () is not MCU pins.

1.4 Example 4 – Power Configuration Block Diagram for RH850/U2B24 with SVR (SBMD = 1)

Figure 3 shows an example of a connection with the RH850/U2B24 and RAA271084 with SVR (SBMD = 0); V_{DD} is supplied by SVR. While SBMD = 1, AWOVCL is a power supply for connecting internal circuits to external buffer capacitors.

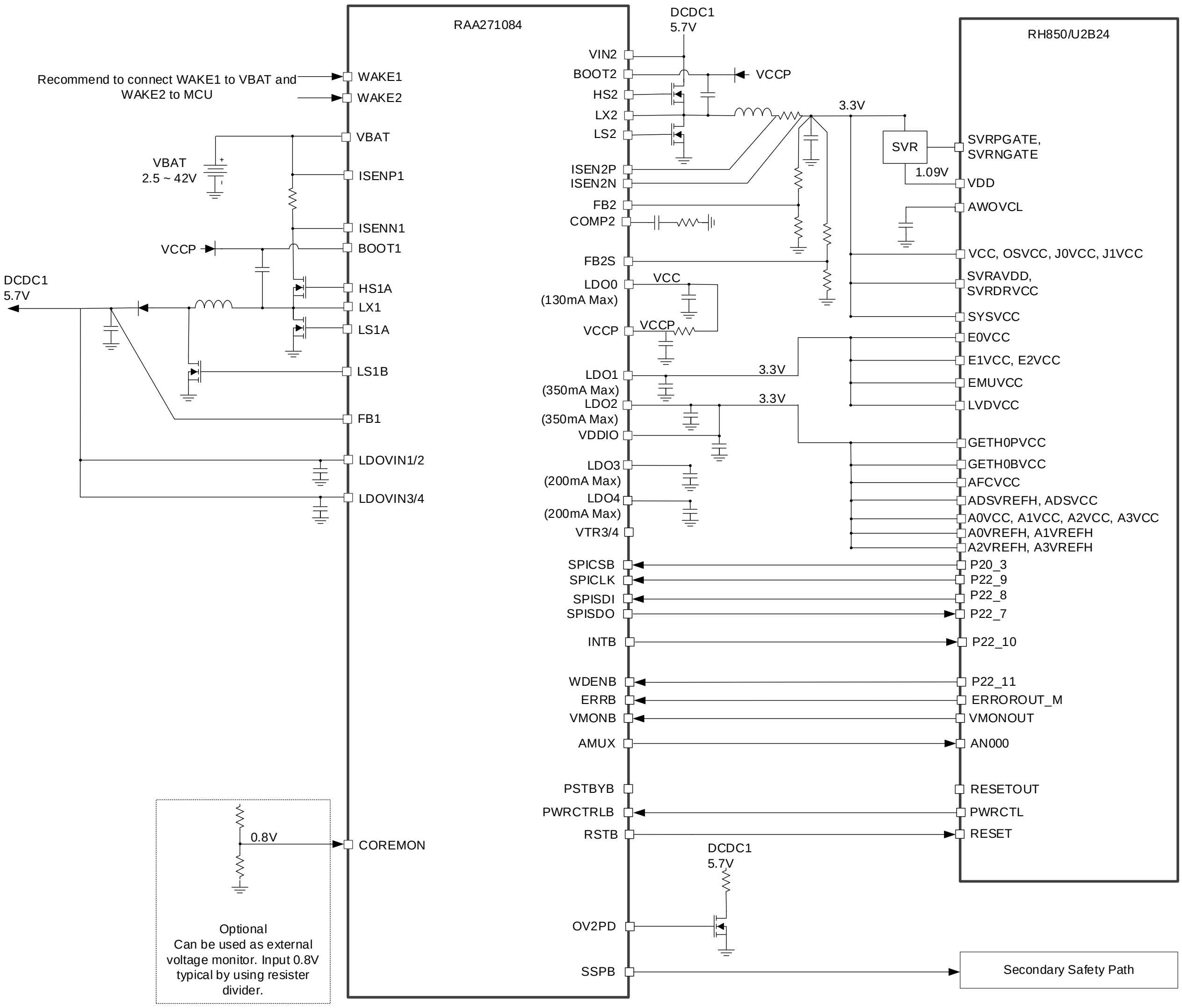

Figure 4. RAA271084 Application Diagram Showing RH850/U2B24 with SVR (SBMD = 1)

Table 7. Regulator Connections for Example 4

Regulators	Output Voltage	Output Current	Supply for
DCDC1	5.7V	-	VIN2, LDOVIN1/2, and LDOVIN3/4 of RAA271084
DCDC2	3.3V	-	INPUT of SVR
LDO1	3.3V	350mA	VCC, OSCVCC, J0VCC, J1VCC, SYSVCC, SVRAVDD, and SVRDRVCC of MCU
LDO2	3.3V	350mA	E0VCC, E1VCC, E2VCC, LVDVCC, and EMUVCC of MCU
LDO3	3.3V	200mA	GETH0PVCC, GETH0BVCC of MCU

Regulators	Output Voltage	Output Current	Supply for
LDO4	3.3V	200mA	AFCVCC, ADSVREFH, ADSVCC, A0VCC, A1VCC, A2VCC, A3VCC, A0VREFH, A1VREFH, A2VREFH, and A3VREFH of MCU
VCC(LDO0)	5V	130mA	VCCP of RAA271084

Table 8. I/O Connections

The RAA271084		The RH850/U2B24
Pin#	**Pin Name**	**Pin Name**
7	WAKE1	
8	WAKE2	
10	OV2_PD	(External FET gate)
13	PSTBYB	RESETOUT
14	PWRCTLB	PWRCTL
23	COREMON	(Optional, external 0.8V)
24	AMUX	AN000
25	SSPB	(Depends on System)
26	WDENB	P22_11
27	VMONB	VMONOUT
28	ERRB	ERROROUT_M
29	RSTB	RESET
30	INTB	P22_10
31	SPISDO	P22_7
32	SPISDI	P22_8
33	SPICLK	P22_9
34	SPICSB	P20_3

Note: () is not MCU pins.

2. RAA271084 Power On/Off Requirements from the RH850/U2B24

The RH850/U2B24 is a sequence-free product. Thus, only power-on-reset timing and power-hold time requirements are considered when the regulators are disabled. Both requirements are satisfied by the RAA271084 if any OTP settings for the power-on/off sequence timings are set (OPT_SEQ_CTRL, OPT_SLOT_TIME, OPT_SLOT_DCDC, OPT_SLOT_LDO, OPT_TOFF_TIME, or OPT_RSTB_DLY).

For power-on timing, keep the RESET at Low during t_{RESH1} after all MCU power rails are supplied. The order of the power supplies are not required for the MCU power rails. The startup timing of each regulator and RSTB hold time for the RAA271084 are configurable. Any settings of OPT_SEQ_CTRL, OPT_SLOT_TIME, OPT_SLOT_DCDC, OPT_SLOT_LDO, or OPT_RSTB_DLY satisfies the RH850/U2B24 requirement. For more information about configurable items and timings, refer to the *Timing Summary* section of the RAA271084 datasheet.

For power-off timing, keep the power-rails High during t_{PWH} from RESET = Low in order to avoid damaging the device. The RAA271084 regulators can configure the off delay time (regulator output hold time when the regulator is disabled.). Any setting of OPT_TOFF_TIME satisfies the RH850/U2B24 requirement.

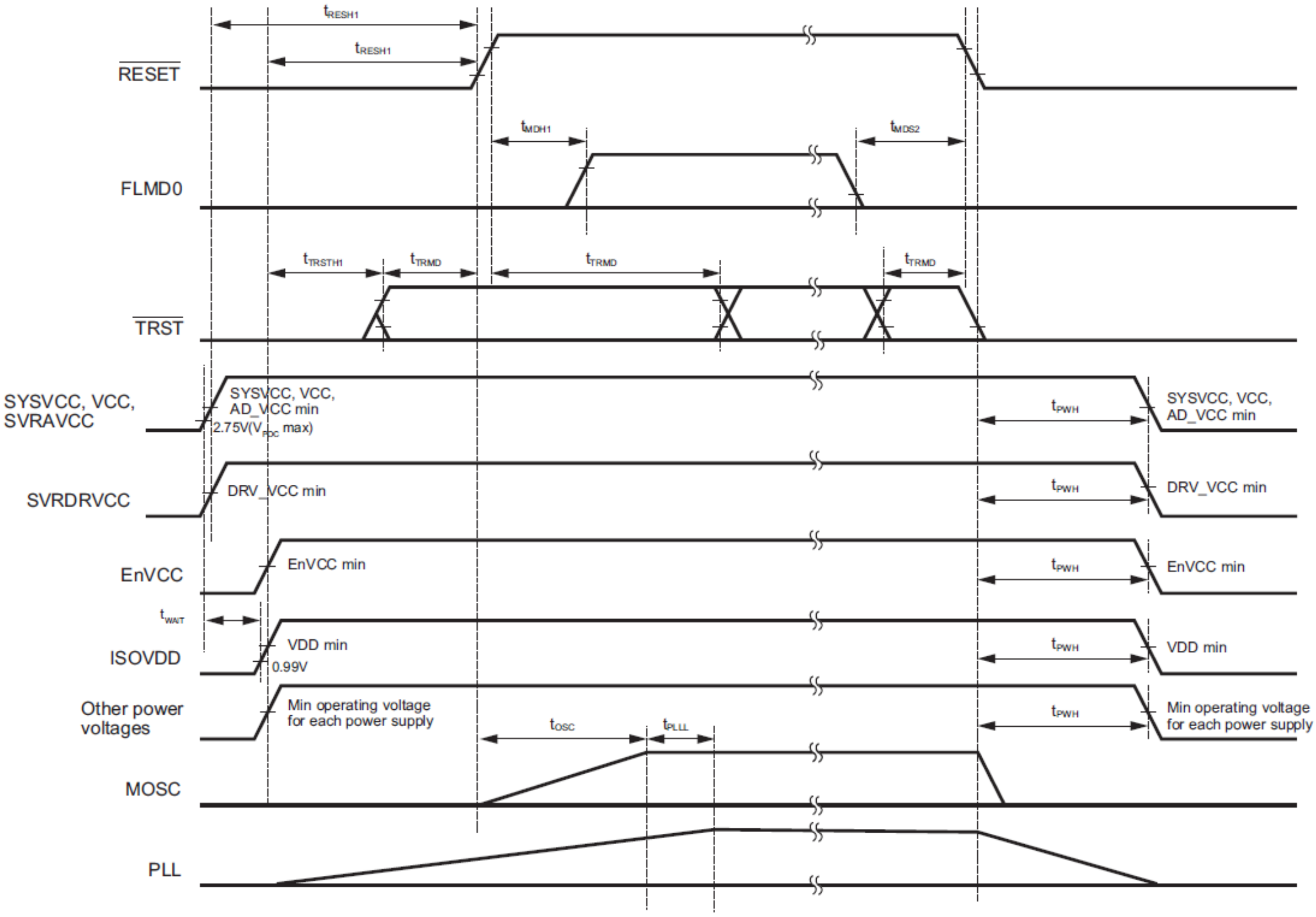

Figure 5. RH850/U2B24 Power On/Off Timings (Normal Operating Mode and User Boot Mode 0)

Note: For more information, refer to the *Power On/Off Timing* section of the RH850/U2B24 hardware manual.

3. Supported Settings for the MCU Low-Power Mode

The RH850/U2B24 provides DeepSTOP mode as the low-power mode. The RAA271084 contains a dedicated DeepSTOP mode to support this setting. The RAA271084 stops the power supply for the MCU V_{DD} during DeepSTOP mode. The regulator output state in DeepSTOP is configurable by OTP and the output status is shown in Table 9. For more information about how to enter/exit the DeepSTOP mode, refer to the *DeepSTOP Entry/Exit* section of the RAA271084 datasheet.

In Example 1 (see Table 9), DCDC2 is disabled because it is supplied by V_{DD}. Other regulators are enabled to retain the MCU power supply.

In Example 3 (see Table 9), DCDC2 is enabled because it supplies not only the MCU SVR but other MCU power rails as well. LDO3 and LDO4 are disabled as they do not provide a supply to the MCU.

Note: LDO3 and LDO4 output statuses depends on the connecting devices and system requirements.

Table 9. Regulator State at DeepSTOP Mode

Assumed Use-Case at DeepSTOP Mode							
Regulators	**LDO0**	**DCDC1**	**DCDC2**	**LDO1**	**LDO2**	**LDO3**	**LDO4**
Example 1	On	On	Off	On	On	On	On
Example 3	On	On	On	On	On	Off*	Off*

4. Unused Pins Recommendations

This section describes recommendations for unused pins (see Table 10). For any functions or pins that are not being used, change the OTP configuration from the recommended values (described in Table 11) to what is noted in Table 10.

Table 10. RAA271084 Unused Pins Recommendations

Pin No.	Pin Name	I/O	Recommended Handling of Unused Pin(s)	Note
3	NC	-	Open	-
7	WAKE1	Input	Connect to ground	Use either WAKE1 or WAKE2.
8	WAKE2	Input	Connect to ground	Use either WAKE1 or WAKE2.
10	OV2_PD	Output	Open	-
13	PSTBY	Input	Open	-
14	PWRCTRLB	Input	Open	-
15	LDOVO4	Output	Open	Set LDO4 as disabled by OTP.
16	LDOVIN3/4	Input	Open	Set LDO3 and LDO4 as disabled by OTP.
17	LDOVO3	Output	Open	Set LDO3 as disabled by OTP.
18	VTR3/4	Input	Open	Set LDO3 and LDO4 as LDO output by OTP.
19	NC	-	Open	-
20	LDOVO2	Output	Open	Set LDO2 as disabled by OTP.
21	LDOVIN1/2	Input	Open	Set LDO1 and LDO2 as LDO output by OTP.

Pin No.	Pin Name	I/O	Recommended Handling of Unused Pin(s)	Note
22	LDOVO1	Output	Open	Set LDO1 as disabled by OTP.
23	COREMON	Input	Connect to ground	-
24	AMUX	Output	Open	-
25	SSPB	Output	Open	-
26	WDENB	Input	Connect to ground	-
27	VMONB	Input	Connect to ground	-
28	ERRB	Input	Connect to ground	-
30	INTB	Output	Open	-
31	SPISDO	Output	Open	-
32	SPISDI	Input	Open	-
33	SPICLK	Input	Open	-
34	SPICSB	Input	Open	-

5. OTP Configuration Recommendations

The RAA271084 has a custom configuration saved in one time programmable (OTP) memory. This section shows the recommended OTP configuration/value settings (see Table 11) for Example 1 (see section 1.1) and Example 3 (see section 1.3). For more information about the device, see the RAA271084 datasheet.

Table 11. OTP Configuration for Example 1 and Example 3

Address	Register Name	OTP Value Example 1	OTP Value Example3
0x10	OPT_SEQ_CTRL	0x00	0x00
0x11	OPT_SLOT_TIME	0x00	0x00
0x12	OPT_SLOT_DCDC	0x00	0x00
0x13	OPT_SLOT_LDO	0x00	0x00
0x14	OPT_HP	0x00	0x00
0x15	OPT_DS	0x00	0x32
0x16	OPT_TOFF_TIME	0x00	0x00
0x30	OPT_ERRB_CTRL	0x00	0x00
0x31	OPT_VMONB_CTRL	0x00	0x00
0x82	OPT_WDT_CONFIG1	0x00	0x00
0x120	OPT_FLT_RESP1	0x00	0x00
0x121	OPT_FLT_RESP2	0x00	0x00
0x122	OPT_FLT_RESP3	0x00	0x00
0x123	OPT_FLT_RESP4	0x00	0x00

Address	Register Name	OTP Value Example 1	OTP Value Example3
0x124	OPT_FLT_RESP5	0x00	0x00
0x125	OPT_FLT_RESP6	0x00	0x00
0x126	OPT_FLT_RESP7	0x00	0x00
0x127	OPT_FLT_RESP8	0x00	0x00
0x128	OPT_FLT_SHDN1	0x00	0x00
0x129	OPT_FLT_SHDN2	0x00	0x00
0x140	OPT_INTB_MASK1	0x00	0x00
0x141	OPT_INTB_MASK2	0x00	0x00
0x142	OPT_INTB_MASK3	0x00	0x00
0x143	OPT_INTB_MASK4	0x00	0x00
0x148	OPT_SSPB_MASK1	0x00	0x00
0x149	OPT_SSPB_MASK2	0x00	0x00
0x14A	OPT_SSPB_MASK3	0x00	0x00
0x14D	OPT_SSPB_MASK5	0x00	0x00
0x150	OPT_VOUT	0x2C	0x38
0x151	OPT_FB1_THRESH	0x00	0x00
0x152	OPT_FB2_THRESH	0x00	0x00
0x153	OPT_LDO1_THRESH	0x00	0x00
0x154	OPT_LDO2_THRESH	0x00	0x00
0x155	OPT_LDO3_THRESH	0x00	0x00
0x156	OPT_LDO4_THRESH	0x00	0x00
0x157	OPT_COREMON_THRESH	0x00	0x00
0x158	OPT_LDO0_THRESH	0x00	0x00
0x160	OPT_FAULT_DLY1	0x00	0x00
0x161	OPT_FAULT_DLY2	0x00	0x00
0x162	OPT_FAULT_DLY3	0x00	0x00
0x163	OPT_FAULT_DLY4	0x00	0x00
0x164	OPT_FAULT_DLY5	0x00	0x00
0x200	OPT_DEV_MODE1	0x30	0x00
0x201	OPT_DEV_MODE2	0x10	0x10
0x202	OPT_DEV_MODE3	0x00	0x00
0x203	SEL_DEV_MODE1	0x11	0x00

Address	Register Name	OTP Value Example 1	OTP Value Example3
0x204	OPT_WAIT_DISCHG1	0x00	0x00
0x205	OPT_WAIT_DISCHG2	0x00	0x00
0x206	OPT_PD_CTRL	0x00	0x00
0x207	OPT_STATE_CTRL	0x00	0x00
0x208	OPT_SS	0x00	0x00
0x209	OPT_WDENB_CTRL	0x00	0x00
0x20B	OPT_PG_CTRL	0x00	0x00
0x20C	OPT_AMUX_BUF_OFFSET	0x00	0x00
0x20D	OPT_CALIB_OSC32K	0x00	0x00
0x20E	OPT_VDDIO	0x01	0x02
0x3C1	OTP ID1	-	-
0x3D0	OTP ID2	-	-

6. References

[1] RAA271084 Datasheet

[2] RH850/U2B Group User’s Manual: Hardware (r01uh0923ej0100_rh850u2b.pdf)

Note: Unless otherwise indicated, the references listed above are the latest published version.

7. Revision History

Revision	Date	Description
1.01	May 28, 2025	Updated Figures 1 to 4. Updated Tables 2, 4, 6, and 8.
1.00	Oct 16, 2024	Initial release.

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