RAA306012
Smart Gate Driver

R18AN0067EJ0100
Rev.1.00
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The RAA306012 is a smart gate driver IC for 3-phase brushless DC (BLDC) motor applications.

Index

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Chapter 1 Overview

This device includes three half-bridge gate drivers, a buck switching regulator and a charge pump for the gate drive voltage, two LDOs for the internal analog and logic circuitry and MCU, three accurate differential amplifiers, a BEMF sense amplifier, three general purpose comparators, and extensive protection functions.
The three half-bridge gate drivers are capable of driving up to three N-channel MOSFET bridges and support bridge voltages from 6V to 65V. Each gate driver supports up to 0.64A source and 1.28A sink peak drive current with adjustable drive strength control. The driver control input supports both 3-phase HI/LI mode and 3-phase PWM mode. Adaptive and adjustable dead-times are implemented to ensure robustness and flexibility. The active gate holding mechanism prevents miller effect induced cross-conduction and further enhances robustness.
The device also features a low-power sleep mode that consumes only 28µA to maximize battery life in portable applications. Three accurate differential amplifiers with adjustable gain support ground-side shunt current sensing for each bridge. The device can also support both BLDC sensor/sensor-less motor drive by the three general purpose comparators or a BEMF sense amplifier.
The device can be configured to use SPI interface. All the parameters can be set through the SPI interface and allows better monitoring.
The protection functions include supply voltage OV/UV protection, buck regulator OV/UV/OC protection, charge pump UV protection, MOSFET VDS OC protection, current sense OC protection, MOSFET VGS fault, thermal warning, and thermal shutdown. Fault conditions are reported on the nFAULT signal and each status bit in the Fault Status registers.

To control the smart gate driver effectively, it is important to configure not only the control signals from the MCU, but also the peripheral circuits and register settings according to the application.
For detail on this device specification, refer to the ***"RAA306012 Datasheet (R18DS0037EJ)"***.

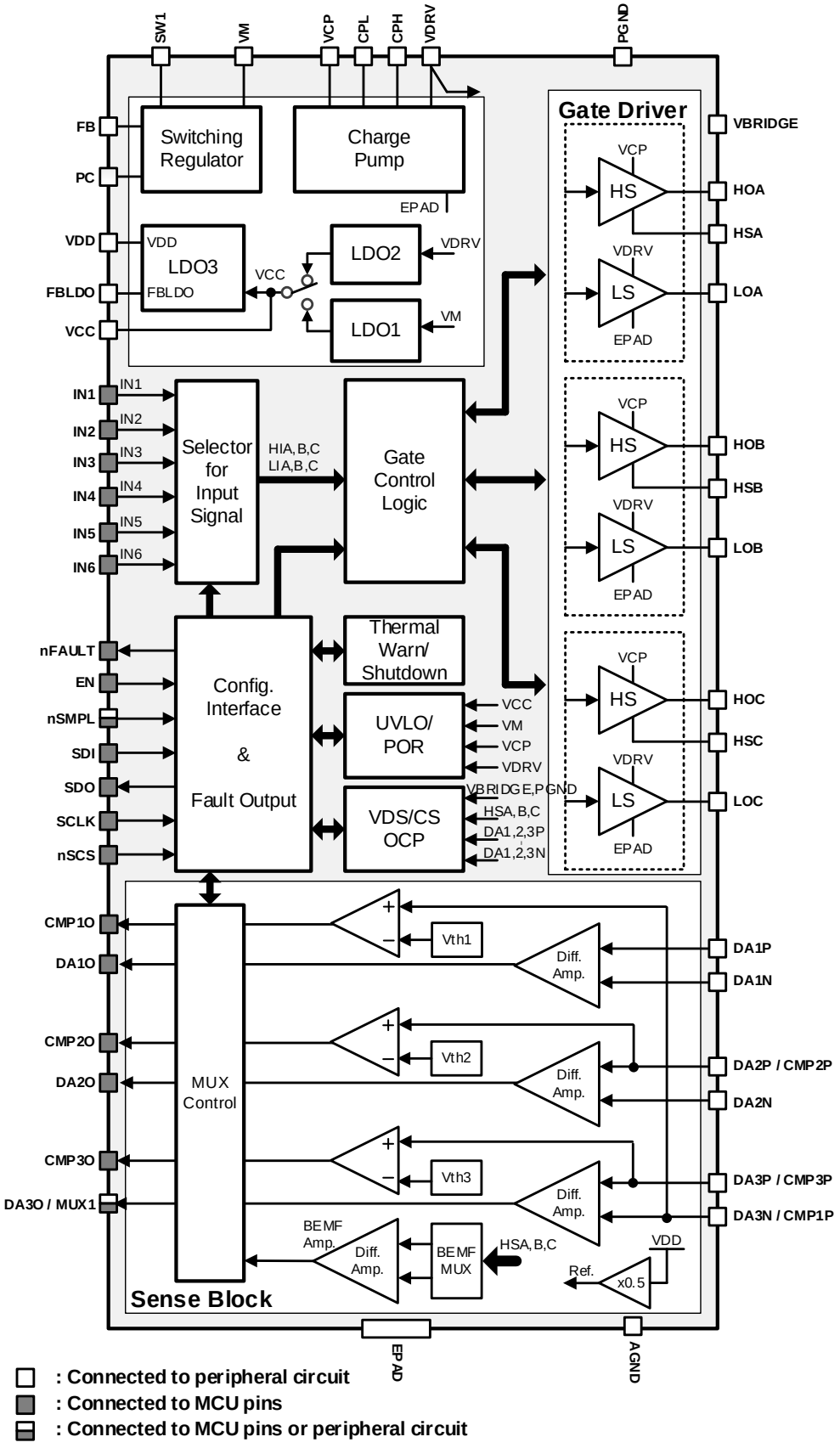


Figure 1-1 RAA306012 Internal Block Diagram

1.1 Features

Recommended operating power supply voltage conditions
- VBRIDGE: 6 to 65V (Abs. Max 78V)
- VM: 6 to 60V (Abs. Max 65V)

Ambient operating temperature range
- -40 to +125°C

3-phase gate drivers for BLDC Motors
- Switching frequency range up to 200kHz
- Peak 0.64A/1.28A source/sink current with 16 adjustable drive strength through SPI interface
- Adaptive and adjustable dead time

Flexible configuration for gate driver
- 3-phase HI/LI mode and 3-phase PWM mode
- Input control signal configuration
- Support half-bridge, full-bridge configuration

Fully integrated power supply architecture
- Two VCC LDOs allow for Sleep mode low I_Q
- 500mA buck switching regulator generates drive voltage (5V to 15V adjustable)
- 100mA adjustable output LDO for MCU supplies

Three accurate differential amplifiers (for current sensing)
- Four levels of sense gain setting (x5, x10, x20, x40)
- Supports DC offset calibration during power-up and on-the-fly

BEMF sense amplifier (for sensor-less motor drive)

3 general purpose comparators (for Hall sensor motor drive)

Extensive protection functions (fault detection functions)
- VCC undervoltage (VCC_UV)
- VM undervoltage (VM_UV)
- VM overvoltage (VM_OV)
- VCP undervoltage (VCP_UV) for charge pump
- MOSFET V_{DS} overcurrent (VDS_OCP)
- Current sense over current (CS_OCP)
- MOSFET V_{GS} fault (VGS_FAULT)
- Thermal warning (TWARN)
- Thermal shutdown (OTSD)
- Buck regulator overcurrent limiting (SR_OC1)
- Buck regulator overcurrent protection (SR_OCP)
- Buck regulator undervoltage (VDRV_UV)
- Buck regulator overvoltage (VDRV_OV)
- Fault indicator (nFAULT pin)

7mmx7mm 48 Ld QFN package (0.5mm pitch)

1.2 Applications

Power tools and Garden tools, Printers, Vacuum cleaners, Fans, Pumps, and Robotics

1.3 Pin Configurations

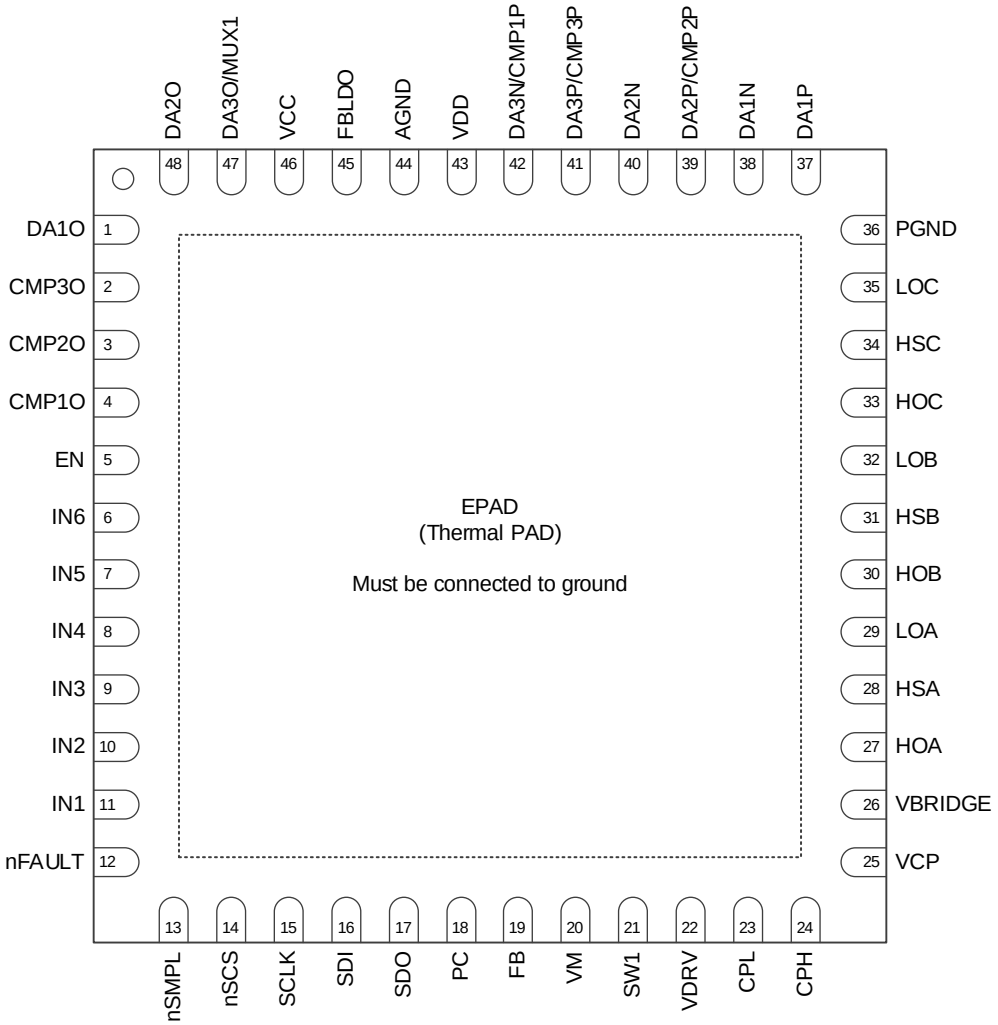


Figure 1-2 Pin Configuration Diagram (Top View)

1.4 Pin Descriptions

Table 1-1 Pin Descriptions (1/2)

Pin		I/O				Function	Note
Number	Name	level	type	Initial (EN=Low)	Enable Control		
1	DA1O	VDD	OUT	330kΩ, pull-down	DA1_EN bit	Output of differential amplifier 1 Pull-down resistor is disabled when differential amplifier 1 is enabled.	
2	CMP3O	VDD	IN/OUT	OUT/380kΩ, pull-down	CMP3_VTH / BEMF_PH bit	Control input for the detect phase selection of BEMF sense amplifier. Output of comparator 3. The pin function is selected by BEMF_PH bits.	1
3	CMP2O	VDD	IN/OUT	OUT/380kΩ, pull-down	CMP2_VTH / BEMF_PH bit	Control input for the detect phase selection of BEMF sense amplifier. Output of comparator 2. The pin function is selected by BEMF_PH bits.	1
4	CMP1O	VDD	IN/OUT	OUT/380kΩ, pull-down	CMP1_VTH / BEMF_PH bit	Control input for the detect phase selection of BEMF sense amplifier. Output of comparator 1. The pin function is selected by BEMF_PH bits.	1
5	EN	VDD	IN	100kΩ, pull-down	—	Enable control pin for Operation Mode. When this pin is logic low, the device goes to a low-power sleep mode.	1, 2
6	IN6	VDD	IN	380kΩ, pull-down	EN pin	Gate driver control input 6. The control input for each phase gate driver is selectable by the register setting.	2
7	IN5	VDD	IN	380kΩ, pull-down	EN pin	Gate driver control input 5. The control input for each phase gate driver is selectable by the register setting.	2
8	IN4	VDD	IN	380kΩ, pull-down	EN pin	Gate driver control input 4. The control input for each phase gate driver is selectable by the register setting.	2
9	IN3	VDD	IN	380kΩ, pull-down	EN pin	Gate driver control input 3. The control input for each phase gate driver is selectable by the register setting.	2
10	IN2	VDD	IN	380kΩ, pull-down	EN pin	Gate driver control input 2. The control input for each phase gate driver is selectable by the register setting.	2
11	IN1	VDD	IN	380kΩ, pull-down	EN pin	Gate driver control input 1. The control input for each phase gate driver is selectable by the register setting.	2
12	nFAULT	VDD	Open drain OUT	Hi-Z	EN pin	Fault indicator output The pull-up resistor option of MCU or external pull-up resistor is required.	3
13	nSMPL	VDD	IN	380kΩ, pull-down	DAz_SH (z = 1, 2, 3) / BEMF_SH bit	Sampling control input of BEMF sense amplifier or differential amplifiers.	
14	nSCS	VDD	IN	380kΩ, pull-up	EN pin	SPI chip select input	4
15	SCLK	VDD	IN	380kΩ, pull-down	EN pin	SPI clock input	4
16	SDI	VDD	IN	380kΩ, pull-down	EN pin	SPI data input	4
17	SDO	VDD	Open drain OUT	Hi-Z	EN pin	SPI data output The pull-up resistor option of MCU or external pull-up resistor is required.	3, 4
18	PC	VCC	OUT	1kΩ, pull-down	EN pin	gm amplifier output for phase compensation of buck switching regulator. When the switching regulator is enabled, the pull-down resistor is disabled.	
19	FB	VCC	IN	-	EN pin	Voltage feedback input of buck switching regulator (Ref = 0.8V)	
20	VM	VM	POWER	-	—	Power supply input. Connect bypass a capacitors between VM and AGND.	
21	SW1	VM	OUT	Hi-Z	EN pin	Switch node of buck switching regulator	
22	VDRV	VDRV	POWER	-	EN pin	Output of buck switching regulator, Low-side gate driver supply Connect to bypass capacitors between VDRV and AGND.	
23	CPL	VDRV	OUT	100kΩ, pull-down	EN pin	Charge pump low-side switch node. Connect a flying capacitor between CPH and CPL pins.	
24	CPH	VCP	OUT	Hi-Z	EN pin	Charge pump high-side switch node. Connect a flying capacitor between CPH and CPL pins.	

Note1: To avoid the collision by output signals of the MCU and this device, set the MCU ports to the digital input port before setting the EN pin to Low.
Note2: To avoid unexpected gate drive output, input the INz (z = 1, 2, 3, 4, 5, 6) pin to Low before setting EN pin to High or recovering from an abnormal condition. For details, refer to the smart gate driver control sequence in ***Chapter 3.***
Note3: The pull-up resistor option of MCU can be used. It is necessary to verify that the actual SPI timings meet the specifications to determine the communication speed.
Note4: SPI communication is enabled after setting the EN pin to High.

Table 1-2 Pin Descriptions (1/2)

Pin		I/O				Function	Note
Number	Name	level	type	Initial (EN=Low)	Enable Control		
25	VCP	VCP	POWER	-	EN pin	Charge pump output. Connect a bypass capacitor between VCP and VBRIDGE pins.	
26	VBRIDGE	VBRIDGE	IN	-	EN pin	Charge pump output reference and high-side MOSFET drain sense Input. Connect a bypass capacitor between VBRIDGE pin and power ground.	
27	HOA	VCP	OUT	200kΩ, pull-down to HSA	EN pin	Phase A high-side gate driver output. Connect to the high-side MOSFET gate.	5
28	HSA	VBRIDGE	IN	300kΩ, pull-down	EN pin	Phase A high-side source sense input. Connect to the high-side MOSFET source.	
29	LOA	VDRV	OUT	200kΩ, pull-down to EPAD	EN pin	Phase A low-side gate driver output. Connect to the low-side MOSFET gate.	5
30	HOB	VCP	OUT	200kΩ, pull-down to HSA	EN pin	Phase B high-side gate driver output. Connect to the high-side MOSFET gate.	5
31	HSB	VBRIDGE	IN	300kΩ, pull-down	EN pin	Phase B high-side source sense input. Connect to the high-side MOSFET source.	
32	LOB	VDRV	OUT	200kΩ, pull-down to EPAD	EN pin	Phase B low-side gate driver output. Connect to the low-side MOSFET gate.	5
33	HOC	VCP	OUT	200kΩ, pull-down to HSA	EN pin	Phase C high-side gate driver output. Connect to the high-side MOSFET gate.	5
34	HSC	VBRIDGE	IN	300kΩ, pull-down	EN pin	Phase C high-side source sense input. Connect to the high-side MOSFET source.	
35	LOC	VDRV	OUT	200kΩ, pull-down to EPAD	EN pin	Phase C low-side gate driver output. Connect to the low-side MOSFET gate.	5
36	PGND	GND	GND	-	—	Ground sense input of external power stage.	
37	DA1P	VDD	IN	-	DA1_EN / DIS_CS1OCP bit	Positive input of differential amplifier 1. When the all functions input from this pin are not used, connect to AGND.	
38	DA1N	VDD	IN	-	DA1_EN/ DIS_CS1OCP bit	Negative input of differential amplifier 1. When the all functions input from this pin are not used, connect to AGND.	
39	DA2P	VDD	IN	-	DA2_EN / DIS_CS2OCP / CMP2_VTH bit	Positive input of differential amplifier 2 and positive input of comparator 2. When the all functions input from this pin are not used, connect to AGND.	
40	DA2N	VDD	IN	-	DA2_EN / DIS_CS2OCP bit	Negative input of differential amplifier 2. When the all functions input from this pin are not used, connect to AGND.	
41	DA3P	VDD	IN	-	DA3_EN / DIS_CS3OCP / CMP3_VTH bit	Positive input of differential amplifier 3 and positive input of comparator 3. When the all functions input from this pin are not used, connect to AGND.	
42	DA3N	VDD	IN	-	DA3_EN / DIS_CS3OCP / CMP1_VTH bit	Negative input of differential amplifier 3 and positive input of comparator 1. When the all functions input from this pin are not used, connect to AGND.	
43	VDD	VDD	POWER	-	—	Internal series regulator output and power supply of output buffers. Connect to a bypass capacitor between VDD and AGND.	6
44	AGND	GND	GND	-	—	Device analog ground.	
45	FBLDO	VCC	IN	-	—	Voltage feedback input of internal series regulator (Ref.=1.2V).	
46	VCC	VCC	POWER	-	—	Internal series regulator output(5V). Connect to a bypass capacitor between VCC and AGND.	6
47	DA3O	VDD	OUT	330kΩ, pull-down	MUX bit	Output of differential amplifier 3, BEMF sense amplifier, and multiplexer. When MUX[2:0] is the setting other than 000b, the pull-down resistor is disabled.	
48	DA2O	VDD	OUT	330kΩ, pull-down	DA2_EN bit	Output of differential amplifier 2. When the differential amplifier 2 is enabled, the pull-downresistor is disabled.	
-	EPAD (Thermal PAD)	GND	GND	-	—	Power ground for gate driver and charge pump. Must be connected to power ground.	

Note5: Although pull-down resistors are integrated between the HOx - HSx (x = A, B, C) pins and between the LOx (x = A, B, C) - EPAD, external pull-down resistors are required depending on the slew rate of the external MOSFETs power supply.

Note6: The capability of VDD and VCC load current depends on the EN pin and the operation mode. For recommended operating conditions, refer to 5.3 in the ***"RAA306012 Datasheet (R18DS0037EJ)"***.

1.5 Typical Application Circuits

1.5.1 Hall Sensor Motor Drive by Using 3 Comparators

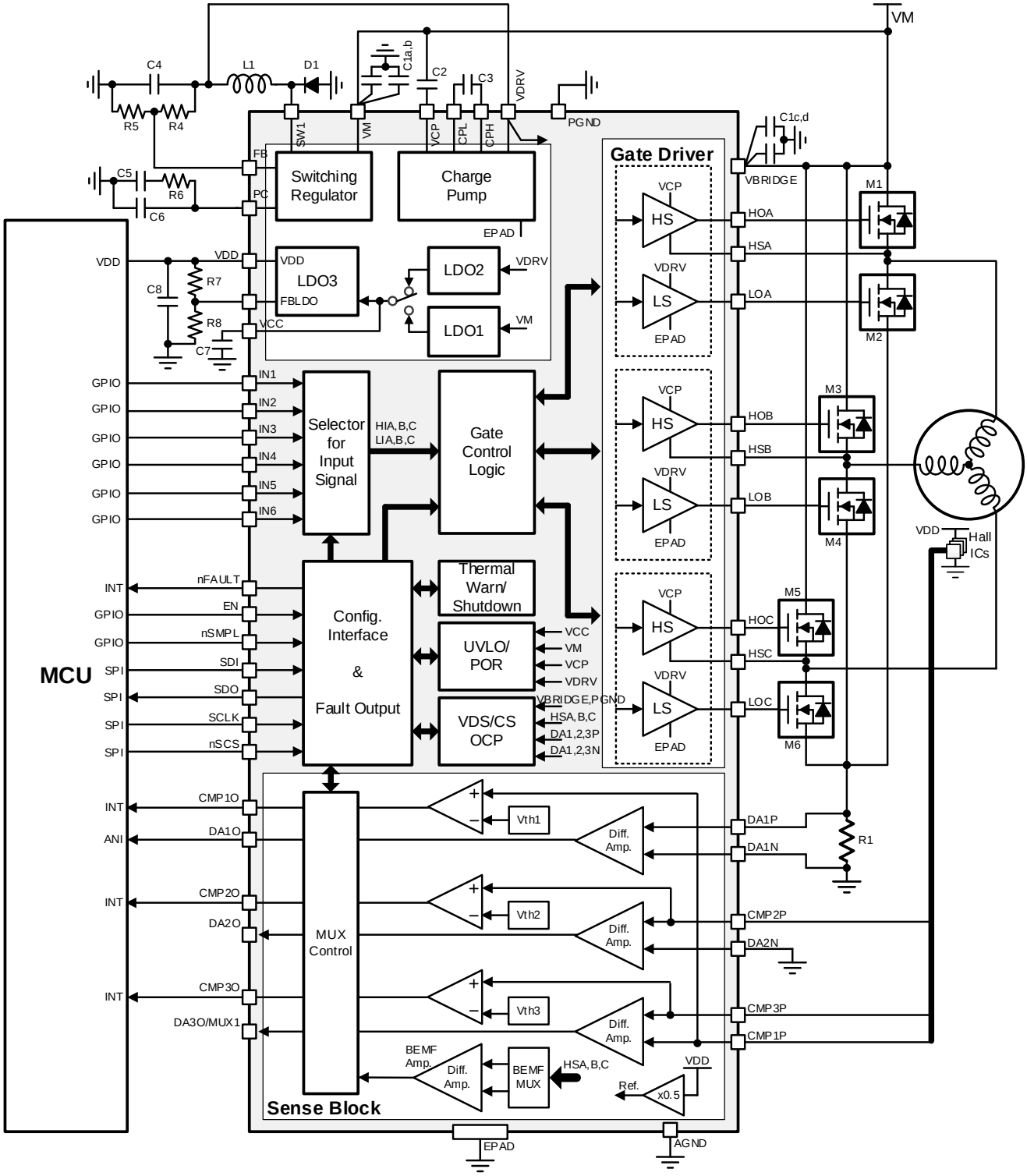


Figure 1-3 Simplified Block Diagram and Application – Hall Sensor Motor Drive by Using 3 Comparators

1.5.2 Sensor-less Motor Drive by BEMF Sensing Comparator

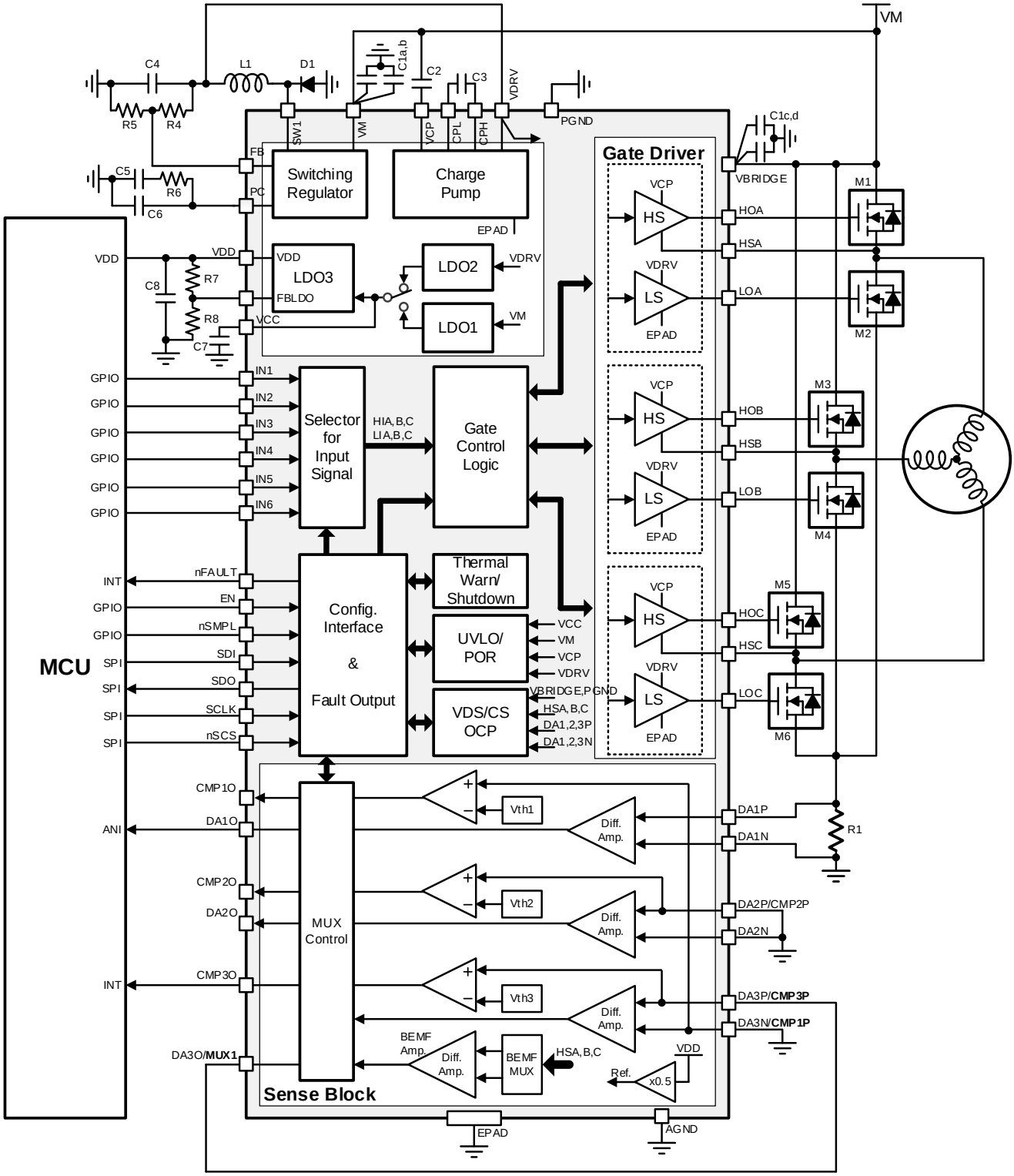


Figure 1-4 Simplified Block Diagram and Application – Sensor-less Motor Drive by BEMF Sensing Comparator

1.5.3 3 Shunt Sensor-less FOC Motor Drive

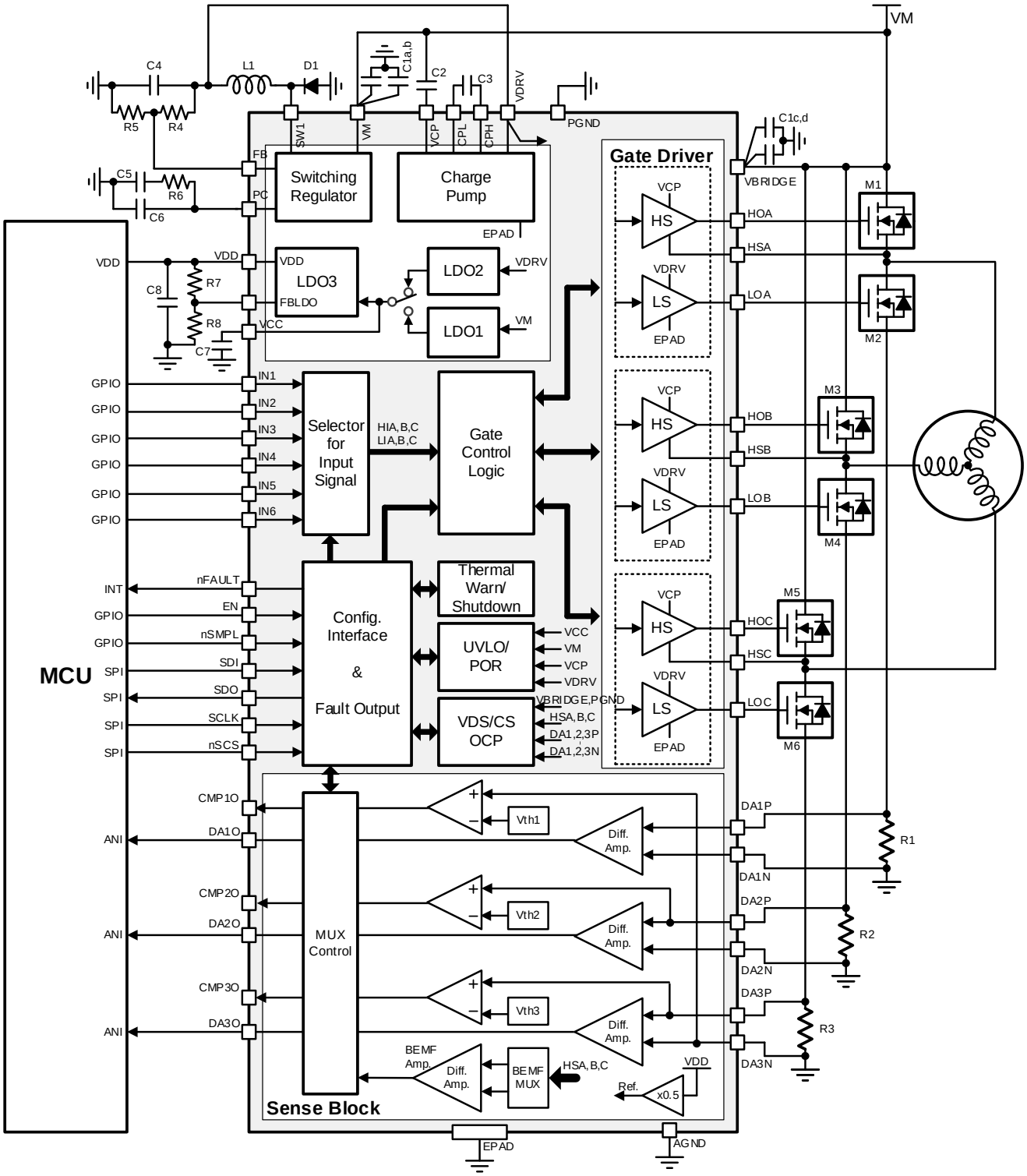


Figure 1-5 Simplified Block Diagram and Application – 3 Shunt Sensor-less FOC Motor Drive

1.5.4 3 Shunt Sensor-less FOC Motor Drive with 5V MCU Supply

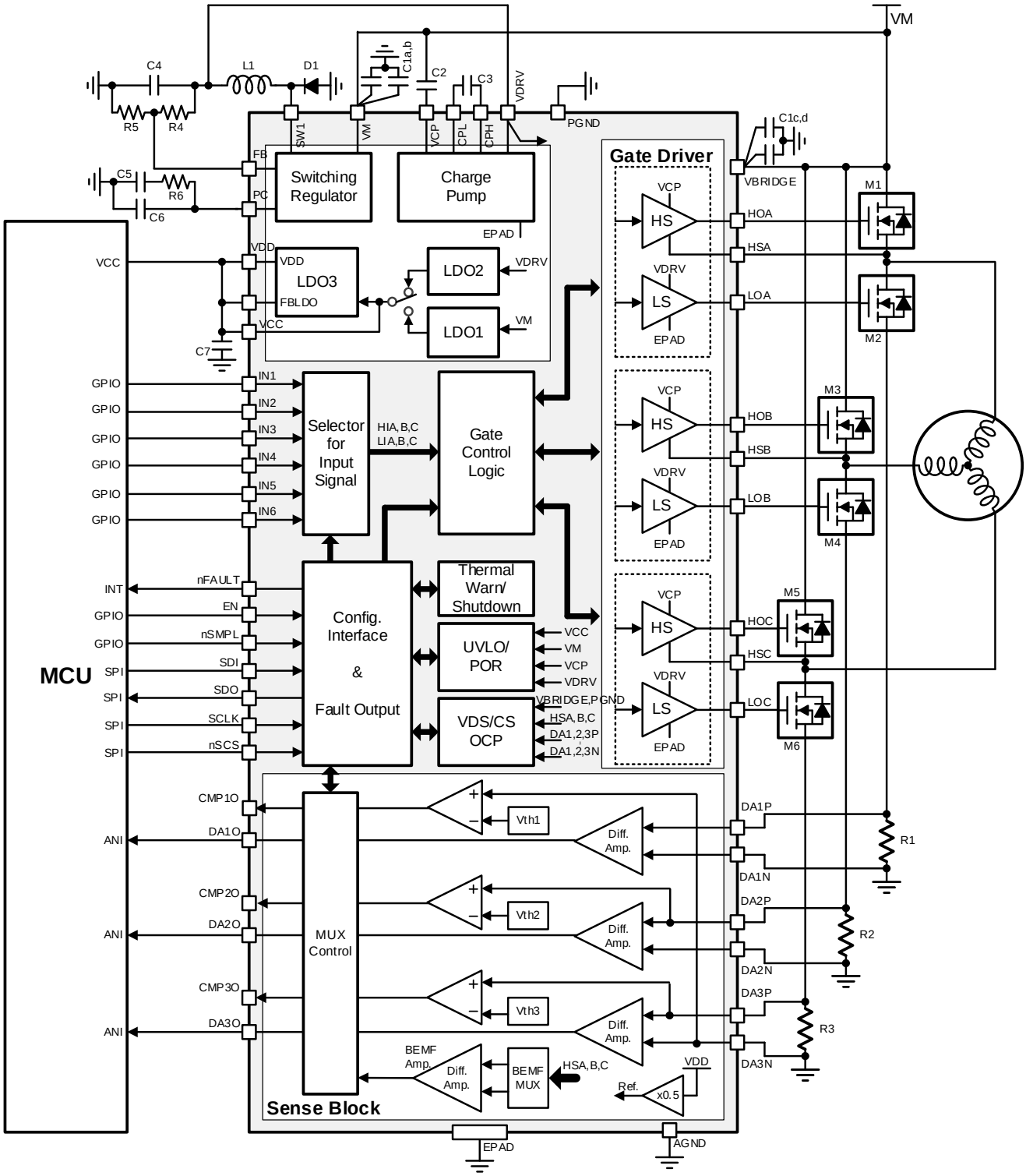


Figure 1-6 Simplified Block Diagram and Application – 3 Shunt Sensor-less FOC Motor Drive with 5V MCU Supply

Chapter 2 Pin Settings and Register Settings

2.1 Pin Settings

2.1.1 EN Pin

The EN pin is input pin of control the operation mode of the smart gate driver. Set the port (Now referred to as EN output port) of the MCU to the digital output port to control this pin. For details of the operation mode, refer to ***6.1*** of the ***"RAA306012 Datasheet (R18DS0037EJ)"***.

(1) After the MCU reset is released, the EN pin becomes Low by the smart gate driver pull-down resistor (100kΩ) even if the EN output port is an input function, Therefore, after the MCU reset is released, the operation mode of the smart gate driver is in Sleep Mode.
(2) In the MCU port settings, it is recommended to set the EN output port to the digital output function to start from Low output.
(3) When setting the EN output port to High, the smart gate driver enters the Operating Mode. It is important to set the other port settings before setting the EN output port to High because the control by signals other than the EN signal are enabled.
(4) When stopping smart gate driver operation due to any abnormality, set the EN output port to low.

2.1.2 SPI Communication Pins (Slave Side): SDO, SDI, SCLK, nSCS

The SPI communication pins are used to set smart gate driver registers and to check the fault status. SPI communication is performed by the 4-wire SPI communication function, or the 3-wire serial I/O and chip select signal with digital output function. Connect the MCU's SPI data output port to the SDI pin, the MCU's SPI data input port to the SDO pin, the MCU's SPI clock output port to the SCLK pin, and the MCU's SPI chip select output port to the nSCS pin. Since the SDO pin of the smart gate driver is an open drain output, the pull-up resistor option of MCU or external pull-up resistor is required. For SPI timing specifications and communication format of this device, refer to ***5.5*** and ***6.6*** of the ***"RAA306012 Datasheet (R18DS0037EJ)"***, and for details of control registers, refer to ***2.2***.

(1) After the MCU reset is released, the SDI and SCLK pins of the smart gate driver are driven Low by a pull-down resistor (380kΩ) each and the nSCS pin is driven High by a pull-up resistor (380kΩ) even if all SPI communication ports of MCU are input function. However, the SDO pin is Hi-Z during non-communication because it is an open-drain output. Therefore, it is necessary to enable the pull-up resistor option of MCU when not mounting the external pull-up resistor.
(2) In the MCU port settings, enable the SPI communication function of the corresponding ports. Set the communication speed (SCLK) to 5MHz or less. However, the operable communication speed depends on the wiring load on the SPI communication pins and the impedance of the pull-up resistor on the SDO pin. So, it is necessary to verify that the actual SPI timings meet the specifications to determine the communication speed.
(3) SPI communication can be performed when the EN output pin is High (Operating Mode). When the EN output port is set to Low, SPI communication is disabled. For details of SPI communication sequence for the register setting and fault status check of the smart gate driver, refer to ***Chapter 3***.

2.1.3 INz (z = 1, 2, 3, 4, 5, 6) Pins

The INz (z = 1, 2, 3, 4, 5, 6) pins are input pins to control each phase gate driver output of the smart gate driver. Connect to the MCU's PWM output ports (Now referred to as INz (z = 1, 2, 3, 4, 5, 6) output ports). The INz (z = 1, 2, 3, 4, 5, 6) pins are assigned to the gate driver control inputs HIx and LIx (x = A, B, C) according to the register settings of the smart gate driver. The gate driver outputs are controlled based on the truth table (Refer to ***6.4.2*** in the ***"RAA306012 Datasheet (R18DS0037EJ)"***) according to the polarity of HIx and LIx (x = A, B, C).

(1) After the MCU reset is released, these pins are driven Low by the pull-down resistors (380kΩ) on each INz (z = 1, 2, 3, 4, 5, 6) pin even if the EN output port is an input function,.
(2) In the MCU port settings, set to the digital output port and Low output as the setting in Sleep Mode of the smart gate driver. These port settings prevent unexpected gate driver operation when the EN output port is set to High.
(3) After the EN output port is set to High, set the Phase-A Gate Driver Input Selection Register (GDSELA), Phase-B Gate Driver Input Selection Register (GDSELB), and Phase-C Gate Driver Input Selection Register (GDSELC) to the suitable value to assign the gate driver control inputs HIx and LIx (x = A, B, and C) from INz (z = 1, 2, 3, 4, 5, 6) pins. Note that INz (z = 1, 2, 3, 4, 5, 6) output ports should be kept Low during these register settings. These port settings prevent abnormal operation caused by register setting changes.
(4) The smart gate driver register settings are reset when the EN pin goes Low. Therefore, when setting the EN output port to Low, set the INz (z = 1, 2, 3, 4, 5, 6) output ports to Low first and then set the EN output port to Low.
(5) When the nFAULT input port goes Low due to a fault detection and the gate driver is disabled, set the INz (z = 1, 2, 3, 4, 5, 6) output ports to Low. When the smart gate driver is recovered from a fault condition, the gate driver is enabled according to the fault condition. These port settings prevent unexpected gate driver operation. For the fault and recovery action of the gate driver, refer to ***6.2*** in the ***"RAA306012 Datasheet (R18DS0038EJ)"***.

2.1.4 nFAULT Pin

The nFAULT pin is output pin for the fault indicator of the smart gate driver. It is recommended to connect the MCU port (Now referred to as nFAULT input port) with an external interrupt function to this pin. It is pulled low if any of the fault conditions occur. It is pulled high when all the fault conditions are removed, and all chip power rail start-ups are done. The smart gate driver can be configured to enable or disable each fault detection by register settings. For details of the Fault Control Registers, refer to ***2.2.1.5*** and ***2.2.1.6***.

(1) After the MCU reset is released, the nFAULT input port might be a digital input function by the MCU default setting. And the nFAULT pin becomes Hi-Z by the open-drain output. Therefore, after the MCU reset is released, it is necessary to enable the pull-up resistor option of MCU.
(2) In the MCU port settings, set to the digital input port or interrupt function to confirm the fault indicator of the smart gate driver. Also, the pull-up resistor option must be enabled.
(3) At power-on, when the EN output port is Low and the nFAULT pin has pull-up resistor, the nFAULT input port goes High. The nFAULT input port switches to Low when the EN output port is set to High. The nFAULT input port goes High again if all power rail start-ups of smart gate driver have been done and all fault conditions are removed. For the control sequence considering the nFAULT behavior, refer to ***Chapter 3.***

2.1.5 DAzO (z = 1, 2, 3) Pins

DAzO (z = 1, 2, 3) pin are analog output pins for the differential amplifiers, BEMF sense amplifier, or analog multiplexer in the smart gate driver. Connect the analog input function ports of the MCU (Now referred to as DAzO (z = 1, 2, 3) input ports) to these pins.

(1) After the MCU reset is released, these ports become analog input ports by the MCU default setting, but are driven Low by the pull-down resistor (330kΩ) on the DAzO (z = 1, 2, 3) pins of the smart gate driver.
(2) In the MCU port settings, set to the analog input port for A/D conversion of the analog output signal from the smart gate driver.
(3) When the EN output port is high, the output of the DA3O pin can be changed by the analog multiplexer according to the register setting of the smart gate driver. When DA3O output is not used, set the MUX bit in the Sense Block Control 5 register (SNSCTL5) of the smart gate driver to “000b”, and the pull-down resistor (330kΩ) is enabled. For details, refer to Section ***6.5.5*** of the ***“RAA306012 Datasheet (R18DS0037EJ)”***.

2.1.6 CMPzO (z = 1, 2, 3) Pins

The CMPzO (z = 1, 2, 3) pins are used as general-purpose comparator output pins for the smart gate driver or as input pins to control the detect phase selection of the BEMF sense amplifier. When used as output pins to a general-purpose comparator, it is recommended to connect the digital input function or the external interrupt function ports of the MCU (Now referred to as CMPzO (z = 1, 2, 3) input/output ports). When used as the detect phase selection for the BEMF sense amplifier, connect the digital output ports of the MCU. The CMPzO (z = 1, 2, 3) pin functions are switched by the register settings of the smart gate driver. For details of the control register, refer to ***2.2.1.15***, and for details of the detect phase selection of the BEMF sense amplifier, refer to Section ***6.5.3*** of the ***“RAA306012 Datasheet (R18DS0037EJ)”***.

(1) After the MCU reset is released, the CMPzO (z = 1, 2, 3) input/output ports become digital input ports by the MCU default setting. The CMPzO (z = 1, 2, 3) pins are driven Low by the pull-down resistor (380kΩ) by the smart gate driver.
(2) Since the default function of the CMPzO (z = 1, 2, 3) pins of the smart gate driver is a general purpose comparator output, set to the digital input function or interrupt function for the CMPzO (z = 1, 2, 3) input/output ports.
(3) To use CMPzO (z = 1, 2, 3) pins for detect phase selection of the BEMF sense amplifier, the register settings of the smart gate driver must be set to switch the pin function of the smart gate driver to the detect phase selection input first for avoiding the collision by output signals of the MCU and smart gate driver. And after the register setting, the MCU ports used for the detect phase selection must be set to the digital output port. Note that the detect phase of the BEMF sense amplifier is selected from the two pins CMP1O/2O or CMP1O/3O. The MCU ports not used as detect phase selection can be used as input port for general purpose comparator output. In this case, set to the digital input port or interrupt function. The pin not used as detect phase selection can be used as input pin for general-purpose comparator output. In this case, set the digital input function or the external interrupt function.
(4) The register settings of the smart gate driver are reset when the EN pin goes Low. To avoid the collision by output signals of the MCU and smart gate driver caused by the reset of register settings, when setting the EN output port to Low, set CMPzO (z = 1, 2, 3) input/output ports to digital input ports first, and then set the EN output port to Low.

2.1.7 nSMPL Pin

The nSMPL pin is an input pin to control the S/H function of the differential amplifier or the BEMF sense amplifier of the smart gate driver. Connect the digital output function port of the MCU (Now referred to as nSMPL output port). For details of the S/H function, refer to ***6.5.2*** and ***6.5.3*** of the ***"RAA306012 Datasheet (R18DS0037EJ)"***.

(1) After the MCU reset is released, the nSMPL pin is driven Low by the smart gate driver pull-down resistor (380kΩ) even if the nSMPL output port is an input function.
(2) In the MCU port settings, when using the S/H function, set to the digital output function and Low output. When not using the S/H function, connect the nSMPL pin to GND.
(3) After the S/H function is enabled by the register setting of the smart gate driver, sampling operation is performed when the nSMPL pin is Low, and hold operation is performed when the nSMPL pin is High. Note that the S/H operation of the BEMF sense amplifier has a period of hold operation even when the nSMPL output pin is Low. Refer to Section ***6.5.3*** in the *"**RAA306012 Datasheet (R18DS0037EJ)**"*.

2.2 Control Register

This device has built-in Control Registers for checking fault status, enabling/disabling fault detections and function blocks, adjusting gate driver switching characteristics, setting operation mode and gain settings, etc. of sense block. SPI communication and register settings are enabled after setting the EN pin to High. However, it is recommended that the register settings of the smart gate driver be executed after the smart gate driver mode enters Operating Mode. All registers are reset when the smart gate driver mode enters Sleep Mode or Shutdown Mode, so it is necessary to set each register again after entering Operating Mode.
Figure 2-1 shows SPI communication format. ***Table 2-1*** shows the Control Register map. For the SPI communication port settings of the MCU, refer to ***2.1.2***.

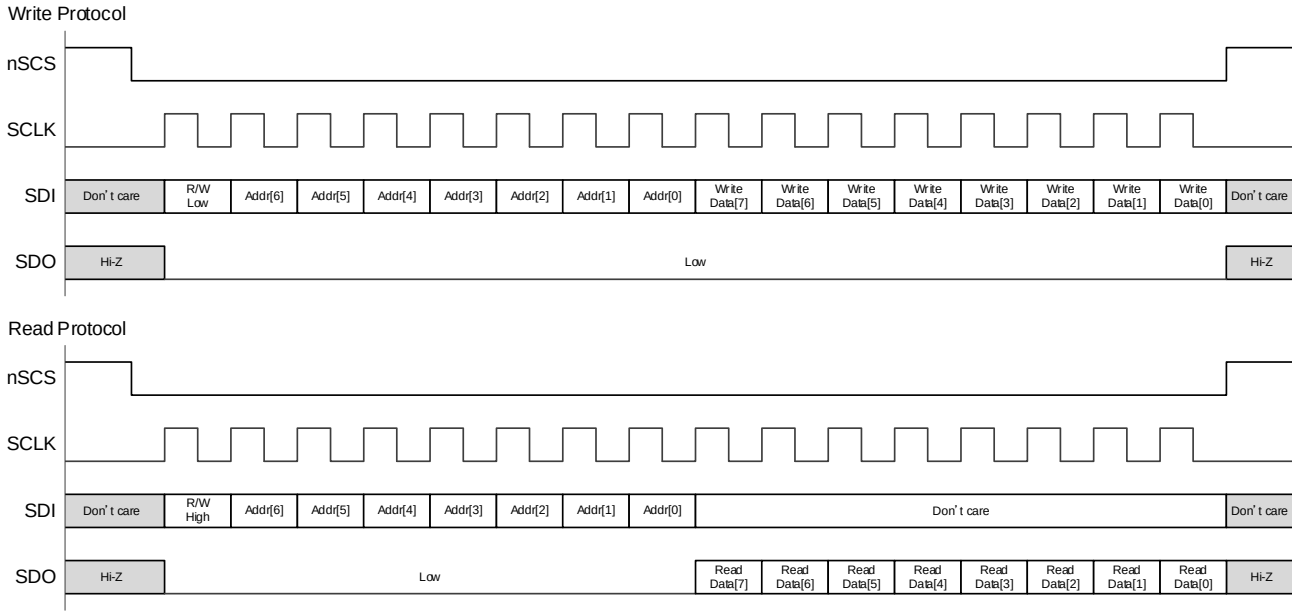


Figure 2-1 SPI Communication Format

Table 2-1 Control Register Map

Address	Register Name	Symbol	Access Type	Initial value	7	6	5	4	3	2	1	0
0x00	Fault Status 0	FLTSTS0	R	00h	FAULT	SR_FAULT	OV_UVLO	VDS_OCP	VGS_FAULT	CS_OCP	OTSD	TWARN
0x01	Fault Status 1	FLTSTS1	R	00h	VDRV_UV	VDRV_OV	SR_OCP	VCP_UV	VM_UV	VM_OV	N/A	N/A
0x02	Fault Status 2	FLTSTS2	R	00h	VDSHA_OCP	VDSLA_OCP	VGSHA_FAULT	VGSLA_FAULT	VDSHB_OCP	VDSLB_OCP	VGSHB_FAULT	VGSLB_FAULT
0x03	Fault Status 3	FLTSTS3	R	00h	VDSHC_OCP	VDSLC_OCP	VGSHC_FAULT	VGSLC_FAULT	N/A	CS1_OCP	CS2_OCP	CS3_OCP
0x04	Fault Control 1	FLTCTL1	R/W	00h	DIS_VDRVUV	DIS_VDRVOV	DIS_SROC	DIS_VCPUV	DIS_VMUV	DIS_VMOV	DIS_OTSD	TWARN_REP
0x05	Fault Control 2	FLTCTL2	R/W	07h	CSOCP_MODE1	CSOCP_MODE0	VDSOCP_MODE1	VDSOCP_MODE0	DIS_VGSFLT	DIS_CS1OCP	DIS_CS2OCP	DIS_CS3OCP
0x06	IC Control 1	ICCTL1	R/W	35h	CLR_FLT	WRITE_LOCK2	WRITE_LOCK1	WRITE_LOCK0	PWMMODE	CSOCP_TH2	CSOCP_TH1	CSOCP_TH0
0x07	IC Control 2	ICCTL2	R/W	50h	DEAD_TIME1	DEAD_TIME0	T_GT1	T_GT0	BEMF_EN	DA1_EN	DA2_EN	DA3_EN
0x08	Gate Driver Control	GDCTL	R/W	FFh	ISRC_HS3	ISRC_HS2	ISRC_HS1	ISRC_HS0	ISRC_LS3	ISRC_LS2	ISRC_LS1	ISRC_LS0
0x09	Over Current Protection Control	OCPCTL	R/W	00h	VDS_TH3	VDS_TH2	VDS_TH1	VDS_TH0	TRETRY_CSOCP	TRETRY_VDSOCP	DEG_TIME1	DEG_TIME0
0x0A	Phase-A Gate Driver Input Selection	GDSELA	R/W	14h	CMP1_HYS	HOA_SEL2	HOA_SEL1	HOA_SEL0	VMUV_TH	LOA_SEL2	LOA_SEL1	LOA_SEL0
0x0B	Phase-B Gate Driver Input Selection	GDSELB	R/W	25h	CMP2_HYS	HOB_SEL2	HOB_SEL1	HOB_SEL0	PDMODE	LOB_SEL2	LOB_SEL1	LOB_SEL0
0x0C	Phase-C Gate Driver Input Selection	GDSELC	R/W	36h	CMP3_HYS	HOC_SEL2	HOC_SEL1	HOC_SEL0	CPUV_TH	LOC_SEL2	LOC_SEL1	LOC_SEL0
0x0D	Sense Block Control 1	SNSCTL1	R/W	AAh	BEMF_GAIN1	BEMF_GAIN0	DA1_GAIN1	DA1_GAIN0	DA2_GAIN1	DA2_GAIN0	DA3_GAIN1	DA3_GAIN0
0x0E	Sense Block Control 2	SNSCTL2	R/W	00h	CAL_BCONN	BEMF_PH2	BEMF_PH1	BEMF_PH0	BEMF_SH	DA1_SH	DA2_SH	DA3_SH
0x0F	Sense Block Control 3	SNSCTL3	R/W	88h	CMP1_VTH3	CMP1_VTH2	CMP1_VTH1	CMP1_VTH0	CMP2_VTH3	CMP2_VTH2	CMP2_VTH1	CMP2_VTH0
0x10	Sense Block Control 4	SNSCTL4	R/W	80h	CMP3_VTH3	CMP3_VTH2	CMP3_VTH1	CMP3_VTH0	CAL_CONN	CAL_DA1	CAL_DA2	CAL_DA3/BEMF
0x11	Sense Block Control 5	SNSCTL5	R/W	00h	DIS_SADT	RESERVED11_6	CTL6_UNLOCK	RESERVED11_4	RESERVED11_3	MUX2	MUX1	MUX0
0x12	Sense Block Control 6	SNSCTL6	R/W	40h	RESERVED12_7	BEMF_OFFSET	RESERVED12_5	RESERVED12_4	RESERVED12_3	RESERVED12_2	RESERVED12_1	GD_AOR

2.2.1 Register Description

2.2.1.1 Fault Status 0 Register: FLTSTS0 (Address = 0x00) [Default = 0x00]

Table 2-2 and ***Table 2-3*** show the details of Fault Status 0 register.

Table 2-2 Fault Status 0 Register FLTSTS0

7	6	5	4	3	2	1	0
FAULT	SR_FAULT	OV_UVLO	VDS_OCP	VGS_FAULT	CS_OCP	OTSD	TWARN
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 2-3 Fault Status 0 Register FLTSTS0 Description [1]

Bit	Field	Type	Default	Description
7	FAULT	R	0b	Logic OR of all Fault Status bits
6	SR_FAULT	R	0b	Logic OR of the Fault Status bits for buck switching regulator: VDRV_UV, VDRV_OV, SR_OCP
5	OV_UVLO	R	0b	Logic OR of the Fault Status bits for undervoltage and overvoltage: VCP_UV, VM_UV, VM_OV
4	VDS_OCP	R	0b	Logic OR of the Fault Status bits for V_{DS} overcurrent: VDSHx_OCP, VDSLx_OCP
3	VGS_FAULT	R	0b	Logic OR of the Fault Status bits for V_{GS} fault : VGSHx_FAULT, VGSLx_FAULT
2	CS_OCP	R	0b	Logic OR of the Fault Status bits for current sense overcurrent: CS1_OCP, CS2_OCP, CS3_OCP
1	OTSD	R	0b	Indicator of thermal shutdown
0	TWARN	R	0b	Indicator of thermal warning

Note1: Fault Status registers are reset by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

2.2.1.2 Fault Status 1 Register: FLTSTS1 (Address = 0x01) [Default = 0x00]

Table 2-4 and ***Table 2-5*** show the details of Fault Status 1 register.

Table 2-4 Fault Status 1 Register FLTSTS1

7	6	5	4	3	2	1	0
VDRV_UV	VDRV_OV	SR_OCP	VCP_UV	VM_UV	VM_OV	N/A	N/A
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 2-5 Fault Status 1 Register FLTSTS1 Description [1]

Bit	Field	Type	Default	Description
7	VDRV_UV	R	0b	Indicator of VDRV undervoltage (V_{DRVUV})
6	VDRV_OV	R	0b	Indicator of VDRV overvoltage (V_{DRVOV})
5	SR_OCP	R	0b	Indicator of buck switching regulator overcurrent (I_{OC2_SR})
4	VCP_UV	R	0b	Indicator of VCP undervoltage (V_{CPUV})
3	VM_UV	R	0b	Indicator of VM undervoltage (V_{VMUV})
2	VM_OV	R	0b	Indicator of VM overvoltage (V_{VMOV})
1	N/A	R	0b	Not assigned
0	N/A	R	0b	Not assigned

Note1: Fault Status registers are reset by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

2.2.1.3 Fault Status 2 Register: FLTSTS2 (Address = 0x02) [Default = 0x00]

Table 2-6 and ***Table 2-7*** show the details of Fault Status 2 register.

Table 2-6 Fault Status 2 Register FLTSTS2

7	6	5	4	3	2	1	0
VDSHA_OCP	VDSLA_OCP	VGSHA_FAULT	VGSLA_FAULT	VDSHB_OCP	VDSLB_OCP	VGSHB_FAULT	VGSLB_FAULT
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 2-7 Fault Status 2 Register FLTSTS2 Description [1]

Bit	Field	Type	Default	Description
7	VDSHA_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-A high-side MOSFET
6	VDSLA_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-A low-side MOSFET
5	VGSHA_FAULT	R	0b	Indicator of V_{GS} fault on Phase-A high-side MOSFET
4	VGSLA_FAULT	R	0b	Indicator of V_{GS} fault on Phase-A low-side MOSFET
3	VDSHB_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-B high-side MOSFET
2	VDSLB_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-B low-side MOSFET
1	VGSHB_FAULT	R	0b	Indicator of V_{GS} fault on Phase-B high-side MOSFET
0	VGSLB_FAULT	R	0b	Indicator of V_{GS} fault on Phase-B low-side MOSFET

Note1: Fault Status registers are reset by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

2.2.1.4 Fault Status 3 Register: FLTSTS3 (Address = 0x03) [Default = 0x00]

Table 2-8 and ***Table 2-9*** show the details of Fault Status 3 register.

Table 2-8 Fault Status 3 Register FLTSTS3

7	6	5	4	3	2	1	0
VDSHC_OCP	VDSLC_OCP	VGSHC_FAULT	VGSLC_FAULT	N/A	CS1_OCP	CS2_OCP	CS3_OCP
R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b	R: 0b

Table 2-9 Fault Status 3 Register FLTSTS3 Description [1]

Bit	Field	Type	Default	Description
7	VDSHC_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-C high-side MOSFET
6	VDSLC_OCP	R	0b	Indicator of V_{DS} overcurrent on Phase-C low-side MOSFET
5	VGSHC_FAULT	R	0b	Indicator of V_{GS} fault on Phase-C high-side MOSFET
4	VGSLC_FAULT	R	0b	Indicator of V_{GS} fault on Phase-C low-side MOSFET
3	N/A	R	0b	Not assigned
2	CS1_OCP	R	0b	Indicator of current sense overcurrent by DA1P, DA1N inputs
1	CS2_OCP	R	0b	Indicator of current sense overcurrent by DA2P, DA2N inputs
0	CS3_OCP	R	0b	Indicator of current sense overcurrent by DA3P, DA3N inputs

Note1: Fault Status registers are reset by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

2.2.1.5 Fault Control 1 Register: FLTCTL1 (Address = 0x04) [Default = 0x00]

Table 2-10 and ***Table 2-11*** show the details of Fault Control 1 register.

Table 2-10 Fault Control 1 Register FLTCTL1

7	6	5	4	3	2	1	0
DIS_VDRVUV	DIS_VDRVOV	DIS_SROC	DIS_VCPUV	DIS_VMUV	DIS_VMOV	DIS_OTSD	TWARN_REP
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 2-11 Fault Control 1 Register FLTCTL1 Description

Bit	Field	Type	Default	Description
7	DIS_VDRVUV	R/W	0b	Write 1b to report status only for VDRV undervoltage (V_{DRVUV}) detection
6	DIS_VDRVOV	R/W	0b	Write 1b to report status only for VDRV overvoltage (V_{DRVOV}) detection
5	DIS_SROC	R/W	0b	Write 1b to report status only for buck switching regulator overcurrent (I_{OC2_SR}) protection
4	DIS_VCPUV	R/W	0b	Write 1b to report status only for VCP undervoltage (V_{CPUV}) detection
3	DIS_VMUV	R/W	0b	Write 1b to report status only for VM undervoltage (V_{VMUV}) detection
2	DIS_VMOV	R/W	0b	Write 1b to report status only for VM overvoltage fault (V_{VMOV}) detection
1	DIS_OTSD	R/W	0b	Write 1b to report status only for thermal shutdown
0	TWARN_REP	R/W	0b	0b: Thermal warning is reported on only TWARN bit. 1b: Thermal warning is reported on nFAULT pin, FAULT bit and TWARN bit.

2.2.1.6 Fault Control 2 Register: FLTCTL2 (Address = 0x05) [Default = 0x07]

Table 2-12 and ***Table 2-13*** show the details of Fault Control 2 register.

Table 2-12 Fault Control 2 Register FLTCTL2

7	6	5	4	3	2	1	0
CSOCP_MODE1	CSOCP_MODE0	VDSOCP_MODE1	VDSOCP_MODE0	DIS_VGSFLT	DIS_CS1OCP	DIS_CS2OCP	DIS_CS3OCP
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 1b

Table 2-13 Fault Control 2 Register FLTCTL2 Description

Bit	Field	Type	Default	Description
7	CSOCP_MODE1	R/W	0b	Response mode for current sense overcurrent 00b: Latch upon current sense overcurrent [Note2] 01b: Automatic retry upon current sense overcurrent 10b: Report on nFAULT pin, FAULT, CS_OCP and CS1/2/3_OCP bits only. No action takes place. 11b: Disable. No report and no action takes place.
6	CSOCP_MODE0	R/W	0b	
5	VDSOCP_MODE1	R/W	0b	Response mode for V_{DS} overcurrent 00b: Latch upon V_{DS} overcurrent [Note2] 01b: Automatic retry upon V_{DS} overcurrent 10b: Report on nFAULT pin, FAULT, VDS_OCP, VDSHx_OCP and VDSLx_OCP bits only. No action takes place. 11b: Disable, No report and no action takes place
4	VDSOCP_MODE0	R/W	0b	
3	DIS_VGSFLT	R/W	0b	Write 1b to disable V_{GS} fault detection
2	DIS_CS1OCP	R/W	1b	Write 1b to disable current sense overcurrent by DA1P, DA1N inputs
1	DIS_CS2OCP	R/W	1b	Write 1b to disable current sense overcurrent by DA2P, DA2N inputs
0	DIS_CS3OCP	R/W	1b	Write 1b to disable current sense overcurrent by DA3P, DA3N inputs

Note2: Latch is recovered by writing 1b to CLR_FLT of ICCTL1 register, or recovery low pulse (> tsleep: 0.85ms) on EN pin.

2.2.1.7 IC Control 1 Register: ICCTL1 (Address = 0x06) [Default = 0x35]

Table 2-14 and ***Table 2-15*** show the details of IC Control 1 register.

Table 2-14 IC Control 1 Register ICCTL1

7	6	5	4	3	2	1	0
CLR_FLT	WRITE_LOCK2	WRITE_LOCK1	WRITE_LOCK0	PWMMODE	CSOCP_TH2	CSOCP_TH1	CSOCP_TH0
R/W: 0b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b

Table 2-15 IC Control 1 Register ICCTL1 Description

Bit	Field	Type	Default	Description
7	CLR_FLT	R/W	0b	Write 1b to clear the all flagged fault status bits. This bit is reset to 0b automatically.
6	WRITE_LOCK2	R/W	0b	Write 110b to ignore all further register write except WRITE_LOCK[2:0]. Write 011b to unlock to allow register write. Writing other values takes no effect.
5	WRITE_LOCK1	R/W	1b	
4	WRITE_LOCK0	R/W	1b	
3	PWMMODE	R/W	0b	0b: 3-Phase HI/LI mode, 1b: 3-Phase PWM mode
2	CSOCP_TH2	R/W	1b	Threshold voltage setting of current sense overcurrent by DAzP, DAzN (z=1,2,3) inputs 000b: 51mV, 001b: 105mV, 010b: 157mV, 011b: 208mV, 100b: 260mV, 101b: 516mV, 110b: 773mV, 111b: 1029mV
1	CSOCP_TH1	R/W	0b	
0	CSOCP_TH0	R/W	1b	

2.2.1.8 IC Control 2 Register: ICCTL2 (Address = 0x07) [Default = 0x50]

Table 2-16 and ***Table 2-17*** show the details of IC Control 2 register.

Table 2-16 IC Control 2 Register ICCTL2

7	6	5	4	3	2	1	0
DEAD_TIME1	DEAD_TIME0	T_GT1	T_GT0	BEMF_EN	DA1_EN	DA2_EN	DA3_EN
R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 2-17 IC Control 2 Register Description

Bit	Field	Type	Default	Description
7	DEAD_TIME1	R/W	0b	Dead time from V_{GS} voltage monitor output to start timing of another-side turn on 00b: 50ns, 01b: 100ns, 10b: 200ns, 11b: 400ns
6	DEAD_TIME0	R/W	1b	
5	T_GT1	R/W	0b	Maximum gate transition time 00b: 500ns, 01b: 1000ns, 10b: 2000ns, 11b: 4000ns
4	T_GT0	R/W	1b	
3	BEMF_EN	R/W	0b	Write 1b to enable BEMF sense amplifier.
2	DA1_EN	R/W	0b	Write 1b to enable differential amplifier 1.
1	DA2_EN	R/W	0b	Write 1b to enable differential amplifier 2.
0	DA3_EN	R/W	0b	Write 1b to enable differential amplifier 3.

2.2.1.9 Gate Drive Control Register: GDCTL (Address = 0x08) [Default = 0xFF]

Table 2-18 and ***Table 2-19*** show the details of Gate Drive Control register.

Table 2-18 Gate Control Register GDCTL

7	6	5	4	3	2	1	0
ISRC_HS3	ISRC_HS2	ISRC_HS1	ISRC_HS0	ISRC_LS3	ISRC_LS2	ISRC_LS1	ISRC_LS0
R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b	R/W: 1b

Table 2-19 Gate Control Register GDCTL Description

Bit	Field	Type	Default	Description
7	ISRC_HS3	R/W	1b	High-side gate driver output source current. Sink current is 2*(source current). 0000b: 50mA, 0001b: 60mA, 0010b: 70mA, 0011b: 80mA, 0100b: 100mA, 0101b: 120mA, 0110b: 140mA, 0111b: 160mA, 1000b: 200mA, 1001b: 240mA, 1010b: 280mA, 1011b: 320mA, 1100b: 400mA, 1101b: 480mA, 1110b: 560mA, 1111b: 640mA
6	ISRC_HS2	R/W	1b	
5	ISRC_HS1	R/W	1b	
4	ISRC_HS0	R/W	1b	
3	ISRC_LS3	R/W	1b	Low-side gate driver output source current. Sink current is 2*(source current). 0000b: 50mA, 0001b: 60mA, 0010b: 70mA, 0011b: 80mA, 0100b: 100mA, 0101b: 120mA, 0110b: 140mA, 0111b: 160mA, 1000b: 200mA, 1001b: 240mA, 1010b: 280mA, 1011b: 320mA, 1100b: 400mA, 1101b: 480mA, 1110b: 560mA, 1111b: 640mA
2	ISRC_LS2	R/W	1b	
1	ISRC_LS1	R/W	1b	
0	ISRC_LS0	R/W	1b	

2.2.1.10 Overcurrent Protection Control Register: OCPCTL (Address = 0x09) [Default = 0x00]

Table 2-20 and ***Table 2-21*** show the details of Overcurrent Protection Control register.

Table 2-20 Overcurrent Protection Control Register OCPCTL

7	6	5	4	3	2	1	0
VDS_TH3	VDS_TH2	VDS_TH1	VDS_TH0	TRETRY_CSOCP	TRETRY_VDSOCP	DEG_TIME1	DEG_TIME0
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 2-21 Overcurrent Protection Control Register OCPCTL Description

Bit	Field	Type	Default	Description
7	VDS_TH3	R/W	0b	Threshold voltage setting of V_{DS} overcurrent fault 0000b: 40mV, 0001b: 60mV, 0010b: 80mV, 0011b: 120mV, 0100b: 160mV, 0101b: 200mV, 0110b: 240mV, 0111b: 320mV, 1000b: 400mV, 1001b: 480mV, 1010b: 600mV, 1011b: 720mV, 1100b: 960mV, 1101b: 1200mV, 1110b: 1600mV, 1111b: 2000mV
6	VDS_TH2	R/W	0b	
5	VDS_TH1	R/W	0b	
4	VDS_TH0	R/W	0b	
3	TRETRY_CSOCP	R/W	0b	Retry time for current sense overcurrent fault with CSOCP_MODE=01b, 0b: 4000µs, 1b: 70µs
2	TRETRY_VDSOCP	R/W	0b	Retry time for V_{DS} overcurrent fault with VDSOCP_MODE=01b, 0b: 4000µs, 1b: 70µs
1	DEG_TIME1	R/W	0b	Deglitch time for both current sense and V_{DS} overcurrent fault 00b: 1.57µs, 01b: 2.38µs, 10b: 3.49µs, 11b: 5.73µs
0	DEG_TIME0	R/W	0b	

2.2.1.11 Phase-A Gate Driver Input Selection Register: GDSELA (Address = 0x0A) [Default = 0x14]

Table 2-22 and ***Table 2-23*** show the details of Phase-A Gate Driver Input Selection register.

Table 2-22 Phase-A Gate Driver Input Selection Register GDSELA

7	6	5	4	3	2	1	0
CMP1_HYS	HOA_SEL2	HOA_SEL1	HOA_SEL0	VMUV_TH	LOA_SEL2	LOA_SEL1	LOA_SEL0
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b

Table 2-23 Phase-A Gate Driver Input Selection Register GDSELA Description

Bit	Field	Type	Default	Description
7	CMP1_HYS	R/W	0b	Comparator 1 hysteresis setting, 0b: +/-44mV, 1b: 0mV
6	HOA_SEL2	R/W	0b	Input selection for Phase-A high-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
5	HOA_SEL1	R/W	0b	
4	HOA_SEL0	R/W	1b	
3	VMUV_TH	R/W	0b	VM under voltage threshold setting, 0b: 5.3V, 1b: 7.5V
2	LOA_SEL2	R/W	1b	Input selection for Phase-A low-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
1	LOA_SEL1	R/W	0b	
0	LOA_SEL0	R/W	0b	

Note3: When HOx_SEL or LOx_SEL bits set to 111b, the source/sink current of gate driver becomes off (Hi-Z).

2.2.1.12 Phase-B Gate Driver Input Selection Register: GDSELB (Address = 0x0B) [Default = 0x25]

Table 2-24 and ***Table 2-25*** show the details of Phase-B Gate Driver Input Selection register.

Table 2-24 Phase-B Gate Driver Input Selection Register GDSELB

7	6	5	4	3	2	1	0
CMP2_HYS	HOB_SEL2	HOB_SEL1	HOB_SEL0	PDMODE	LOB_SEL2	LOB_SEL1	LOB_SEL0
R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b

Table 2-25 Phase-B Gate Driver Input Selection Register GDSELB Description

Bit	Field	Type	Default	Description
7	CMP2_HYS	R/W	0b	Comparator 2 hysteresis setting, 0b: +/-44mV, 1b: 0mV
6	HOB_SEL2	R/W	0b	Input selection for Phase-B high-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
5	HOB_SEL1	R/W	1b	
4	HOB_SEL0	R/W	0b	
3	PDMODE	R/W	0b	Gate driver pulldown mode after VDS_OCP, CS_OCP, 0b: Hi-Z pulldown, 1b: driver output low
2	LOB_SEL2	R/W	1b	Input selection for Phase-B low-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
1	LOB_SEL1	R/W	0b	
0	LOB_SEL0	R/W	1b	

Note3: When HOx_SEL or LOx_SEL bits set to 111b, the source/sink current of gate driver becomes off (Hi-Z).

2.2.1.13 Phase-C Gate Driver Input Selection Register: GDSELC (Address = 0x0Ch) [Default = 0x36]

Table 2-26 and ***Table 2-27*** show the details of Phase-C Gate Driver Input Selection register.

Table 2-26 Phase-C Gate Driver Input Selection Register GDSELC

7	6	5	4	3	2	1	0
CMP3_HYS	HOC_SEL2	HOC_SEL1	HOC_SEL0	CPUV_TH	LOC_SEL2	LOC_SEL1	LOC_SEL0
R/W: 0b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 1b	R/W: 0b

Table 2-27 Phase-C Gate Driver Input Selection Register GDSELC Description

Bit	Field	Type	Default	Description
7	CMP3_HYS	R/W	0b	Comparator 3 hysteresis setting, 0b: +/-44mV, 1b: 0mV
6	HOC_SEL2	R/W	0b	Input selection for Phase-C high-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
5	HOC_SEL1	R/W	1b	
4	HOC_SEL0	R/W	1b	
3	CPUV_TH	R/W	0b	VCP under voltage threshold setting, 0b: 0.58*VDRV, 1b: 0.8*VDRV
2	LOC_SEL2	R/W	1b	Input selection for Phase-C low-side gate driver Note3 000b: Low fix, 001b: IN1, 010b: IN2, 011b: IN3, 100b: IN4, 101b: IN5, 110b: IN6, 111b: Hi-Z
1	LOC_SEL1	R/W	1b	
0	LOC_SEL0	R/W	0b	

Note3: When HOx_SEL or LOx_SEL bits set to 111b, the source/sink current of gate driver becomes off (Hi-Z).

2.2.1.14 Sense Block Control 1 Register: SNSCTL1 (Address = 0x0D) [Default = 0xAA]

Table 2-28 and ***Table 2-29*** show the details of Sense Block Control 1 register.

Table 2-28 Sense Block Control 1 Register SNSCTL1

7	6	5	4	3	2	1	0
BEMF_GAIN1	BEMF_GAIN0	DA1_GAIN1	DA1_GAIN0	DA2_GAIN1	DA2_GAIN0	DA3_GAIN1	DA3_GAIN0
R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 1b	R/W: 0b

Table 2-29 Sense Block Control 1 Register SNSCTL1 Description

Bit	Field	Type	Default	Description
7	BEMF_GAIN1	R/W	1b	Gain setting of BEMF sense amplifier with DA3_GAIN=00b 00b: 0.05V/V, 01b: 0.1V/V, 10b: 0.5V/V, 11b: 1.0V/V
6	BEMF_GAIN0	R/W	0b	
5	DA1_GAIN1	R/W	1b	Gain setting of differential amplifier 1 00b: 5V/V, 01b: 10V/V, 10b: 20V/V, 11b: 40V/V
4	DA1_GAIN0	R/W	0b	
3	DA2_GAIN1	R/W	1b	Gain setting of differential amplifier 2 00b: 5V/V, 01b: 10V/V, 10b: 20V/V, 11b: 40V/V
2	DA2_GAIN0	R/W	0b	
1	DA3_GAIN1	R/W	1b	Gain setting of differential amplifier 3 00b: 5V/V, 01b: 10V/V, 10b: 20V/V, 11b: 40V/V
0	DA3_GAIN0	R/W	0b	

2.2.1.15 Sense Block Control 2 Register: SNSCTL2 (Address = 0x0E) [Default = 0x00]

Table 2-30 and ***Table 2-31*** show the details of Sense Block Control 2 register.

Table 2-30 Sense Block Control 2 Register SNSCTL2

7	6	5	4	3	2	1	0
CAL_BCONN	BEMF_PH2	BEMF_PH1	BEMF_PH0	BEMF_SH	DA1_SH	DA2_SH	DA3_SH
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 2-31 Sense Block Control 2 Register SNSCTL2 Description

Bit	Field	Type	Default	Description
7	CAL_BCONN	R/W	0b	Input selection of BEMF sense amplifier during BEMF offset calibration 0b: The amplifier inputs are connected to the reference voltage of BEMF sense amplifier (DAREF) 1b: The amplifier inputs are connected to the phase selected by BEMF_PH bits
6	BEMF_PH2	R/W	0b	Detect phase selection of BEMF sense amplifier Note4 00xb: Select automatically from the input signals of the gate driver at every nSMPL falling edge 010b: Select by CMP1O and CMP2O pins (CMP1O, CMP2O)= (0,0): No selection, (0,1): Phase-A, (1,0): Phase-B, (1,1): Phase-C 011b: Select by CMP1O and CMP3O pins (CMP1O, CMP3O)= (0,0): No selection, (0,1): Phase-A, (1,0): Phase-B, (1,1): Phase-C 100b: No selection, 101b: Phase-A, 110b: Phase-B, 111b: Phase-C
5	BEMF_PH1	R/W	0b	
4	BEMF_PH0	R/W	0b	
3	BEMF_SH	R/W	0b	S/H control setting of BEMF sense amplifier Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Low & PWM ON after tGT
2	DA1_SH	R/W	0b	S/H control setting of differential amplifier 1 Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Low
1	DA2_SH	R/W	0b	S/H control setting of differential amplifier 2 Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Low
0	DA3_SH	R/W	0b	S/H control setting of differential amplifier 3 Note4 0b: keep sampling, 1b: sampling during nSMPL signal=Low

Note4: Refer to ***6.5.2***, ***6.5.3*** of ***"RAA306012 Datasheet (R18DS0037EJ)"***.

2.2.1.16 Sense Block Control 3 Register: SNSCTL3 (Address = 0x0F) [Default = 0x88]

Table 2-32 and ***Table 2-33*** show the details of Sense Block Control 3 register.

Table 2-32 Sense Block Control 3 Register SNSCTL3

7	6	5	4	3	2	1	0
CMP1_VTH3	CMP1_VTH2	CMP1_VTH1	CMP1_VTH0	CMP2_VTH3	CMP2_VTH2	CMP2_VTH1	CMP2_VTH0
R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b

Table 2-33 Sense Block Control 3 Register SNSCTL3 Description

Bit	Field	Type	Default	Description
7	CMP1_VTH3	R/W	1b	Threshold voltage setting of Comparator 1 0000b: Disable, 0001b to 1111b: Threshold voltage= VDD /16 x CMP1_VTH
6	CMP1_VTH2	R/W	0b	
5	CMP1_VTH1	R/W	0b	
4	CMP1_VTH0	R/W	0b	
3	CMP2_VTH3	R/W	1b	Threshold voltage setting of Comparator 2 0000b: Disable, 0001b to 1111b: Threshold voltage= VDD /16 x CMP2_VTH
2	CMP2_VTH2	R/W	0b	
1	CMP2_VTH1	R/W	0b	
0	CMP2_VTH0	R/W	0b	

2.2.1.17 Sense Block Control 4 Register: SNSCTL4 (Address = 0x10) [Default = 0x80]

Table 2-34 and ***Table 2-35*** show the details of Sense Block Control 4 register.

Table 2-34 Sense Block Control 4 Register SNSCTL4

7	6	5	4	3	2	1	0
CMP3_VTH3	CMP3_VTH2	CMP3_VTH1	CMP3_VTH0	CAL_CONN	CAL_DA1	CAL_DA2	CAL_DA3/BEMF
R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 2-35 Sense Block Control 4 Register SNSCTL4 Description

Bit	Field	Type	Default	Description
7	CMP3_VTH3	R/W	1b	Threshold voltage setting of Comparator 3 0000b: Disable, 0001b to 1111b: Threshold voltage= VDD /16 x CMP3_VTH
6	CMP3_VTH2	R/W	0b	
5	CMP3_VTH1	R/W	0b	
4	CMP3_VTH0	R/W	0b	
3	CAL_CONN	R/W	0b	Input selection of differential amplifier during DC offset calibration 0b: The amplifier inputs are connected to GND. 1b: The amplifier inputs are connected to the external shunt.
2	CAL_DA1	R/W	0b	Write 1b to enable DC offset calibration for differential amplifier 1. This bit is automatically reset to 0 after calibration is done.
1	CAL_DA2	R/W	0b	Write 1b to enable DC offset calibration for differential amplifier 2. This bit is automatically reset to 0 after calibration is done.
0	CAL_DA3/BEMF	R/W	0b	Write 1b to this bit to enable DC offset calibration for differential amplifier 3 if BEMF sensing is disabled (BEMF_EN=0b). Write 1b to this bit to enable DC offset calibration for BEMF sensing amplifiers if BEMF sensing is enabled (BEMF_EN=1b). This bit automatically resets to 0 after calibration is done

2.2.1.18 Sense Block Control 5 Register: SNSCTL5 (Address = 0x11) [Default = 0x00]

Table 2-36 and ***Table 2-37*** show the details of Sense Block Control 5 register.

Table 2-36 Sense Block Control 5 Register SNSCTL5

7	6	5	4	3	2	1	0
DIS_SADT	RESERVED11_6	CTL6_UNLOCK	RESERVED11_4	RESERVED11_3	MUX2	MUX1	MUX0
R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 2-37 Sense Block Control 5 Register SNSCTL5 Description

Bit	Field	Type	Default	Description
7	DIS_SADT	R/W	0b	Write 1b to disable the adaptive dead time control function
6	RESERVED11_6	R/W	0b	Reserved. The write value should be 0b.
5	CTL6_UNLOCK	R/W	0b	Write 0b to ignore SNSCTL6 register write. Write 1b to unlock to allow SNSCTL6 register write.
4	RESERVED11_4	R/W	0b	Reserved. The write value should be 0b.
3	RESERVED11_3	R/W	0b	Reserved. The write value should be 0b.
2	MUX2	R/W	0b	Output selection of DA3O/MUX1 pin 000b: GND (pulldown: 330kΩ) 001b: VM monitor 010b: TEMP monitor 011b: Differential amplifier reference voltage 101b: Differential amplifier 1 output 110b: Differential amplifier 2 output In case of BEMF_EN=0b, 100b: Differential amplifier 3 output w/ 10kΩ 111b: Differential amplifier 3 output w/o 10kΩ In case of BEMF_EN=1b, 100b: BEMF sense amplifier output w/ 10kΩ 111b: BEMF sense amplifier output w/o 10kΩ
1	MUX1	R/W	0b	
0	MUX0	R/W	0b	

2.2.1.19 Sense Block Control 6 Register: SNSCTL6 (Address = 0x12) [Default = 0x40h]

Table 2-38 and ***Table 2-39*** show the details of Sense Block Control 6 register. CTL6_UNLOCK=1b is necessary to allow SNSCTL6 register write. After writing SNSCTL6 register, CTL6_UNLOCK should be set to 0b.

Table 2-38 Sense Block Control 6 Register SNSCTL6

7	6	5	4	3	2	1	0
RESERVED12_7	BEMF_OFFSET	RESERVED12_5	RESERVED12_4	RESERVED12_3	RESERVED12_2	RESERVED12_1	GD_AOR
R/W: 0b	R/W: 1b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b	R/W: 0b

Table 2-39 Sense Block Control 6 Register SNSCTL6 Description

Bit	Field	Type	Default	Description
7	RESERVED12_7	R/W	0b	Reserved. The write value should be 0b.
6	BEMF_OFFSET	R/W	1b	Data selection of BEMF sense amplifier DC offset 0b: calibration data, 1b: trimming data by shipping test This bit automatically sets to 0 after DC offset calibration for BEMF sense amplifier is done.
5	RESERVED12_5	R/W	0b	Reserved. The write value should be 0b.
4	RESERVED12_4	R/W	0b	Reserved. The write value should be 0b.
3	RESERVED12_3	R/W	0b	Reserved. The write value should be 0b.
2	RESERVED12_2	R/W	0b	Reserved. The write value should be 0b.
1	RESERVED12_1	R/W	0b	Reserved. The write value should be 0b.
0	GD_AOR	R/W	0b	Write 1b to enable the active override mode of the gate driver logic.

2.3 Register Settings for Motor Control

RAA306012 incorporates various sense blocks to control BLDC motors. The optimal motor control for each application can be realized by using these function blocks. This section describes the circuit configuration and register settings for hall sensor motor drive, sensor-less motor drive, and 3 shunt sensor-less FOC motor drive as examples.

2.3.1 Hall Sensor Motor Drive by Using 3 Comparators

2.3.1.1 Circuit Diagram

Figure 2-2 shows an example of a simplified application block diagram and application for hall sensor motor drive by using 3 comparators.

In hall sensor motor drive, the motor is controlled by switching the energized phase according to the position detection signal from the hall IC. The polarity of the position detection signals can be determined by using general purpose comparators and is input to the CMPzP (z = 1, 2, 3) pins.

When detecting the motor drive current by a shunt resistor or using current sense overcurrent function (CS_OCP), input the differential voltage across the shunt resistor to the DA1P and DA1N pins. The unused pins on the DAzP and DAzN (z = 1, 2, 3) pins should be connected to AGND.

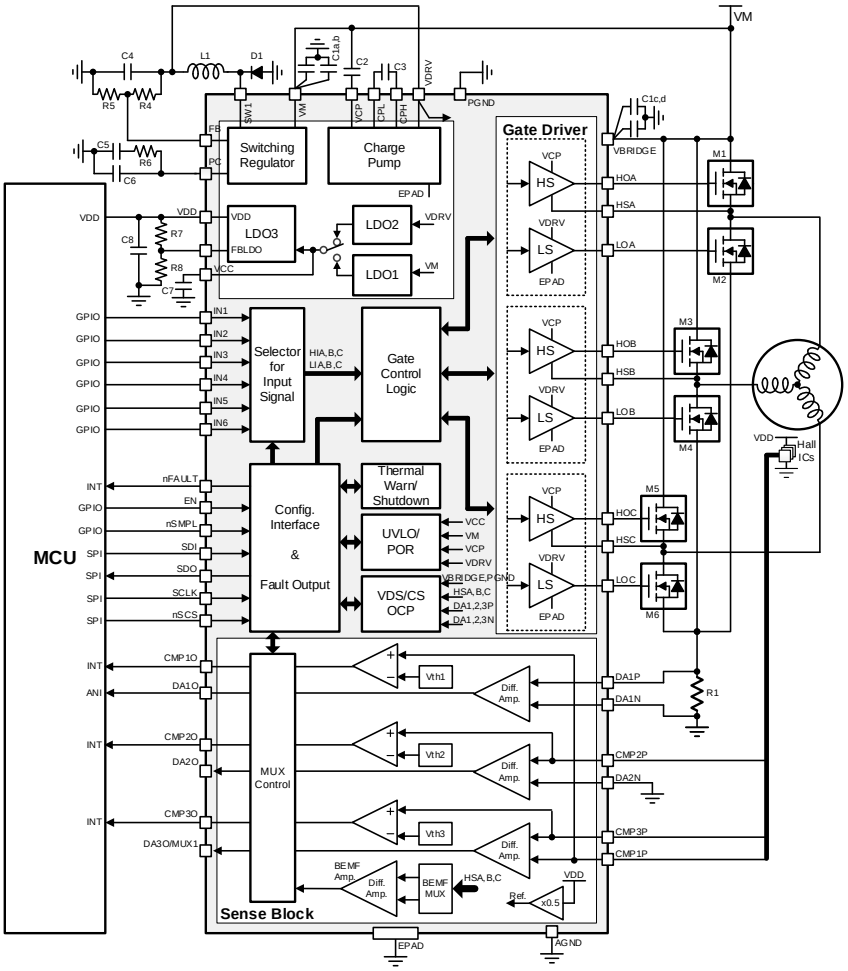


Figure 2-2 Simplified Application Block Diagram – Hall Sensor Motor Drive by Using 3 Comparators

2.3.1.2 Register Setting

This device requires register settings for various functions of the smart gate driver before motor control. The following four types of register settings are required for each function.

(a) Fault detection function: enable/disable, response mode, adjustment bits, and Fault Status clear bit
(b) Gate driver: input selection, control mode, and adjustment bits.
(c) Sense block: enable/disable, control bits, and adjustment bits
(d) Sense block calibration: enable bit

In the register settings for hall sensor motor drive by using 3 comparators, the following settings are required for the general purpose comparators and differential amplifier 1 (if used) in the sense block.

- ICCTL2 register: DA1_EN bit
- GDSELA register: CMP1_HYS bit
- GDSELB register: CMP2_HYS bit
- GDSELC register: CMP3_HYS bit
- SNSCTL1 register: DA1_GAIN bit
- SNSCTL2 register: DA1_SH bit
- SNSCTL3 register: CMP1_VTH, CMP2_VTH bits
- SNSCTL4 register: CMP3_VTH, CAL_CONN, CAL_DA1 bits

The start-up sequence of the smart gate driver is configured by dividing the register settings into three steps (Register Setting 1, 2, and 3) for the above register settings (a), (b), (c), and (d).
For the timing of register settings, refer to ***3.1***. The registers to be set in Register Setting 1, 2, and 3 are shown below.

(1) Register Setting 1:

Register Setting 1 mainly includes the registers for the fault detection function. The following register settings are executed in start-up sequence example described in ***3.1***.

- FLTCTL1 register
- FLTCTL2 register
- ICCTL1 register

The response mode and adjustment bits of the fault detection function are also partially assigned to the OCPCTL register and the GDSELx (x = A, B, C) register. If you want to change the threshold value before judging the nFAULT pin output to confirm the normal start-up, please execute these register settings with Register Setting 1. When the register settings of the fault detection function are completed, set the CLR_FLT bit to clear the Fault Status.

(2) Register Setting 2:

Register Setting 2 mainly includes the registers for the gate driver and the sense block. The following register settings are executed in start-up sequence example described in ***3.1***.

- ICCTL2 register
- GDCTL register
- OCPCTL register
- GDSELx (x = A, B, C) register
- SNSCTLz (z = 1, 2, 3, 4) register

GDSELx (x = A, B, C) registers are used to select gate driver input signals. Set to the appropriate values considering the connections with the MCU to be used.

Until these bit settings are completed, all INz (z = 1, 2, 3, 4, 5, 6) signals must be Low to avoid unexpected gate driver outputs. Also, all INz (z = 1, 2, 3, 4, 5, 6) signals must be Low before the EN pin is set to Low because all registers are reset when the EN pin is set to Low. For details, refer to the control sequence examples in ***3.1*** and ***3.2***.

The differential amplifiers also have register settings (CAL_DAz (z = 1, 2, 3) bits) to enable DC offset calibration. DC offset calibration can be performed separately for each differential amplifier, so be sure to perform the DC offset calibration corresponding to the differential amplifier used. To achieve highly accurate calibration, CAL_CONN = “1b” is recommended. With this setting, the inputs of the differential amplifier during the calibration period are the DAzP and DAzN (z = 1, 2, 3) pins, and normal calibration cannot be performed with current flowing through the shunt resistor.

(3) Register Setting 3

Register Setting 3 includes other settings of the gate driver and the sense block. The following register settings are executed in start-up sequence example described in ***3.1***.

- SNSCLT2 register
- SNSCTL5 register
- SNSCTL6 register

Although the SNSCTL2 register setting is not required for hall sensor control, the setting is provided in consideration of the versatility of the start-up sequence.

The SNSCTL6 register has a write-protection function. Since setting the CTL6_UNLOCK bit of the SNSCTL5 register is required to allow SNSCTL6 register write, set the registers according to the following procedures.

(1) Set CTL6_UNLOCK bit of SNSCTL5 register to “1b” (Release the write lock to the SNSCTL6 register)
(2) Set SNSCTL6 register to “0x41”
(3) Set CTL6_UNLOCK bit of SNSCTL5 register to “0b” (Set the write lock to SNSCTL6 register)

The BEMF_OFFSET bit and the GD_AOR bit in the SNSCTL6 register must be set to “1b”. The RESERVED bits in the SNSCTL5 and SNSCTL6 registers must be set to “0b”.

2.3.1.3 Control Method and Operating Waveforms

In hall sensor motor drive, the motor is controlled by switching the energized phase according to the position detection signal from the hall IC. The polarity of the position detection signals can be detected by using general purpose comparators in the smart gate driver and interrupt functions of MCU.

Figure 2-3 shows an operating waveform diagram for hall sensor motor drive by using 3 comparators. The polarity change of the hall IC outputs (CMPzP (z = 1, 2, 3) inputs) depend on the mounting position of the Hall sensor, so the pattern of the energized phase must be changed according to the relation between the rotor position and the polarity of the hall IC output.

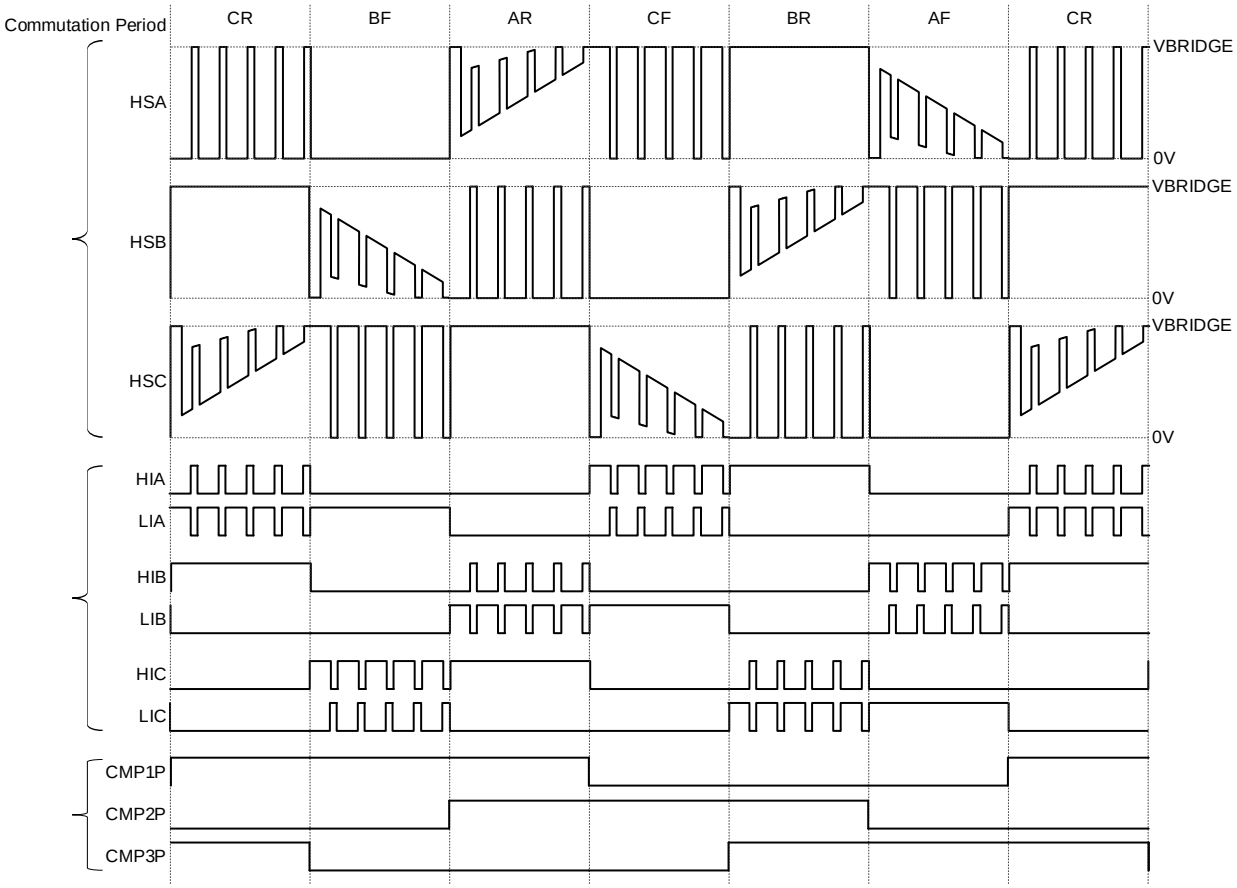


Figure 2-3 Operating Waveform Diagram – Hall Sensor Motor Drive by Using 3 Comparators

2.3.2 Sensor-less Motor Drive by BEMF Sensing Comparator

2.3.2.1 Circuit Diagram

Figure 2-4 shows an example of a simplified application block diagram and application for sensor-less motor drive by BEMF sensing comparator.

In sensor-less motor drive by BEMF sensing comparator, the motor is controlled by switching the energized phase according to the induced voltage (BEMF) generated by the motor rotation. Motor position detection is performed by detecting the BEMF zero crossing using a general-purpose comparator or an A/D converter in the MCU in addition to the BEMF sense amplifier built into the smart gate driver. When using the general-purpose comparator built into the smart gate driver as a method to detect the BEMF zero crossing, connect the DA3O/MUX1 pin to the CMP2P pin or the CMP3P pin. ***Figure 2-4*** shows an example of input to the CMP3P pin. When using the A/D converter in the MCU as a method to detect the BEMF zero crossing, connect the DA3O/MUX1 pin to the A/D converter input port. When using a comparator in the MCU, connect the DA3O/MUX1 pin to the comparator input port to be used.

When detecting the motor drive current by a shunt resistor or using current sense overcurrent function (CS_OCP), input the differential voltage across the shunt resistor to the DA1P and DA1N pins. The unused pins on the DAzP and DAzN (z = 1, 2, 3) pins should be connected to AGND.

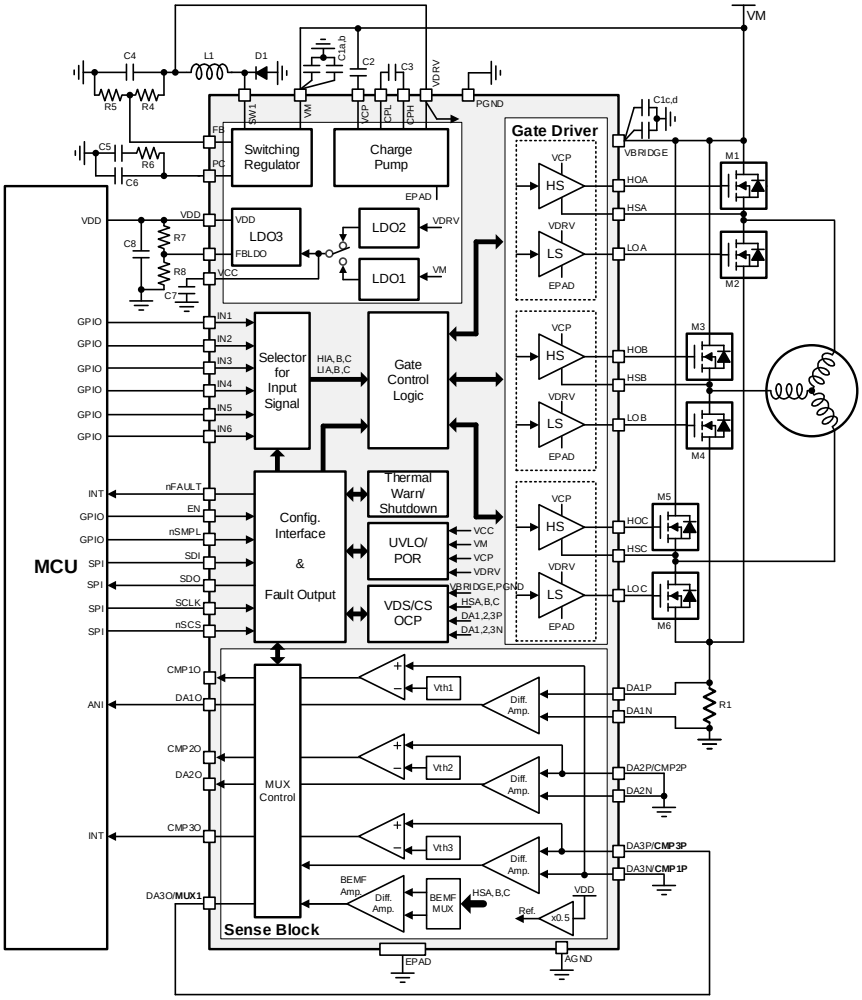


Figure 2-4 Simplified Application Block Diagram – Sensor-less Motor Drive by BEMF Sensing Comparator

2.3.2.2 Register Settings

In the register settings for sensor-less motor drive by BEMF sensing comparator, the following settings are required for the BEMF sense amplifier, general-purpose comparator, and differential amplifier 1 (if used) in the sense block.

- ICCTL2 register: BEMF_EN, DA1_EN bits
- GDSELC register: CMP3_HYS bit
- SNSCTL1 register: BEMF_GAIN, DA1_GAIN bits
- SNSCTL2 register: BEMF_PH, BEMF_SH, DA1_SH bits
- SNSCTL3 register: CMP1_VTH, CMP2_VTH bits
- SNSCTL4 register: CMP3_VTH, CAL_CONN, CAL_DA1 bits
- SNSCTL5 register: MUX bits
- SNSCTL6 register: BEMF_OFFSET bit

The start-up sequence of the smart gate driver is configured by dividing the register settings into three steps (Register Setting 1, 2, and 3) similar to the hall sensor motor drive by using 3 comparators. The similar settings and procedures are used except for the above register settings of the sense block. For details on each register, refer to ***2.3.1.2***.

For details on the BEMF sense amplifier, refer to ***6.5.3*** in the ***"RAA306012 Datasheet (R18DS0037EJ)"***. Also, for output control of the DA3O/MUX1 pin, refer to ***6.5.5*** in the ***"RAA306012 Datasheet (R18DS0037EJ)"***. The unused general-purpose comparator can be disabled by setting CMPz_VTH (z = 1, 2, 3) bits to "0000b". It is recommended to set these bits together with the DAz_EN (z = 1, 2, 3) bits to disable unused differential amplifiers to reduce power consumption.

2.3.2.3 Control Method and Operating Waveforms

In sensor-less motor drive by BEMF sensing comparator, the motor is controlled by switching the energized phase according to the BEMF zero crossing signal using a general-purpose comparator or an A/D converter in the MCU in addition to the BEMF sense amplifier built into the smart gate driver. The switching timing of the energized phase is controlled by using a timer so that the BEMF zero crossing comes in the center of the switching timing interval.

Figure 2-5 shows an operating waveform diagram for sensor-less motor drive by BEMF sensing comparator. Since BEMF can be observed in the de-energized phase, the BEMF detection phase must be selected suitably each time the energized phase is switched. The selection method of the BEMF detection phase can be selected by the BEMF_PH bits. For details, refer to **6.5.3** in the ***"RAA306012 Datasheet (R18DS0037EJ)"*.** In addition, a detection mask time must be provided to prevent zero-crossing false detection due to kickback that occurs when switching the energized phase. Set an appropriate detection mask time considering the motor speed, drive current, etc.

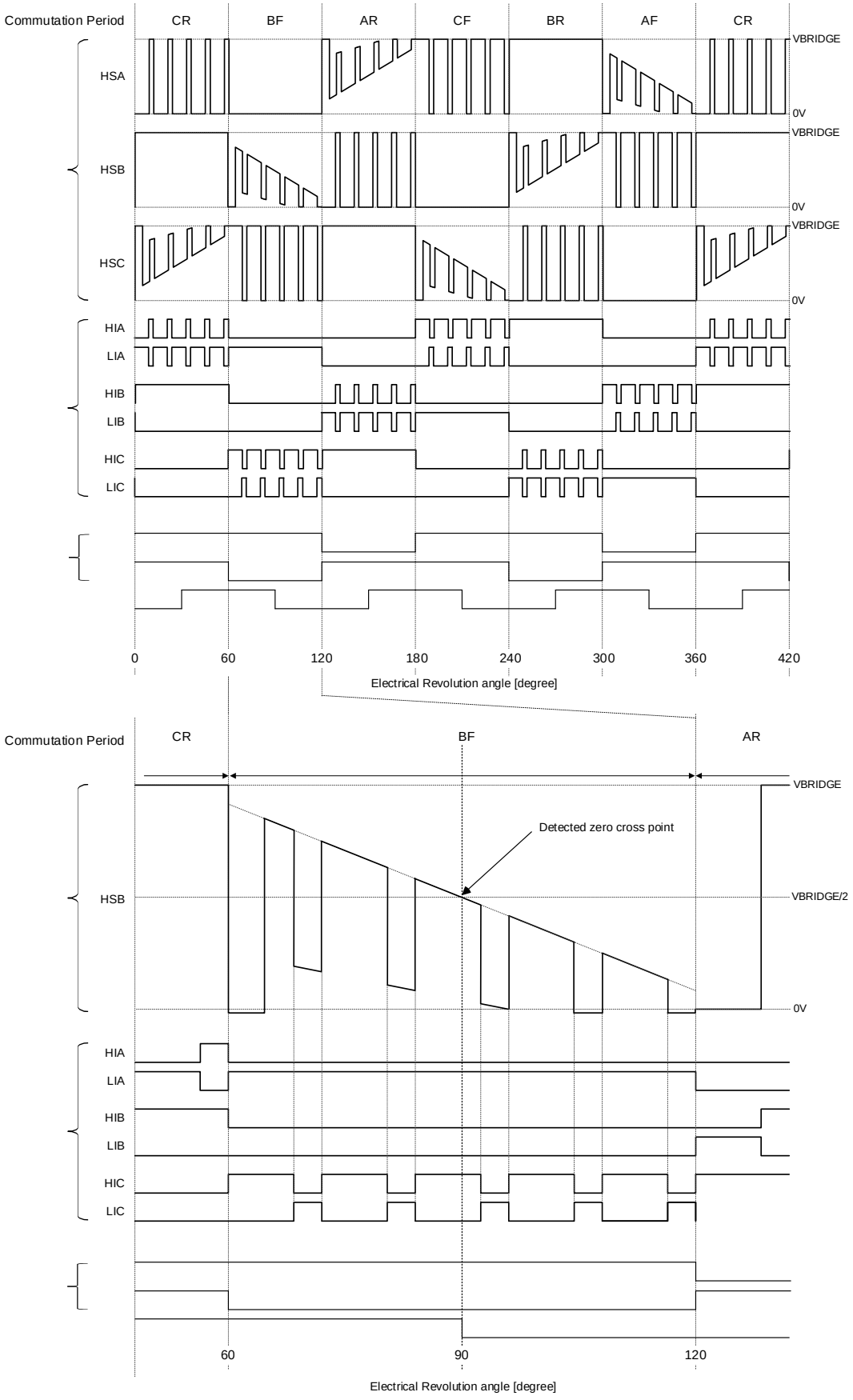


Figure 2-5 Operating Waveform Diagram – Sensor-less Motor Drive by BEMF Sensing Comparator

2.3.3 3 Shunt Sensor-less FOC Motor Drive

2.3.3.1 Circuit Diagram

Figure 2-6 shows an example of a simplified application block diagram for 3 shunt sensor-less FOC motor drive. In 3 shunt sensor-less FOC motor drive, the motor position is estimated from the 3-phase armature currents, and the motor rotation is controlled by PWM drive in the appropriate phase. The 3-phase armature currents can be detected by the 3-channels of differential amplifiers built into the smart gate driver and the A/D converter of the MCU. Therefore, no special external components are required except for the shunt resistors.
Figure 2-6 is an example in which all three shunt resistors are connected to the differential amplifiers. In sensor-less FOC motor drive, the number of shunt resistors and amplifiers used depends on the control method, the differential amplifiers unused for sensor-less FOC motor drive can be used for other purposes.

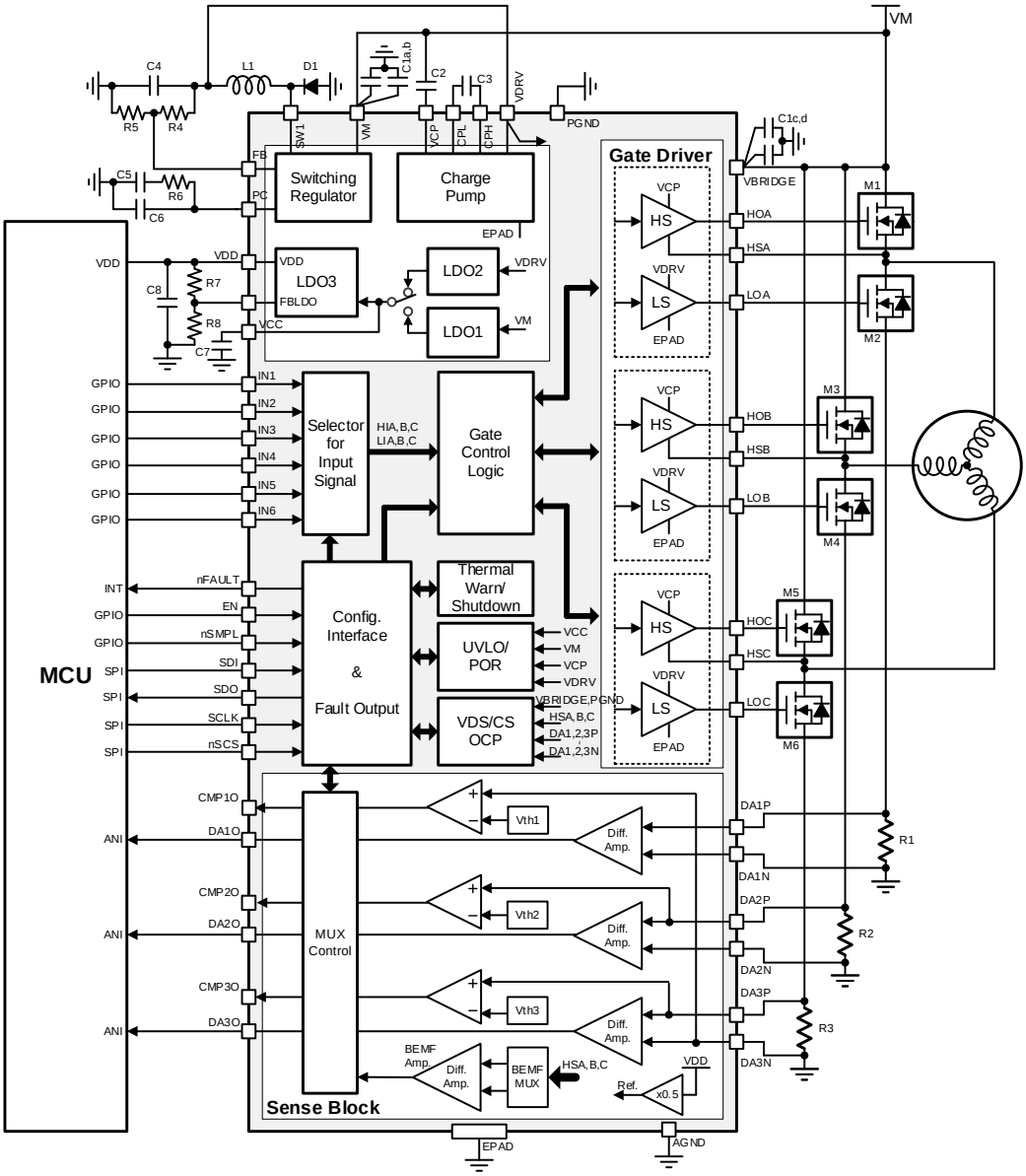


Figure 2-6 Simplified Application Block Diagram – 3 Shunt Sensor-less FOC Motor Drive

2.3.3.2 Register Settings

In the register settings for 3 shunt sensor-less FOC motor drive, the following settings are required for the differential amplifier 1, 2, and 3 in the sense block.

- ICCTL2 register: DA1_EN, DA2_EN, DA3_EN bits
- SNSCTL1 register: DA1_GAIN, DA2_GAIN, DA3_GAIN bits
- SNSCTL2 register: DA1_SH, DA2_SH, DA3_SH bits
- SNSCTL4 register: CAL_CONN, CAL_DA1, CAL_DA2, CAL_DA3/BEMF bits
- SNSCTL5 register: MUX bits

The start-up sequence of the smart gate driver is configured by dividing the register settings into three steps (Register Setting 1, 2, and 3) similar to the hall sensor motor drive by using 3 comparators. The similar settings and procedures are used except for the above register settings of the sense block. For details on each register, refer to ***2.3.1.2***.

For details on the DA3O/MUX1 pin output control, refer to ***6.5.5*** in the ***"RAA306012 Datasheet (R18DS0037EJ)"***. The unused general-purpose comparator can be disabled by setting CMPz_VTH (z = 1, 2, 3) bits to "0000b" to reduce power consumption.

2.3.3.3 Control Method

In the sensor-less FOC motor drive, the motor runs with open loop control in the low-speed region because the position and speed estimation error is not negligible. When the motor speed reaches the region that the position and speed estimation error is negligible, the control mode is shifted from open-loop control to sensor-less control (closed loop control). In the sensor-less control, it is necessary to estimate the position by some methods. RAJ306101 sample program that can be used for RAA306012 RSSK uses the position estimation method by the BEMF observer. For details, please refer to the application note of "***RAJ306101 Sample Program: Sensorless vector control for permanent magnetic synchronous motor (Implementation) (R18AN0060EJ)***" and ***"Motor Control Application: Sensorless Vector Control for Permanent Magnet Synchronous Motor (Algorithm) (R01AN3786EJ)***".

Chapter 3 Control Sequence

This device is used by controlling the operation mode by the MCU. To use this product to control a motor, the smart gate driver must be set to Operating Mode after the MCU reset is released, and the appropriate PWM signal must be input to INz (z = 1, 2, 3, 4, 5, 6). The smart gate driver operation mode depends on the EN output port setting of the MCU and the fault status of the smart gate driver.
This chapter shows the flowchart and notes on each step for the following two control sequence examples to control the smart gate driver operation mode.
1. Start-up sequence
2. Error recovery sequence

For details on the smart gate driver power-on sequence, operation modes and Fault Management, refer to ***6.1*** and **6.2** in the ***"RAA306012 Datasheet (R18DS0038EJ)"*** respectively. For details on register settings corresponding to motor control, refer to ***2.2***, ***2.3***, and "***Source Files for Each Sample Program of RAJ306101 and RAJ306102***".

3.1 Start-up Sequence Example

Figure 3-1 shows a flowchart of a start-up sequence example for the smart gate driver. In addition, the following are points to be noted at each step**.**

(1) Confirm power-on completion

This step is to judge the operation start of the start-up sequence. VCC pin voltage must be 4.0V (VCCUVR) or higher and the VM pin voltage must be 5.5V (VMUVR) or higher for the smart gate driver to start up. In this sequence example, after the measured VBRIDGE (= VM) pin voltage is at least 80% of the normal operating voltage, the sequence transitions to the next step. Consider an appropriate power supply confirmation method depending on the actual application, such as when using separate power supplies for the VM and VBRIDGE pins. In applications where the power-on completion is guaranteed by setting a wait time, it is acceptable to use a method that does not measure the power supply voltage.

(2) Wait for Smart Gate Driver start-up completion

This step is to wait until the power rail start-ups of the smart gate driver are done after the activation of the smart gate driver. First, the INz (z = 1, 2, 3, 4, 5, 6) output ports of the MCU are set to Low and the CMPzO (z = 1, 2, 3) input/output ports are set to digital input ports. The outputs of general-purpose comparators in the smart gate driver are set to output by default. These port settings of the MCU in advance can avoid unexpected gate driver outputs or output signal collisions with I/O ports of the MCU.
The smart gate driver is activated when the EN output port of the MCU is set to High. The nFAULT input port goes Low when the smart gate driver's band-gap voltage rises. The successful activation of the smart gate driver can be confirmed by checking the nFAULT input port.
After confirming the successful activation of the smart gate driver, a 15ms wait time is set. This is the wait time for the ready time of the internal oscillator, the DC offset calibration time of the differential amplifiers, the start-up time of the buck switching regulator and the charge pump. The wake-up time delay (twake) from the EN output port sets to High to the nFAULT input port goes High is 6.5ms (typ.), but since it varies depending on the clock frequency of the internal oscillator and the start-up time of the charge pump including external capacitors, check the actual start-up completion time and set to an appropriate wait time.

(3) Enable/disable fault detection functions and clear the Fault Status z (z = 0, 1, 2, 3) registers

This step is to select enable/disable for each fault detection function and clear the Fault Status z (z = 0, 1, 2, 3) registers (FLTSTSz (z = 0, 1, 2, 3)), which contain the indicators corresponding to each fault detection, before driving the motor.
The Fault Control 1 register (FLTCTL1) and the Fault Control 2 register (FLTCTL2) are used to select enable/disable for each fault detection function. Only current sense overcurrent protection by shunt resistor (CS_OCP), where the input signals to DAzP and DAzN (z = 1, 2, 3) are different depending on the application, is disabled by default. Enable the suitable fault detection functions according to the actual application and specifications. The Fault Status z (z = 0, 1, 2, 3) register can be cleared by setting the CLR_FLT bit in the IC Control 1 register (ICCTL1) to “1b”. The CLR_FLT bit automatically returns to “0b”. It is recommended that the other settings in the IC Control 1 register (ICCTL1) be set together when setting the CLR_FLT bit.
A 1ms wait time is provided as the status clear execution time after completing Register Setting 1 (refer to ***2.3.1.2 (1)***) as the status clear execution time, even 300µs including variation is sufficient.

(4) Confirm normal start-up completion and set registers according to application

This step is to confirm the normal start-up completion of the smart gate driver, set the various registers of the gate driver and sense block, and complete the start-up sequence.
nFAULT input port is checked, and if it is High, the start-up is judged to have been completed normally. This indicates that the smart gate driver has entered to the Operating Mode. On the other hand, if the nFAULT input port is low, it means that a fault detection has been triggered and the Initial Error is judged. If an error occurs at start-up after power-on, it is assumed that some power rails are abnormal, so set the EN output port to Low to stop the smart gate driver operation.
After confirming the nFAULT input port is High, set register settings for the gate driver and sense block as Register Setting 2 (refer to ***2.3.1.2 (2)***). In this example sequence, it is configured that the DC offset calibration of the differential amplifiers to be used is executed in Register Setting 2. The DC offset calibration of the corresponding amplifiers is initiated by setting the CAL_DA1 bit, CAL_DA2 bit, and CAL_DA3/BEMF bit in the Sense Block Control 4 register (SNSCTL4) to “1b”. By using the CAL_CONN bit, it is possible to perform offset calibration with high accuracy using the same inputs as the actual differential amplifier. It is recommended that the CAL_CONN bit be set to “1b”. However, note that when a motor is being driven or motor current is flowing through the shunt resistor, it is impossible to perform a normal offset calibration.
A 1ms wait time is provided after the initiation of the DC offset calibration in Register Setting 2. Since the DC offset calibration requires a wait time of 400µs per amplifier, set the wait time according to the number of amplifier to be calibrated, or use the automatic clear function of the CAL_DA1 bit, CAL_DA2 bit, and CAL_DA3/BEMF bit to confirm completion of the DC offset calibration.
In Register Setting 3 (refer to ***2.3.1.2 (3)***), set the detect phase selection method of the BEMF sense amplifier and change the Sense Block Control 6 register (SNSCTL6) setting to the recommended value.
When using the BEMF sense amplifier, the BEMF_PH bit in the Sense Block Control 2 register (SNSCTL2) must be set to the appropriate selection method. For details, refer to ***6.5.3*** in the ***“RAA306012 Datasheet (R18DS0037EJ)”***.
Sense Block Control 6 register (SNSCTL6) has a write-protection function and is initially in a write-locked state, so set the registers according to the following procedure.
(1) Set CTL6_UNLOCK bit of SNSCTL5 register to “1b” (Release the write lock to the SNSCTL6 register)
(2) Set SNSCTL6 register to “0x41”
(3) Set CTL6_UNLOCK bit of SNSCTL5 register to “0b” (Set the write lock to SNSCTL6 register)
After completing Register Setting 3, the MCU can change the CMPzO (z = 1, 2, 3) input/output port settings according to application. This completes the start-up sequence.

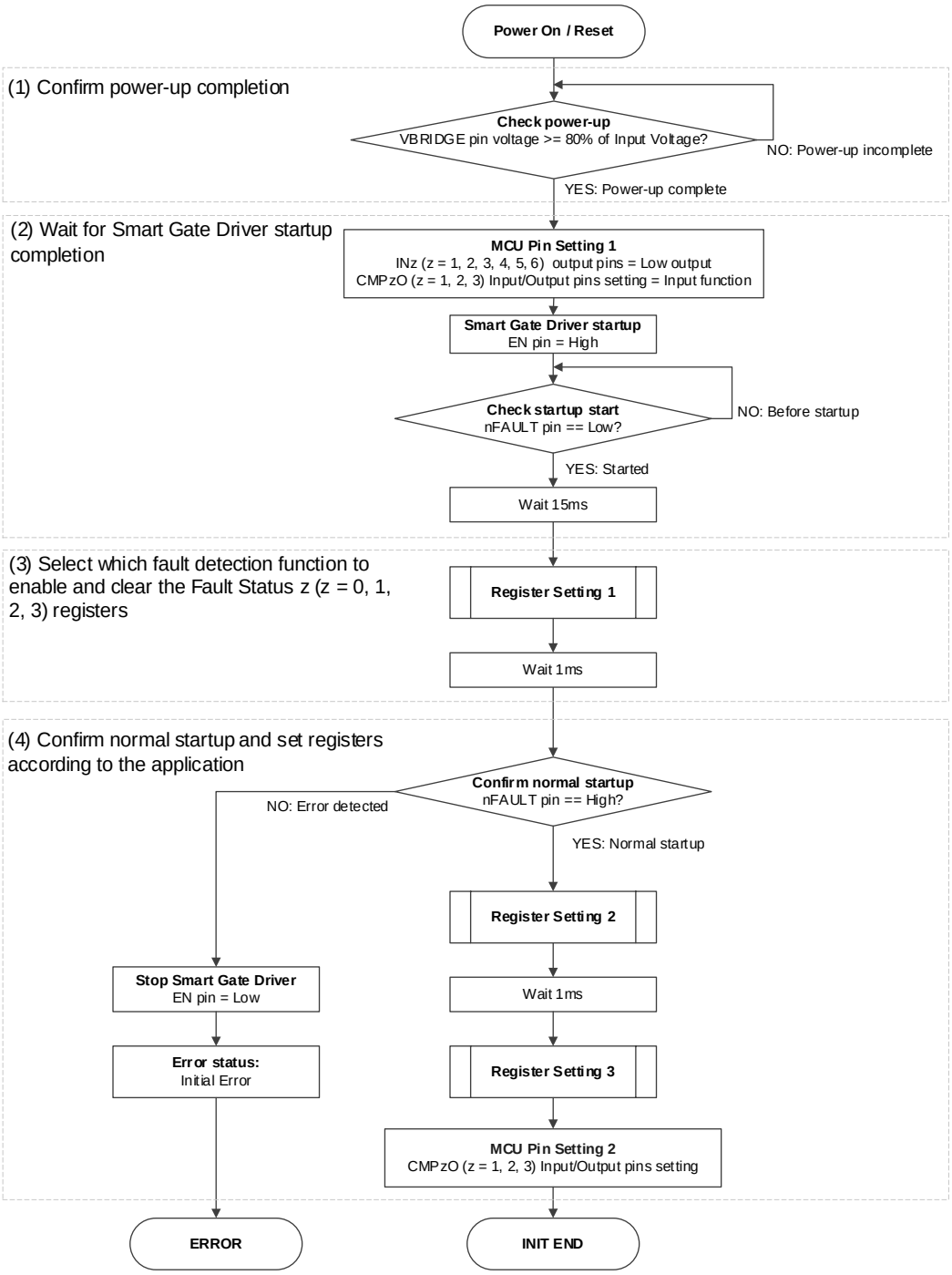


Figure 3-1 Smart Gate Driver Start-up Sequence Example

3.2 Error Recovery Sequence Example

Figure 3-2 shows a flowchart of an error recovery sequence example for the smart gate driver. The fault and recovery actions for the fault detection functions of the smart gate driver depend on the contents of the fault detection. Although these actions also depend on the register settings for the fault detection function, they are classified as follow*ings in the sequence example shown in* ***Figure 3-2***.

(a) Fault detection with automatic recovery (OTSD, TWARN, VM_UV, VM_OV, VDRV_OV)
(b) Fault detection with automatic recovery and the power rails restart (VCP_UV, SR_OCP, VDRV_UV)
(c) Fault detection without automatic recovery (latched mode fault) (VDS_OCP, VGS_FAULT, CS_OCP)

In the error recovery sequence, it is important to check the contents of the fault detection, classify them according to the contents of the fault detection and the recovery action as described above, and then design a recovery flow corresponding to each fault detection. The followings are points to be noted at each step of the error recovery sequence. This sequence example is used in the sample program of this device. All errors including the abnormality of the motor drive are configured to pass through this sequence. Refer to ***"Source Files for Each Sample Program of RAJ306101 and RAJ306102"*** and modify the sequence configuration according to the specification of error handling on application.

(1) Check operation status

In the first step of the error recovery sequence, the status of the EN output port is checked to judge whether the detected error is recoverable or not. When the EN output port is Low, the error corresponds to an Initial Error in the start-up sequence, a Regulator Error that the power rails could not be restarted as described below, or an Overcurrent Error that is not automatically recoverable. In these cases, the EN output port is configured to remain Low as a non-recoverable error detection.

(2) Check error contents and port settings

This step is to confirm whether the error has been detected in the smart gate driver and to change the port settings in advance for recovery. If the smart gate driver does not report any error (FAULT bit in Fault Status 0 register (FLTSTS0) is "0b"), the error is judged as being caused by other than the smart gate driver, such as a motor rotation error. In this case, the smart gate driver does not need to recover, and the error recovery sequence is terminated.
On the other hand, if the FAULT bit is "1b", the smart gate driver is judged to have occurred the fault. The INz (z = 1, 2, 3, 4, 5, 6) output ports must be set to Low and the CMPzO (z = 1, 2, 3) input/output ports must be set to Input mode. These port settings avoid unexpected gate driver outputs or output signal collisions with the I/O ports of the MCU by the recovery action from the fault condition.

(3) Classify error

This step is to classify the detected error into (a), (b), and (c) using the read result of the Fault Status z (z = 0, 1, 2, 3) registers (FLTSTSz (z = 0, 1, 2, 3)). If multiple errors are detected, it is recommended that they be classified according to the priority of (c), (b), and (a). Consider the appropriate classification for each error detection according to the application and specifications.

(4) Confirm recovery

This step is to confirm the automatic recovery completion of the smart gate driver by checking the nFAULT input port. When the nFAULT input port is Low, the operation mode of the smart gate driver has not returned to the Operating Mode, so the error recovery sequence is terminated and restarted again. When the nFAULT input port is High, the Operating Mode is recovered, the smart gate driver can operate normally, and the sequence step transitions to (7) Handling to complete recovery.

(5) Confirm power rails restart and Handling to stop

This step judges whether the power rails have recovered by restart for the error classified as (b) in the step of (3) Classify error. If it cannot be recovered, the handling to stop the smart gate driver is executed.
If SR_OCP or VDRV_UV error is detected, the buck switching regulator enters Hiccup mode, where the PWM is disabled for a dummy cycle (63ms) and the true soft-start cycle is attempted again after the dummy cycle. Considering the variation of the dummy cycle and the soft-start period, a wait time of 100ms or more (150ms in the sequence example) is provided before checking the nFAULT input port to judge whether the power rails have recovered.
In this sequence example, this nFAULT check is repeated up to 5 times, and if the nFAULT input port goes High and the power rails recover, the sequence step transitions to (7) Handling to complete recovery. If not, the EN output port is set to Low to stop the smart gate driver, the Regulator Error is judged, the error recovery sequence is terminated, and the smart gate driver remains stopped.
This sequence example shows the same sequence of checking the nFAULT input port every 150ms when a VCP_UV fault is detected. Since the charge pump does not enter Hiccup mode like the buck switching regulator, the timing for checking the nFAULT input port can be changed to the different check timing from the buck switching regulator. Please consider the appropriate check timing and handling according to the actual application and specifications.

(6) Handling to stop for latched mode fault

This step is to stop the smart gate driver when a fault is detected that keeps the smart gate driver in Fault Management Mode. Since this fault detection is caused by the half bridge error, the EN output port is set to Low to stop the smart gate driver, the Overcurrent Error is judged, the error recovery sequence is terminated, and the smart gate driver remains stopped.

(7) Handling to complete recovery

This step is to clear the Fault Status z (z = 0, 1, 2, 3) registers and to reconfigure the I/O ports of the MCU for the motor restart when the automatic recovery of the smart gate driver is confirmed in the (4) Confirm recovery and (5) Confirm power rails restart and Handling to stop. The CLR_FLT bit in the IC Control 1 register (ICCTL1) clears the Fault Status z (z = 0, 1, 2, 3) registers and the CMPzO (z = 1, 2, 3) input/output ports are changed to application-specific settings to complete the error recovery sequence. The error recovery sequence is terminated.

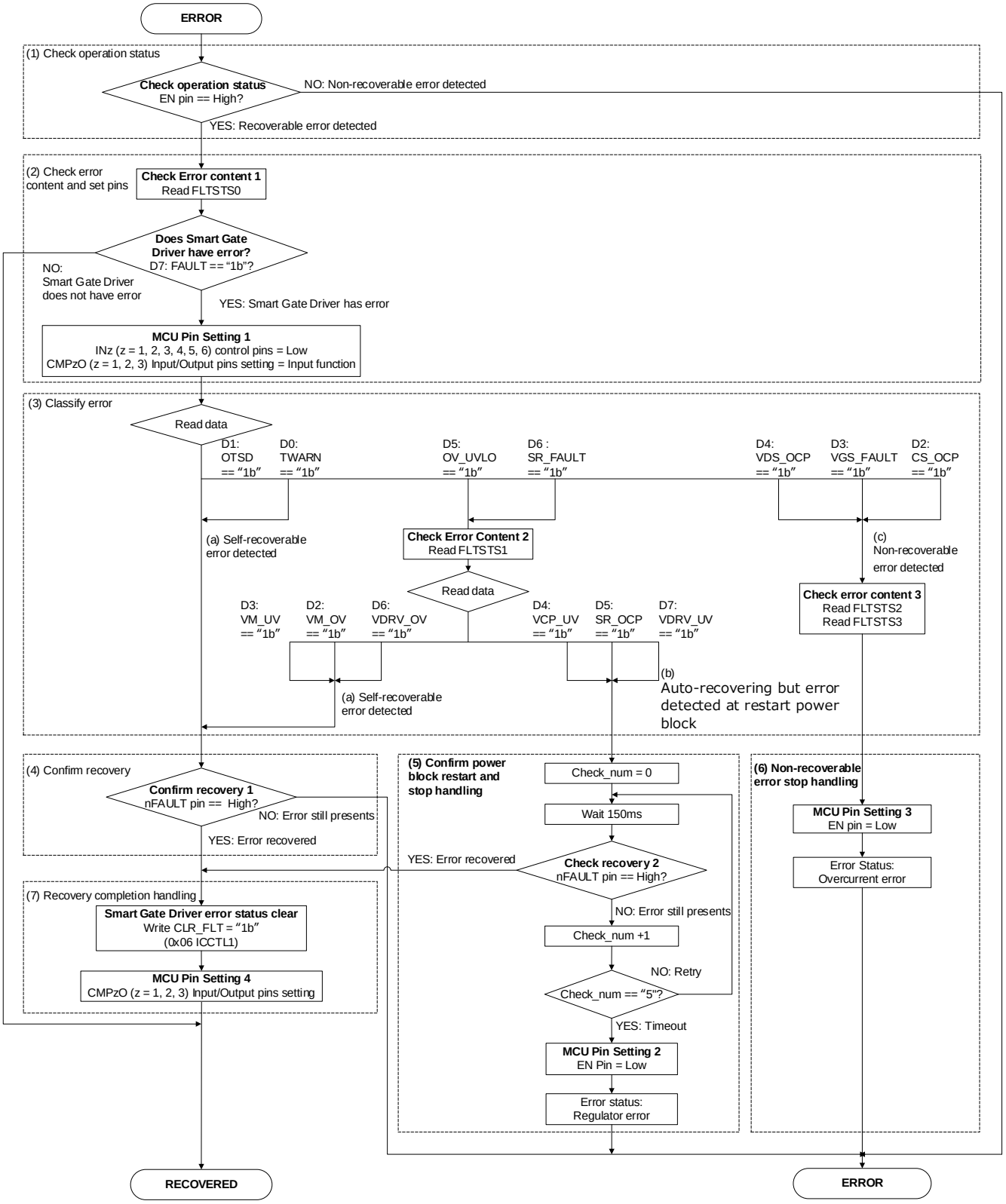


Figure 3-2 Smart Gate Driver Error Recovery Sequence Example

Chapter 4 Circuit Design, Component Selection, and Board Layout Recommendations

The RAA306012 incorporates both circuits that operates at high voltages and high slew rates and becomes noise sources, such as buck switching regulators, charge pumps, and gate drivers, and small-signal circuits that are sensitive to noise, such as differential amplifiers and BEMF detection amplifiers. Therefore, it is important to use this device with the appropriate hardware configuration. This chapter describes the circuit design, component selection and precautions, and board layout recommendations. The appropriate hardware configuration for each application should be determined by careful checks and verifications based on the operating environment, conditions, and specifications.

4.1 Circuit Design, Component Selection, and Precautions

Figure 4-1 and ***Table 4-1*** show an example of the external circuit for *3 shunt sensor-less FOC motor drive and the external component list.* The effective capacitance value of the capacitor decreases from the nominal value according to the applied voltage due to the DC bias characteristics. Please select the capacitors in consideration of the DC bias characteristics of the product. The capacitance values shown in the following descriptions are nominal values.

The example parts list shows the effective capacitance value of the capacitor used on our evaluation board (RTK0EM00F0B00022BJ) as a reference.

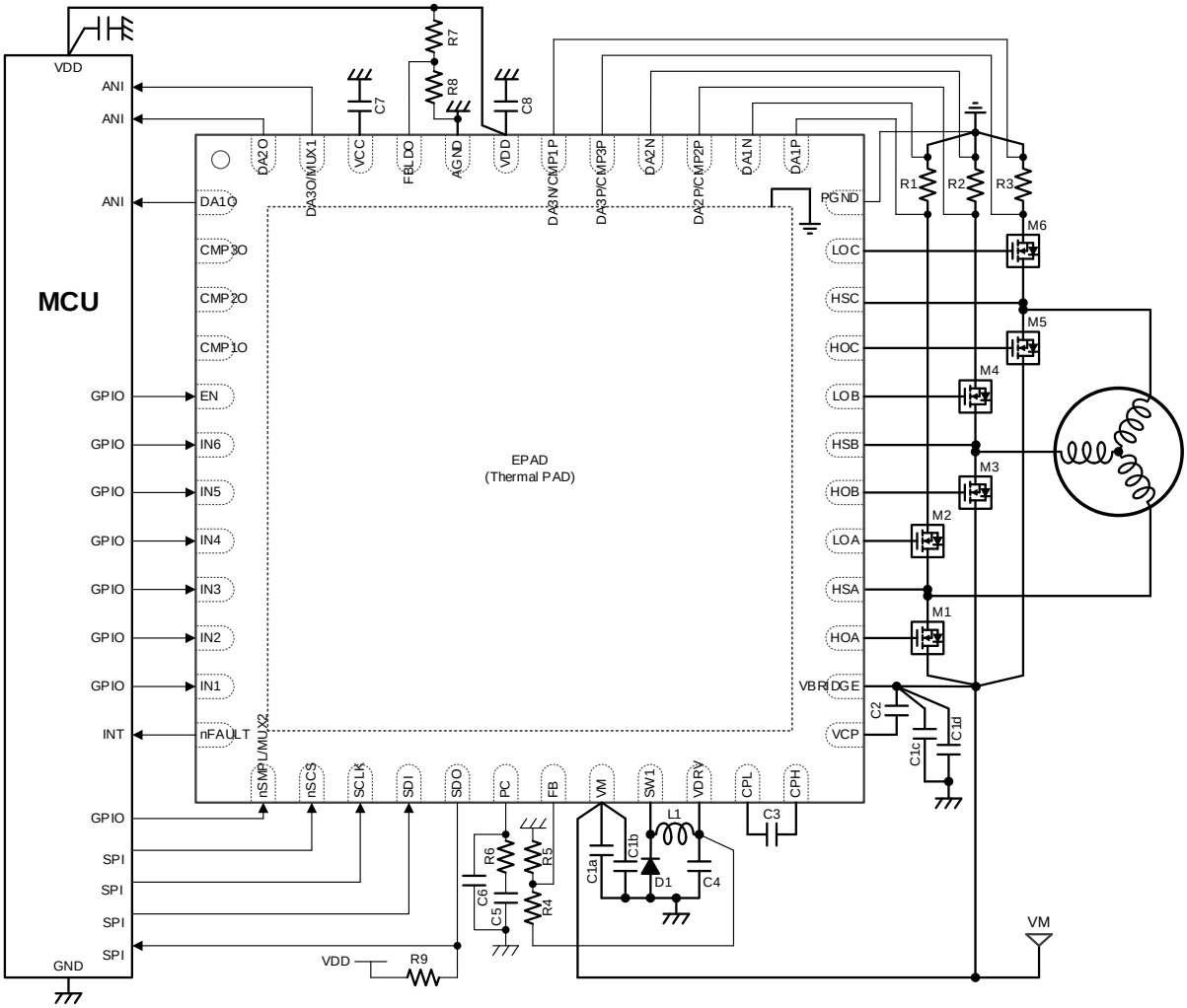


Figure 4-1 External Circuit Example of 3 Shunt Sensor-less FOC Motor Drive

Table 4-1 External Component List Example of 3 Shunt Sensor-less FOC Motor Drive

Part No.	Recommended value	Recommended value	Ratings	Purpose	Notes
R1 to R3	Depend on application	-	Depend on application	Shunt resistance for current sense	
R4	48.7kΩ	-	-	Bleeder resistance for VDRV output voltage setting	1
R5	3.48kΩ	-	-	Bleeder resistance for VDRV output voltage setting	2
R6	60.4kΩ	-	-	Phase compensation resistance for the switching regulator	5
R7	160kΩ	-	-	Bleeder resistance for VDD output voltage setting	2
R8	91kΩ	-	-	Bleeder resistance for VDD output voltage setting	2
R9	DNP	-	-	Pullup resistance for SDO pin. Pullup function of MCU I/O can be used.	3
C1a	3 x 4.7μF	2 x 5.45μF	100V	Bypass capacitance for VM pin	6
C1b	0.1μF	0.038μF	100V	Bypass capacitance for VM pin	6
C1c	4.7μF	5.45μF	100V	Bypass capacitance for VBRIDGE pin	6
C1d	0.1μF	0.038μF	100V	Bypass capacitance for VBRIDGE pin	6
C2	2.2μF	1.04μF	25V	Bypass capacitance for VCP pin	4
C3	0.22μF	0.18μF	100V	Pumping capacitance for the charge pump	4
C4	10μF	5.5μF	25V	Output capacitance for the switching regulator (VDRV pin)	5
C5	2200pF	2190pF	10V	Phase compensation capacitance for the switching regulator	5
C6	DNP	DNP	10V	Phase compensation capacitance for the switching regulator	
C7	22μF	10.3μF	10V	Output capacitance for the linear regulator (VCC pin)	
C8	22μF	10.3μF	10V	Output capacitance for the linear regulator (VDD pin)	
M1 to M6	Depend on application	-	Depend on application	Power MOSFET for the motor drive	
L1	22μH or 33μH	-	>2A	Coil for the switching regulator	
D1	0.6V	-	100V, >2A	Schottky rectifier diode for the switching regulator	
MCU	RX13T or RL78/G1F	-	3.3 or 5V operation	Microcontroller for the motor drive control	

Note1: VDRV output voltage is 12V with these resistors.
Note2: VDD output voltage is 3.310V with these resistors.
Note3: In some cases, the external pull-up resistor for SDO pin is required depending on the SCLK period and the load capacitance including the parasitic capacitance.
Note4: Please consider the effective capacitance. The smaller C3 causes the larger voltage to drop of VCP. The smaller C2 causes the larger voltage ripple of VCP.
Note5: Please select the suitable value of R6 and C5 depending on C4 effective capacitance.
Note6: The suitable capacitance depends on the constraints of the application and characteristic.

4.1.1 VM, VBRIDGE Pin Capacitors (C1a, C1b, C1c, C1d)

This device operates by supplying DC power (6 to 65V) to the VM and VBRIDGE pins. The capacitors are required in the power supply line to stabilize the power supply and to handle high frequency currents. These capacitors can prevent abrupt voltage changes during system power-on. Increasing capacitance helps reduce power supply ripple but increases size and cost. The appropriate capacitor should be selected considering the motor system operating voltage, switching frequency, required current capability, allowable power supply ripple, motor type, and start-up/stop sequence constraints.

The power supply line for high frequency components causes an increase in impedance due to parasitic inductance of the battery and cables; a local capacitor placed near to the power supply pins of this device has the effect of reducing the impedance for high frequencies and thus contributes as a preferable path for the high frequency components. The appropriate local capacitor should be selected based on ripple current, resonant frequency, package, cost constraints, etc. In a typical application, electrolytic capacitors are placed near to the DC power input, and several ceramic capacitors are placed near to the VM and VBRIDGE pins of this device as well.

4.1.2 Linear Regulator Components (C7, C8, R7, R8)

In this device, the VCC pin or the VDD pin can be used as a power supply for peripheral circuits including the MCU. LDO3 that supplies voltage to the VDD pin are supplied from LDO1 and LDO2 that supply 5V to the VCC pin. Therefore, the allowable external load current capability is defined as the total of VCC pin and the VDD pin load current including MCU.

The total current supplied from the VCC and VDD pins to the MCU and peripheral circuits should not exceed the allowable external load current as shown below. When the EN output port is low, LDO1 is ON and LDO2 is OFF. For details on the ON/OFF states of LDO1 and LDO2 according to the Power-On sequence, the smart gate driver mode, and fault and recovery action of fault detection functions, refer to ***6.1***, ***6.3.1*** and ***6.2*** in the ***"RAA306012 Datasheet (R18DS0037EJ)"***.

Condition			External Load Current Capability
EN output port	**5V LDO1**	**5V LDO2**	
Low	ON	OFF	50mA
High	ON	OFF	70mA
High	OFF	ON	90mA

Table 4-2 External Load Current Capability for VCC and VDD Pins

4.1.2.1 VCC Pin Capacitor (C7)

This device contains two LDOs: LDO1 and LDO2, which supply 5V to the VCC pin. These LDOs can supply 5V to the analog and logic circuits in the smart gate driver as well as 5V to the peripheral circuits including the MCU. The voltage on the VCC pin is generated by LDO1, which is powered by the VM pin, while the smart gate driver is disabled (EN output pin = Low), before the smart gate driver is enabled (EN output pin = High) and the buck switching regulator completes start-up. After the start-up of buck switching regulator is completed, the voltage on the VCC pin is generated by LDO2, which is powered by the VDRV pin. A ceramic capacitor of 22µF (with an effective capacitance value of about 10µF) is recommended as the decoupling capacitor (C7) on the VCC pin. This capacitor should be placed as close as possible to the VCC and AGND pins.

4.1.2.2 VDD Pin Capacitor (C8), VDD Output Voltage Setting Resistors (R7, R8)

The smart gate driver uses VDD pin as the interface power supply.
There are three methods to supply voltage to the VDD pin: (1) by using LDO3, (2) by supplying 5V from the VCC pin, or (3) by using an external power supply. The following are precautions for each method.

(1) Supply using LDO3

The external connection and components are shown in ***Figure 4-2 (1).*** The LDO3 output voltage VDD is determined by the bleeder resistors (R7, R8) that are fed back to the FBLDO pin, allowing fine adjustment of the output voltage within the recommended operating conditions. The bleeder resistors should be selected based on ***EQ 4-1.*** Increasing the total value of the bleeder resistor can reduce the current consumption in Sleep Mode. However, note that the stability is reduced by the pole determined by the parasitic capacitance of FBLDO pin and the bleeder resistors.

EQ 4-1

$$V_{DD} = V_{REF\_DD}\left(1 + \frac{R_7}{R_8}\right)$$

where: V_{REF_DD}: FBLDO pin reference voltage = 1.2V, R_7: resistance between VDD and FBLDO pins, R_8: resistance between FBLDO and AGND pins

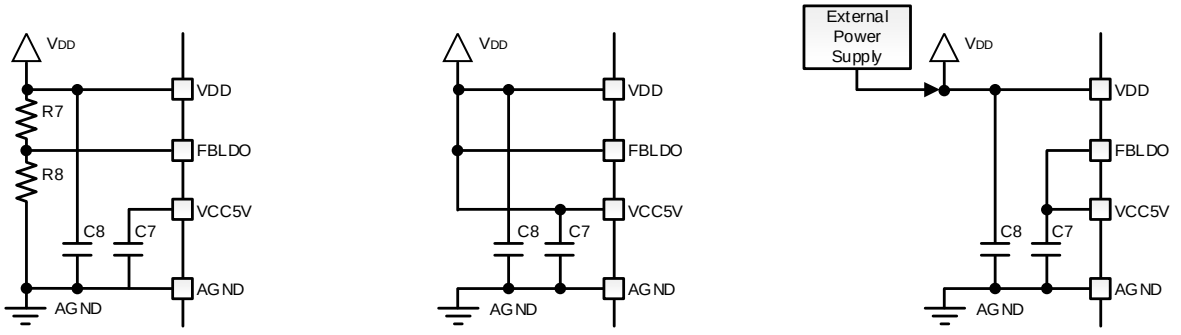
If R_7 = 160kΩ and R_8 = 91kΩ, the output voltage of LDO3 becomes 3.310V. A 22µF (effective capacitance value of about 10µF) ceramic capacitor is recommended as the decoupling capacitor (C8) on the VDD pin. This capacitor should be placed as close as possible to the VDD and AGND pins.

(2) Supply 5V from the VCC pin

The external connection and components are shown in ***Figure 4-2 (2)***. A 0.1µF ceramic capacitor is recommended as a decoupling capacitor (C8) for the VDD pin. This capacitor should be placed as close as possible to the VDD and AGND pins.

(3) Supply using an external power supply

The external connection and components are shown in ***Figure 4-2 (3)***. Connect an external power supply to the VDD pin. Also, connect the FBLDO pin to the VCC pin. Note that the recommended operating voltage range VDDope for the VDD pin voltage is limited from 3.135 to 5.25V. A 0.1µF ceramic capacitor is recommended as the decoupling capacitor (C8) on the VDD pin. This capacitor should be placed as close as possible to the VDD and AGND pins.



(1) VDD = LDO3 (2) VDD = VCC (3) VDD = External power supply

Figure 4-2 VDD Pin Voltage Supply Methods

4.1.3 Components for Buck Switching Regulator (R4, R5, L1, C4, C5, R6)

4.1.3.1 Resistors for VDRV Output Voltage Setting (R4, R5)

The VDRV pin is the output pin of the buck switching regulator. It is used as the power supply for the low-side gate driver and the power supply for LDO2, which supplies 5V to the VCC pin. The output voltage depends on the bleeder ratio (R_4/R_5) of the external feedback resistor configured with the VDRV and FB pins shown in ***Figure 4-3***.

The output voltage V_{DRV} is adjustable from 5 to 15V and can be calculated using ***EQ 4-2***.

EQ 4-2

$$V_{DRV} = V_{REF\_SR}\left(1 + \frac{R_4}{R_5}\right)$$

where: V_{REF_SR}: FB pin reference voltage = 0.8V, R_4: resistance between VDRV and FB pin, R_5: resistance between FB and AGND pin.

For example, if R_4 = 48.7kΩ and R_5 = 3.48kΩ, then V_{DRV} = 12V; if R_4 = 47kΩ and R_5 = 3.3kΩ, then V_{DRV} = 12.19V.

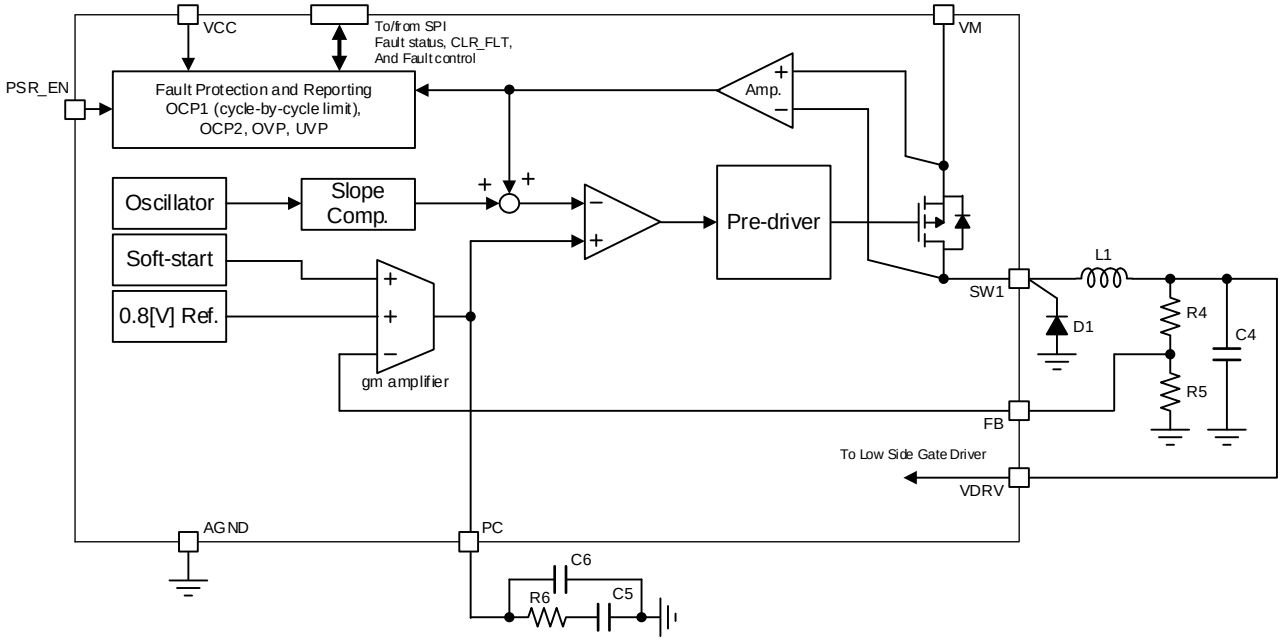


Figure 4-3 Buck Switching Regulator Block Diagram

4.1.3.2 Inductor (L1)

The buck switching regulator generates the VDRV pin voltage at a switching frequency of 500kHz. The buck switching regulator requires a 33µH or 22µH inductor (L1). The inductance of the inductor (L1) determines the ripple current (ΔI). Generally, the ripple current is assumed to be about 30 to 40% of the maximum output load current. Select a inductor (L1) with its peak current including ripple current not exceeding 1A considering the size of the component and load conditions. The values of ripple current (ΔI) and peak current (I_{peak}) of the inductor (L1) can be estimated by ***EQ 4-3*** and ***EQ 4-4***. A 33µH inductor has a ripple current (ΔI) larger than the expected value, as shown in the example below, but this is the recommended value considering the output ripple voltage (ΔV_{DRV}).

EQ 4-3

$$\Delta I = \frac{V_M - V_{DRV}}{f_{sw} \times L_1} \times \frac{V_{DRV}}{V_M}$$

where V_M: input voltage, V_{DRV}: output voltage, f_{sw} : switching frequency = 500kHz, L_1: inductance.

EQ 4-4

$$I_{peak} = I_o + \frac{\Delta I}{2}$$

where I_o: maximum output load current.

For example, if V_M = 48V, V_{DRV} = 12V, L_1 = 33µH, I_o = 0.5A, then ΔI = 0.545A and I_{peak} = 0.773A. If the ripple current (ΔI) of the inductor (L1) becomes large and the peak current (I_{peak}) becomes larger, the current limit (IOC1_SR) (1.2A typ.) per PWM cycle may be triggered when the load current of the VDRV pin is large. Since this limits the load current capability, the inductance should be selected considering the required load current. On the other hand, increasing the inductance can reduce the ripple current and ripple voltage. However, the larger inductance worsens the load transient response, so the actual output voltage (V_{DRV}) waveform should be checked for the suitable component selection. Also, for the inductor specification of the maximum DC current, select a component whose inductance does not decrease significantly even under the current limit (I_{OC1_SR}) conditions.

4.1.3.3 Input Capacitors (C1a, C1b), Output Capacitor (C4)

An output capacitor (C4) is required to smooth the inductor current. The output ripple voltage (ΔV_{DRV}) and load transient response are two important factors when selecting the output capacitor (C4). These characteristics should be considered in terms of the effective capacitance value considering the DC bias characteristic. For the characteristics of capacitors used in the actual application, refer to the "***Datasheets of Relevant Components"***. Under the assumption that low ESR ceramic capacitors are used, the capacitance required to satisfy the output ripple voltage (ΔV_{DRV}) in a buck switching regulator can be estimated by ***EQ 4-5***.

EQ 4-5

$$\Delta V_{DRV} = \frac{\Delta I}{8 \times f_{sw} \times C_4}$$

where ΔI: ripple current of the inductor, f_{sw}: switching frequency = 500kHz, C_4: effective capacitance of the output capacitor.

For example, if ΔI = 0.545A and C_4 = 5.5µF (effective capacitance value), then ΔV_{DRV} = 24.8mV.
In general, to supply a stable input voltage, the main power supply source requires electrolytic capacitors with capacitance corresponding to the input power supply conditions of the system. For better EMC performance, it is important to absorb the switching frequency pulse current by the buck switching regulator, and the input capacitors on the VM pin (C1a, C1b) should be able to handle the RMS current from the switching power supply circuit. Therefore, ceramic capacitors must be used for the input capacitors on the VM pin. The multiple capacitors including 1µF or more and 0.1µF are recommended according to EMC performance. These capacitors should be placed as close as possible to this device. (For the placement of each capacitor, refer to ***4.2***.)

4.1.3.4 Phase Compensation Capacitor (C5) and Resistor (R6)

The phase compensation is required for the stable operation of the buck switching regulator. The following describes how to select the phase compensation capacitor (C5) and resistor (R6).
First, determine the open-loop gain. The buck switching regulator consists of the following three gains, A_1, A_2, and A_3, which can be obtained by ***EQ 4-6***, ***EQ 4-7*** and ***EQ 4-8*** respectively.

- A_1: Gain from VDRV to FB pin by resistor voltage divider
- A_2: Gain from FB pin to gm amplifier output (PC pin)
- A_3: Gain from PC pin to VDRV pin

The open-loop transfer function A_{OPN} is the product of these gains and can be obtained by ***EQ 4-9***. If V_{DRV} = 12V, I_o = 0.5A, then A_{OPN} = 9766V/V = 79.79dB.

EQ 4-6

$$A_1 = \frac{V_{REF\_SR}}{V_{DRV}}$$

where V_{REF_SR}: FB pin reference voltage = 0.8V, V_{DRV}: VDRV pin voltage (V).

EQ 4-7

$$A_2 = g_{m\_SR} \times R_{oSR}$$

where g_{m_SR}: g_m amplifier transconductance = 200µA/V, R_{oSR}: g_m amplifier output resistance = 14MΩ.

EQ 4-8

$$A_3 = g_{m\_PW} \times R_{OUT} = g_{m\_PW} \times \frac{V_{DRV}}{I_o}$$

where g_{m_PW}: g_m amplifier current gain = 2.18A/V, R_{OUT}: VDRV pin output resistance, I_o: output load current (A).

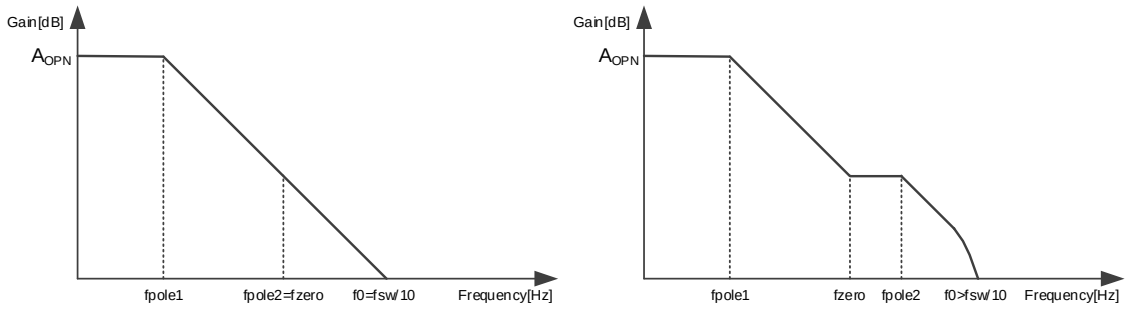
EQ 4-9

$$A_{OPN} = A_1 \times A_2 \times A_3$$

Next, determine the target bandwidth (f_0). In the buck switching regulator, the frequency response is mainly determined by the poles (1) and (2), and zero (3). (4) is a double pole due to switching operation, and the target bandwidth is set to a frequency lower than this double pole.

(1) f_{pole1}: 1st pole determined by g_m amplifier output resistance R_{oSR} and phase compensation capacitance (C_5)
(2) f_{pole2}: 2nd pole determined by VDRV pin output resistance R_{OUT} and output capacitance (C_4)
(3) f_{zero}: Zero determined by phase compensation resistance (R_6) and phase compensation capacitance (C_5)
(4) Double pole at half switching frequency (f_{sw}/2)

The target bandwidth (f_0) is set to 1/10 or less of the switching frequency (f_{sw}) to avoid stability degradation due to the phase delay of (4). The stability is ensured by setting (1) to match the target bandwidth (f_0) and canceling the pole (2) with the zero (3) (***Figure 4-4 (a)***).



(a) Bode plot with fpole2 cancelled by fzero (b) Bode plot when fpole > fzero

Figure 4-4 Image Diagram of Bandwidth and Phase Compensation for the Buck Switching Regulator

The 1st pole (f_{pole1}) is obtained by ***EQ 4-10***.

EQ 4-10

$$f_{pole1} = \frac{1}{2\pi \times R_{oSR} \times C_5}$$

where R_{oSR}: g_m amplifier output resistance = 14MΩ, C_5: phase compensation capacitance.

On the other hand, when the target bandwidth (f_0) is set to 1/N of the switching frequency (f_{sw}), the 1st pole (f_{pole1}) can also be obtained using the open loop gain (A_{OPN}) as in ***EQ 4-11***.

EQ 4-11

$$f_{pole1} = \frac{f_{sw}/\ N}{A_{OPN}}$$

Therefore, the phase compensation capacitance (C_5) can be calculated by ***EQ 4-12*** using ***EQ 4-10***, ***EQ 4-11***.

EQ 4-12

$$C_5 = \frac{A_{OPN} \times N}{2\pi \times R_{oSR} \times f_{sw}0}$$

If the target bandwidth (f_0) is 50kHz (N = 10), which is 1/10 of the switching frequency f_{sw} = 500kHz, A_{OPN} = 9766V/V, R_{oSR} = 14MΩ, then C_5 = 2221pF ≈ 2200pF.
The 2nd pole can be obtained by ***EQ 4-13***.

EQ 4-13

$$f_{pole2} = \frac{1}{2\pi \times R_{OUT} \times C_4} = \frac{I_o}{2\pi \times V_{DRV} \times C_4}$$

where R_{OUT}: VDRV pin output resistance (Ω), C_4: VDRV pin output effective capacitance, I_O: output load current (A).

One the other hand, zero (f_{zero}) is obtained by ***EQ 4-14***.

EQ 4-14

$$f_{zero} = \frac{1}{2\pi \times R_6 \times C_5}$$

where R_6: phase compensation resistance, C_5: phase compensation capacitance.

Since the first-order characteristic determined by the 1st pole (f_{pole1}) and the open-loop gain (A_{OPN}) can be obtained by canceling the 2nd pole (f_{pole2}) with zero (f_{zero}), the phase compensation resistance (R_6) can be calculated by using ***EQ 4-15***.

EQ 4-15

$$R_6 = \frac{V_{DRV} \times C_4}{I_o \times C_5}$$

If V_{DRV} = 12V, I_o = 0.5A, C_5 = 2200pF, C_4 = 5.5µF (effective capacitance value), then R_6 = 60kΩ ≈ 60.4kΩ. The output capacitor (C4) on the VDRV pin should be calculated with the effective capacitance value considering DC bias characteristics. The 2nd pole (f_{pole2}) depends on the output capacitance (C4). If the effective capacitance value is smaller than the value used in the calculation example, the 2nd pole (f_{pole2}) becomes a higher frequency than expected, and the actual bandwidth increases from the target bandwidth (f_0) as shown in ***Figure 4-4 (b)***. It causes the double pole (fpole1n, fpole2n) at a frequency of 1/2 of the switching frequency (f_{sw}) to be more susceptible and may affect stability.

4.1.4 Charge Pump Output Capacitor (C2), Pumping Capacitor (C3)

The charge pump output VCP pin is the power supply for the high-side gate driver. For charge pump operation, a pumping (flying) capacitor (C3) is required between the CPH and CPL pins. A ceramic capacitor with an effective capacitance value of 0.22µF allows a maximum load current of 28mA. The capacitor (C3) with the smaller effective capacitance value causes the greater the drop in VCP pin voltage at the same load. Select a capacitor (C3) that is appropriate for your external MOSFET, PWM frequency, and VCP pin voltage. The load current (I_{VCP}) to drive the external MOSFET can be estimated by ***EQ 4-16***. Note that the load current (I_{VCP}) increases if there are multiple phases operating PWM simultaneously in a 3-phase or 2-phase PWM drive.

EQ 4-16

$$I_{VCP} > N \times Q_g \times f_{PWM}$$

where N: number of simultaneous PWM phases, Q_g: external MOSFET gate input total charge, f_{PWM}: PWM frequency.

A ceramic capacitor with an effective capacitance value of at least 1µF is required between the VCP pin and the VBRIDGE pin as the output capacitor (C2). The output capacitor (C2) should be 5 times larger than the pumping capacitor (C3) considering the output ripple voltage due to charge pump operation.

4.1.5 External MOSFETs (M1 to M6) and Register Settings

4.1.5.1 ISRC_HS and ISRC_LS Bits Setting

The gate drive source (charge) currents (I_{SRCH}, I_{SRCL}) are adjusted by the ISRC_HS and ISRC_LS bits respectively based on the gate-to-drain charge (Q_{gd}) of the external MOSFETs, and the target rise and fall times (t_{RISE}, t_{FALL}) of the half-bridge gate driver output. If the gate drive source currents (I_{SRCH}, I_{SRCL}) set for the external MOSFETs are small, the gate-to-source voltage (V_{GS}) of the external MOSFET may not be fully charged within the maximum gate transition time (t_{GT}) set by the T_GT bit, causing a V_{GS} fault (VGS_FAULT) to be detected or an on-resistance power loss. In addition, slow rise and fall times increase switching power loss. Set the ISRC_HS and ISRC_LS bits appropriately according to the actual application including the external MOSFET and the motor. Using the gate-to-drain charge (Q_{gd}) of the external MOSFET and the target rise time (t_{RISE}) of the half-bridge gate driver output, the gate drive source current (I_{SRCH}) is calculated using ***EQ 4-17***.

EQ 4-17

$$I_{SRCH} > \frac{Q_{gd}}{t_{RISE}}$$

where Q_{gd}: external MOSFET gate-to-drain charge, t_{RISE}: target rise time.

The gate-drive sink (discharge) currents (I_{SNKH}, I_{SNKL}) are set to twice the gate-drive source currents (I_{SRCH}, I_{SRCL}). The target rise and fall time (t_{RISE}, t_{FALL}) should be set appropriately considering these characteristics.

4.1.5.2 DEAD_TIME Bit Setting

The adaptive dead-time function monitors the gate voltage of an external MOSFET during the turn-off transition, detects that the gate-to-source voltage (V_{GS}) falls below a threshold voltage (1V typ.), and then turns on the complementary MOSFET after an extra dead-time (t_{DT}) has elapsed. This function prevents the simultaneous turn-on of high-side and low-side external MOSFETs resulting shoot through and optimizes the diode power loss due to the dead time. The extra dead time (t_{DT}) can be adjusted by the DEAD_TIME bit. The value of the DEAD_TIME bit should be adjusted to ensure that the gate-source voltage (V_{GS}) after the extra dead time (t_{DT}) is less than the gate threshold voltage (V_{TH}), considering the gate-source charge (Q_{gs}) (at V_{GS} = 1V) and gate threshold voltage (V_{TH}) of the external MOSFET.
It is a recommended procedure to optimize the margin between the timing at which the gate-source voltage (V_{GS}) of the one-side external MOSFET falls a threshold voltage (1V typ.) and the turn-on timing of the complementary MOSFET. To prevent external MOSFET breakdown, set the DEAD_TIME bit from “11b” to smaller value gradually with monitoring the gate-source voltage (V_{GS}) of external MOSFETs.

4.1.5.3 T_GT Bit Setting

For half-bridge output switching characteristics optimized by adjusting the ISRC_HS and ISRC_LS bits, set the T_GT bit so that the maximum gate transition time (t_{GT}) is longer than the time required to complete charging the gate-to-source voltage (V_{GS}) of the external MOSFET. A sufficiently long maximum gate transition time (t_{GT}) has no effect on the switching characteristics of the half-bridge outputs, but an optimal maximum gate transition time (t_{GT}) provides low power consumption of gate driver in PWM operation.
It is a recommended procedure to optimize the margin between the timing to complete charging the gate-source voltage (V_{GS}) of the external MOSFET and the timing to complete the maximum gate transition time (t_{GT}). To prevent unintended detection of a V_{GS} fault (VGS_FAULT), set the T_GT bit from “11b” to smaller value gradually with monitoring the gate-source voltage (V_{GS}) of external MOSFETs.

4.1.6 Current Sensing Shunt Resistors (R1, R2, R3) and Differential Amplifier Gain

In this device, the motor drive current can be detected by measuring the differential voltage across the shunt resistor for current sensing (now referred to as “shunt resistor”) with the A/D converter of the MCU via a differential amplifier. The shunt resistor (Rz (z = 1, 2, 3)) is selected based on ***Figure 4-5***, ***EQ 4-18*** and ***EQ 4-20*** using the target current sensing range (I_{SNS}), supply voltage (V_{DD}), differential amplifier output range (V_{O_CSA}), input offset voltage (V_{IO_CSA}), and gain (G_{CSA}).

EQ 4-18

$$V_{O\_DM} = (V_{DD} - V_{O\_CSA}) - (0.5 \times V_{DD} + G_{CSA} \times V_{IO\_CSA})$$

For diffrential amplifier gain G_{CSA} = 20V/V, it becomes ***EQ 4-19***.

EQ 4-19

$$V_{O\_DM} = (3.3V - 0.4V) - (1.65V + 20 \times 5mV) = 1.15V$$

The shunt resistor Rz (z = 1, 2, 3) that can operate within the output dynamic range (V_{O_DM}) is calculated using ***EQ 4-20***.

EQ 4-20

$$R_z < \frac{V_{O\_DM}}{G_{CSA} \times I_{SNS}}$$

For a target current sensing range (I_{SNS}) = 50A, it becomes ***EQ 4-21***.

EQ 4-21

$$R_z < \frac{1.15V}{20 \times 50A} = 1.15m\Omega$$

If Rz = 1mΩ is selected, the power dissipation (P_{SNS}) of the shunt resistor Rz (z = 1, 2, 3) becomes ***EQ 4-22***, using the effective value of the target current sensing range (I_{SNS_RMS}).

EQ 4-22

$$P_{SNS} = I_{SNS\_RMS}^2 \times R_z = 35.4A^2 \times 1m\Omega = 1.25W$$

Please also select the shunt resistor Rz (z = 1, 2, 3) with consideration of the power rating of the component.

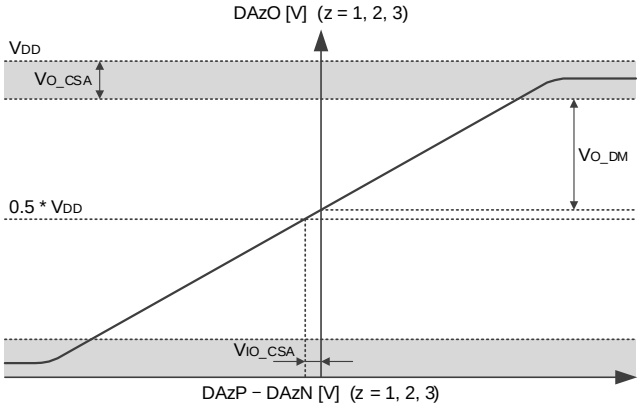


Figure 4-5 Output Dynamic Range of Current Sensing

4.1.7 External Protection Circuit Example

4.1.7.1 Phase Voltage Clamp Circuit with Resistor and Diode

Dead time is necessary to prevent shoot-through current generated by the simultaneous turning on of the high-side and low-side external MOSFETs during motor drive. When sourcing current to the motor, the motor drive current flows through the body diode of the low-side external MOSFET until the low-side external MOSFET is turned on after the high-side external MOSFET is turned off by the complementary PWM operation, but a negative voltage spike may occur at the timing of the falling edge on the bridge output.

In this device, the allowable negative voltage level is specified as the absolute maximum ratings of the HSx (x = A, B, C) pins. These ratings are $VHSx_{abs}$ (x = A, B, C) = -5V for continuous time and $VHSx_{tran}$ (x = A, B, C) = -7V. for transient within 200ns. Negative voltage spikes exceeding the absolute maximum ratings may cause product failure and must be protected by an external circuit.

The magnitude of negative voltage spikes depends on various factors such as operating supply voltage, dead time, transition time of the half-bridge output, external MOSFETs, shunt resistors, and motors, as well as board layout. To avoid negative voltage spikes exceeding the absolute maximum rating during the switching period of the half-bridge output, an external clamping circuit with resistors and diodes may be required.

Figure 4-6 shows an example circuit. The resistors (R_{Sx} (x = A, B, C)) are inserted in the gate drive sink (discharge) current path of the high-side external MOSFET, thus affecting the fall time of the half-bridge output and the gate voltage monitoring of the adaptive dead-time function.

Resistors (R_{Sx} (x = A, B, C)) should be selected to be 10Ω or less, and their effects as well as side effects should be checked with actual waveforms. Resistors (R_{Sx} (x = A, B, C)) and diodes (D_{SxN} (x = A, B, C)) should be placed as close as possible to this device in the board layout design.

A positive voltage spike exceeding the absolute maximum ratings may also occur at the timing of the rising edge on the bridge output when sinking current from the motor. Consider adding diodes (D_{SxP} (x = A, B, C)) for protection of positive voltage spikes if necessary.

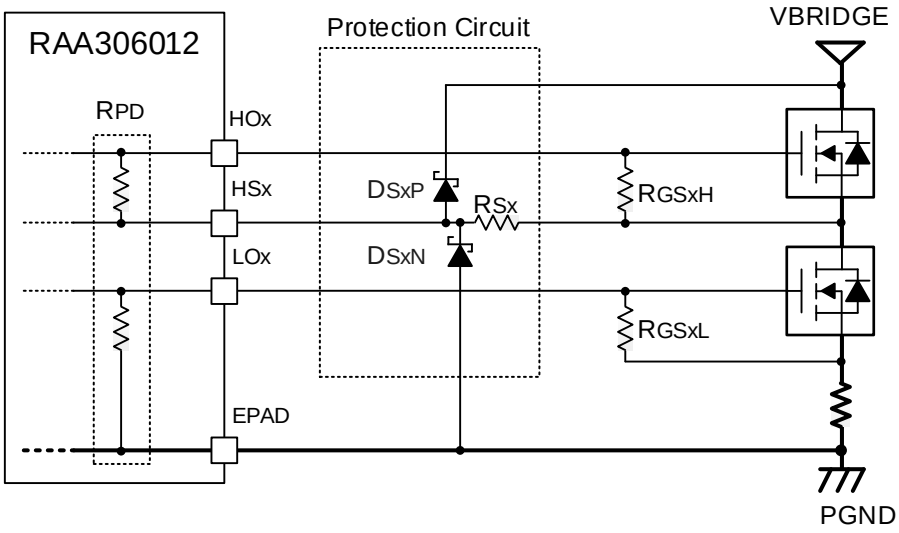


Figure 4-6 Example of Phase Voltage Clamp Circuit with 6 Resistors and Diodes (RSx, DSxP, DSxN (x = A, B, C))

4.1.7.2 Gate-Source Pull-down Resistors for External MOSFETs

This device has built-in pull-down resistors (R_{PD} = 200kΩ typ.) between the HOx and HSx (x = A, B, C) pins and between the LOx (x = A, B, C) and EPAD. After the EN output port is set to Low or a fault is detected, HOx and LOx (x = A, B, C) pins of the gate driver output become Hi-Z. These pull-down resistors (R_{PD}) discharge the gate-to-source voltage (V_{GS}) of external MOSFETs. For some fault detections related to external MOSFETs, the PDMODE bit can be used to select an operation that sets the gate driver to Low output. When an external MOSFET with a large input gate capacitance is used, the discharge time of gate-to-source voltage (V_{GS}) becomes longer. Then external pull-down resistors (RGSxH, RGSxL (x = A, B, C)) should be added as shown in ***Figure 4-7***.

Depending on the slew rate of the external MOSFETs power supply (VBRIDGE) at power-on, the gate voltage may rise due to the charging current of the gate-to-drain capacitance (C_{gd}) of the external MOSFET, causing a shoot-through current. On the other hand, while the external MOSFET is on, the HOx and LOx (x = A, B, C) pins at the output of the gate driver are High, which causes current to flow through the pull-down resistor and increases current consumption. Consider adding external pull-down resistors (RGSxH, RGSxL (x = A, B, C)) if necessary. The appropriate resistance value should be considered the discharge time, gate voltage rise, and current consumption corresponding to the operating conditions.

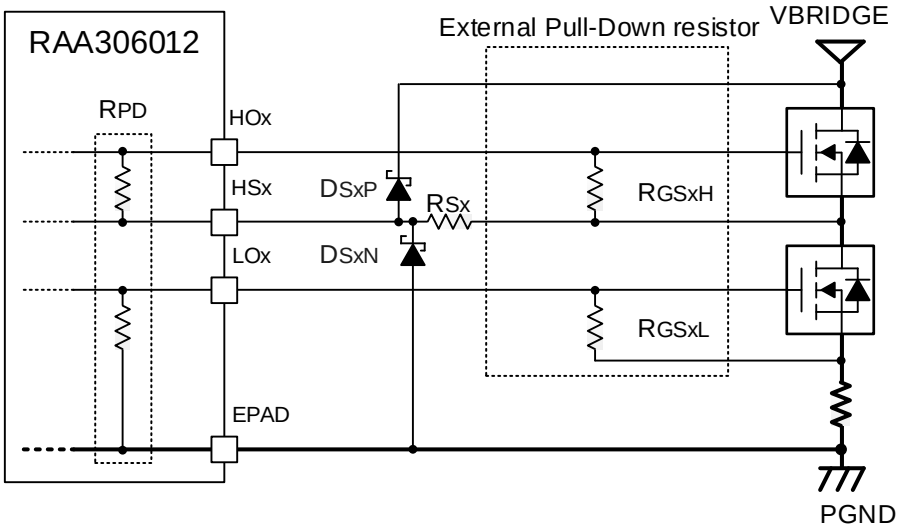


Figure 4-7 Gate-Source Pull-Down Resistors for External MOSFETs (RGSxH, RGSxL (x = A, B, C))

4.2 Board Layout Recommendations

In motor drive applications, a well-considered board layout is important for highly accurate analog signal detection, such as shunt current sensing signals and A/D converter input signals. Since motor drive applications including this device have a buck switching regulator that switches at high voltage and a gate driver that drives an external MOSFETs, pay attention to the classification of GND wiring, placement of external components, and wiring routing. This section describes the guidelines of each item for board layout.

4.2.1 GND Nets

This device uses four GND pins: EPAD, PGND, AGND, and GND_MCU. ***Table 5-3*** shows the blocks using each GND pin.

Table 4-3 Relationship Between 3 GND Nets and Related Blocks

GND	Block
EPAD	Gate driver, Charge pump
PGND	Gate driver
AGND	Differential amplifier, BEMF sense amplifier, General-purpose comparator, LDO, Buck switching regulator control block, Control logic block

Considering the above the GND separation in this device, it is recommended that the GND wiring be divided into 3 GND nets, which consist of PGND net (EPAD, PGND), AGND (AGND, GND_MCU), and REG_GND net. The REG_GND net is defined as the GND of the external components through which the switching current of the buck switching regulator flows. In addition, to avoid noise interference between GNDs, the common impedance with the GND planes of other GND nets should be as small as possible. The followings are precautions for each GND net wiring.

PGND Net

The PGND net is a GND plane that carries the gate discharge current of the external MOSFET associated with the switching of the half bridge. It is recommended that the PGND net be wired in a single layer without vias. The PGND pin and EPAD should be connected near this device without vias. If the wiring of PGND net in a single layer is difficult, connect the layers of the board with many vias to minimize parasitic inductance. Also, separate the wiring from the vicinity of the GND connector on the board (GND of the system) so that there is no common impedance with the GND on the half-bridge side. Since the peak gate discharge current exceeds 1A depending on the external MOSFET used and its switching characteristics (depending on the ISRC_LS bit), ensure that the wiring width is sufficient for the actual application. It is recommended that external components and circuits referenced to the PGND net be adequately covered by the GND plane of the PGND net to avoid noise effects on other blocks.

Since the EPAD is also used for heat dissipation of this device, it is recommended that EPAD be connected by a sufficient number of vias to allow heat dissipation to the rear of the board.

AGND Net

The AGND net is the reference GND plane for the built-in analog circuitry and the MCU. Therefore, it is important that the layout of the AGND net is designed to minimize the noise interference. The minimal overlap with the GND plane of other GND nets and with noisy power supply planes such as VM, VBRIDGE, and half-bridge power supplies is recommended. It is also recommended that external components and circuits referenced to the AGND net be adequately covered by the GND plane of the AGND net. The AGND net is used as a shield against wiring of high-precision analog signals such as shunt current sensing signals and A/D converter input signals.

REG_GND Net

The REG_GND net is the GND for external components through which the switching current of the buck switching regulator flows. To design a board layout that considers the noise countermeasure associated with the switching current of the buck switching regulator is one of the most important design items in applications that include switching power supplies. Since the switching current path changes depending on whether the switching element is on or off, it is recommended that a dedicated GND net (REG_GND) be provided for the GND of external capacitors (C1a, C1b), Schottky diode (D1), and output capacitor (C4) on the VDRV pin. It is important to place the GNDs of these components as close as possible to minimize noise due to parasitic inductance. Even if it is not possible to shorten the distance between the GNDs of external components, this wiring should be directly connected in a single layer.

The wiring from external components GND to the GND connector on the board (GND of the system) should be connected through vias to separate the REG_GND net from other GND nets. It is recommended that these vias be placed near the output capacitor (C4), where there is little current variation due to switching. It is also recommended that the external components and circuits of the buck switching regulator be sufficiently covered by a plane of the REG_GND net on a separate layer to suppress noise interference. Note that this plane must also be connected to the GND connector on the board (GND of the system) through a via to separate it from other GND nets.

4.2.2 Capacitors and Wirings for Power Supply Pins

This device has the following eight power supply pins, including the built-in regulator output pin. ***Table 4-4*** lists the bypass capacitors or output capacitors connected to each power supply pin, and the blocks using each pin. It is recommended that these capacitors be placed as close to this device as possible and be connected to this device in a single layer with low impedance without vias. The VM and VBRIDGE pins should be wired from near the power supply connector on the board (power supply of the system) where the voltage is relatively stable on the board, with consideration of the voltage drop. The followings are precautions to be considered when wiring power supplies, including half-bridge power supplies.

Table 4-4 Power Supply Pin Capacitors and Power Supply Destination Block

Power Supply Pins	Part No.	Power Supply Destination Blocks
VM – REG_GND	C1a, C1b	Buck switching regulator, LDO1
VBRIDGE – PGND	C1c, C1d	Gate driver
VCP – VBRIDGE	C2	Gate driver
VDRV – REG_GND	C4	Gate driver, LDO2, LDO3
VCC – AGND	C7	Differential amplifier, BEMF sense amplifier, General-purpose comparator, Buck switching regulator control block, Control logic block
VDD – AGND	C8	Differential amplifier, BEMF sense amplifier, General-purpose comparator

VM Pin Wiring

Like the wiring of REG_GND net, wiring to the power supply connector on the board (power supply of the system) is recommended to be connected on a separate layer with vias near the VM pin bypass capacitors (C1a, C1b). The purpose is to have the bypass capacitors (C1a, C1b) absorb the abrupt current changes that occur in the buck switching regulator as much as possible. The VM pin wiring should be independently connected to the power supply connector on the board even if it is used at the same potential as the VBRIDGE pin.

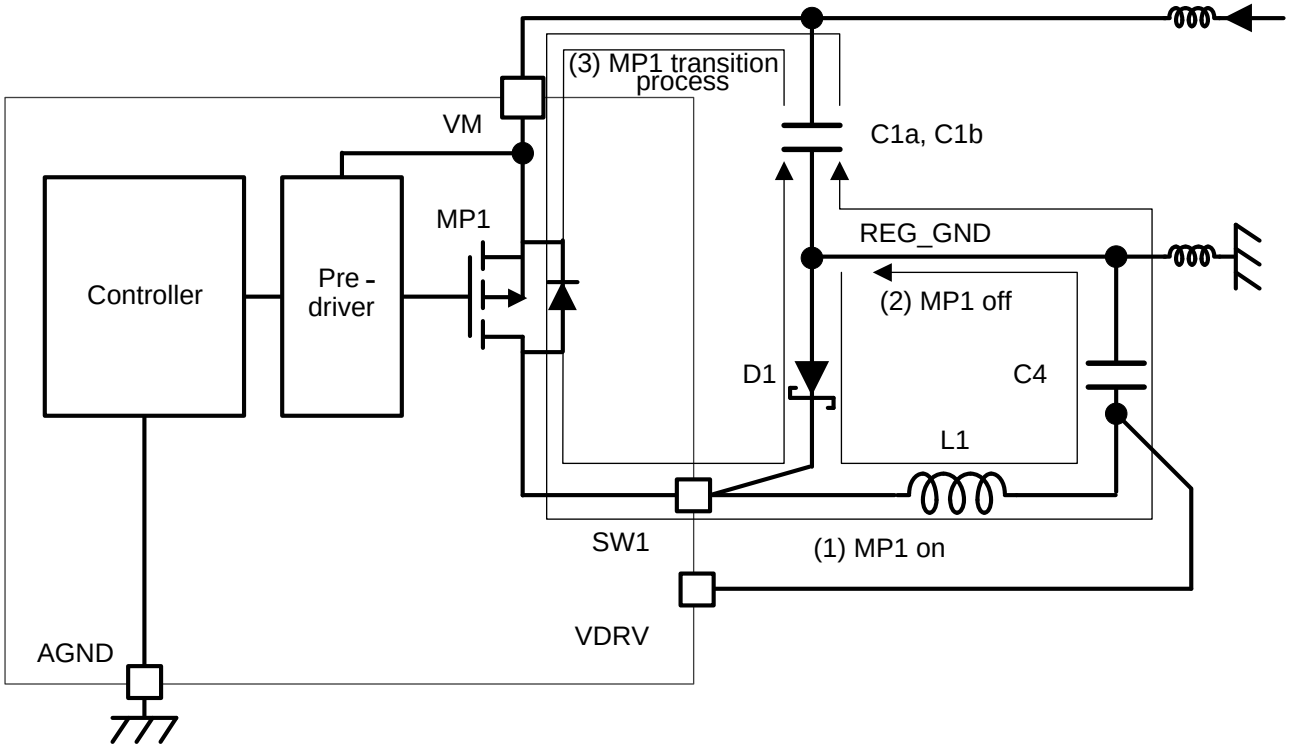
Half-bridge Power Supply, VBRIDGE Pin Wiring

To bypass the high current path of the external MOSFETs, electrolytic capacitors are usually added. These electrolytic capacitors are placed so that the length of the high current path through the external MOSFETs is minimized, considering the placement of the external MOSFETs and shunt resistors. Wiring should be designed to minimize parasitic inductance, with sufficient wiring width and enough vias connecting between layers of the board according to the actual application. Wiring to the bypass capacitors (C1c, C1d) at the VBRIDGE pin should be independent from the electrolytic capacitor terminals to minimize the common impedance with the high current path.

4.2.3 Buck Switching Regulator

The most important aspect of the board layout for the buck switching regulator is the minimization of noise generated by the switching regulator. As shown in ***Figure 4-8***, the buck switching regulator changes the switching current flow path according to the (1) the switching element (MP1) on, (2) MP1 off, and (3) MP1 transition process from off to on, and the steep current change at the switch timing of MP1 generates noise. To minimize this noise, it is required to minimize the area of the current loop in (3) shown in ***Figure 4-8.*** The followings are some points to be considered for minimizing the area of the current loop in (3). It is very important to connect the wiring between the external components of the buck switching regulator in a single layer without vias to minimize noise.

- Place VM pin capacitors (C1a, C1b) and Schottky diode (D1) as close as possible to this device and keep wiring between the elements and this device pins as short as possible.
- Make the REG_GND wiring between VM pin capacitors (C1a, C1b) and Schottky diode (D1) as short as possible.
  Also, consider the following precautions when implementing the board layout.
- Design the board layout so that the area of the current loop in (1) composed of the inductor (L1), output capacitor (C4), and Schottky diode (D1) is small.
- The wiring between the SW1 pin and the inductor (L1), and the REG_GND wiring between the Schottky diode (D1) and the output capacitor (C4) should be as short as possible, giving priority to the board layout for (3), because current flows continuously in the conditions (1) and (2).
- The wiring area (length and width) between the SW1 pin and the inductor (L1) should be small to the extent that it does not interfere with the current capacity and the heat generated by the inductor (L1).
- The wiring to VDRV pin should be wired from the land of the output capacitor (C4), not between the inductor



(L1) and the output capacitor (C4).

Figure 4-8 Current Path of the Buck Switching Regulator

4.2.4 N-ch MOSFET Bridge

The placing and wiring of the external MOSFETs should be considered to minimize the gate current loop that controls the on/off of the external MOSFETs. For high-side MOSFETs, it is recommended that the wiring from the MOSFETs gate to HOx (x = A, B, C) and from HSx (x = A, B, C) to the external MOSFETs source be shortened and parallel wiring. For low-side external MOSFETs, it is recommended that the wiring from the gate of the MOSFET to LOx (x = A, B, C) and from EPAD to the GND side of the shunt resistors be shortened and parallel wiring.
Note that the gate-drive sink (discharge) currents (I_{SNKH}, I_{SNKL}) exceed1A depending on the external MOSFET used and the switching characteristics (ISRC_HS, ISRC_LS bit dependent). Ensure sufficient wiring width considering the peak current for the actual application. In addition, to avoid mismatch with respect to the propagation delay of the half-bridge output, the placing and wiring of external components in each phase should be as symmetrical as possible.

4.2.5 Charge Pump

Place the pumping capacitor (C3) and the output capacitor (C2) of the charge pump as close to this device as possible, and make the loop caused by the wirings of CPH and CPL to the C3 as small as possible. The loop caused by the wirings of VCP and VBRIDGE to C2 should be as small as possible. Since these wirings are subject to large current variations during charging and pumping operations, it is recommended that they be connected in a single layer without vias. Note that the wiring loop to C3 and the wiring loop to C2 should be sufficiently covered by a GND plane in the PGND net.

4.2.6 Shunt Current Sensing

For current sensing by the shunt resistors (R1, R2, R3), it is recommended that the wirings be used Kelvin connections and connected to the differential amplifier input DAzP and DAzN (z = 1, 2, 3) pins with parallel and equal length to accurately detect the differential voltages across the shunt resistors. To avoid noise interference to the differential wirings, it is also recommended to provide shields on both sides, upper, and lower layers of the AGND net. It is recommended that wirings be done as far away from noise sources such as the wirings of power supply and Hall IC output as possible. An R-C filter can be inserted just before the differential input DAzP and DAzN (z = 1, 2, 3) pins for the purpose of noise reduction, but these pins have an input impedance of 10kΩ, so use a resistor of 20Ω or less to prevent gain errors. Also, when inserting R-C filters, select an appropriate cut-off frequency by fully considering the timing of the signals to be detected and the delay time due to the R-C filter.

Chapter 5 Precautions for Use

5.1 High Temperature Operation

The following operating temperature profile is assumed for the usage of this device. Please take the use within this profile into consideration.

High ambient temperature environment 1:	85°C < Ta ≤ 125°C, 1.0 hr/day
High ambient temperature environment 2:	55°C < Ta ≤ 85°C, 4.0 hrs/day
Not high ambient temperature environment:	-40°C ≤ Ta ≤ 55°C, 19.0 hrs/day

Revision History

Revision	Date	Description	Object Page
1.00	1-Sep-23	• Initial release.	• All

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