

Renesas RX and RA families

Design Guide for Main Clock Circuits and Sub Clock Circuits

Introduction

This application note introduces recommended resonators for the RX and RA families along with the relevant resonator matching evaluation results, oscillation evaluation methods, and some recommendations on board design as information for the design of the main clock oscillation circuit and the sub-clock oscillation circuit.

Target Device

RX and RA families

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1. Using the Application Note

This application note is intended for those who are considering how to select or evaluate an external resonator connected to RX and RA microcontroller (MCU) device families. Since it is difficult to select the optimal resonator yourself, we recommend that you ask the resonator manufacturer to perform the matching evaluation. For details, see each chapter.

- Chapter 2: This Chapter provides information on the external components connected to the RX and RA families clock systems.
- Chapter 3: This chapter introduces resonator manufacturers who have performed resonator matching evaluations with RX and RA and explains how to search for suitable resonators for RX and RA on their website (Tool). If you wish to select a resonator that has already been evaluated, refer to this chapter.
- Chapter 4: This chapter describes the resonator characteristics and provides information on the proposed components mounted on the board based on the evaluation. Refer to this chapter if you want to narrow down the resonator selection conditions.
- Chapter 5: This chapter describes how to select and evaluate external components to stabilize oscillation.
- Chapter 6: This chapter describes the key points of the board design. Read this chapter before designing a board.
- Chapter 7: This chapter describes the method for measuring clock frequency accuracy on MCU board products.

2. Connecting External Components

Most RX and RA MCUs support the use of a ceramic or crystal resonator as the main clock source, as shown in Figure2.1. This should be connected between EXTAL and XTAL pins of the MCU. Note that for some MCU groups, the pin names EXTAL and XTAL may be replaced with X2 and X1. A crystal resonator can be used as the sub-clock source, which should be connected between XCIN and XCOUT pins of the MCU.

The frequency of the external resonator for the main clock source should be within the range specified as the oscillator frequency of the main clock oscillator of the MCU. The frequency of the external resonator for the sub-clock source must be exactly 32.768 kHz. For details, refer to "Electrical Characteristics" and "Clock Generation Circuit" in the MCU User's Manual: Hardware.

The damping register (R_d) and the load capacitors (C_{L1} , C_{L2}) are typically specified by the resonator manufacturer, and must be implemented as external components. When selecting external components, we recommend that you contact the resonator manufacturer for a matching evaluation. If you prefer to calculate suitable capacitances by yourself, refer to Chapter 5 "Oscillation Evaluation and Oscillation Circuit Constant Calculation Method".

Since RX and RA MCU have a built-in feedback resistor, it is not necessary to implement the feedback resistor (*) shown in Figure2.1. However, if the resonator manufacturer recommends implementing the feedback resistor, follow the resonator manufacturer's instructions.

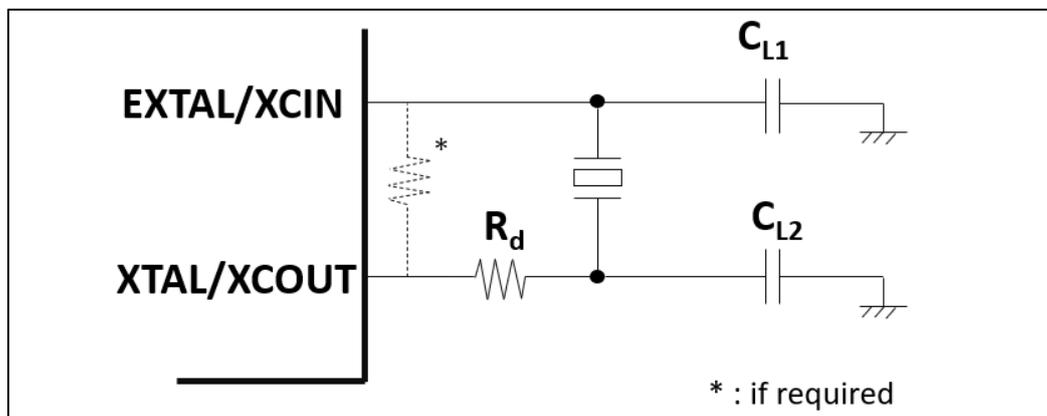


Figure2.1 Connection Example of External Resonator

3. Introduction of resonator manufacturers that Renesas has requested matching evaluations from

Several resonator manufacturers have performed evaluations of the RX and RA family's oscillator circuits, and publish a list of suitable resonators for some of the RX or RA families. Table 3.1 Example Resonator List with Matching Evaluated shows some examples of resonators for which an evaluation has been performed. For the latest information, visit the resonator manufacturers' website.

If you cannot find the targeted MCU on the oscillator manufacturer's website :

Search for the target MCU from Table 4.1 and then Search the MCUs in the same group on the oscillator manufacturer's web.

Table 3.1 Example Resonator List with Matching Evaluated

Manufacturer	Resonator/Part Number	Oscillation frequency	Circuit-load capacitance (pF)	C _{L1} (pF)	C _{L2} (pF)	R _d (ohm)	MCU group name
Kyocera Corporation	CX3225CA12000D0PRTC2	12 MHz	6.49	10	10	4700	RX72T, RX66T
Murata Manufacturing	XRCGB24M000F3M26R0	24 MHz	6	8	8	0	RX72M, RX72N, RX66N, RX671
NIHON DEMP A KOGYO CO., LTD.	STD-MUA-9	32.768 kHz	9	12	12	0	RX660
Seiko Instruments Inc.	SSP-T7-F	32.768 kHz	12.5	22	22	0	RA2L1
DAISHINKU CORP.	DSX211SH	20Hz	8	Open	Open	0	RA0E1

The following shows how to search for a resonator matching the RX and RA families on the resonator manufacturers' website.

■ Kyocera Corporation:Search Page: [Crystal Units vs. IC Matching Search](#)

- 1) Select "Renesas Electronics" from the dropdown of IC Manufacturers.
- 2) Select the group-name from the dropdown of IC family.
Ex.) IC family: RX72N
- 3) Press the search button. The corresponding data is displayed.

■ Murata Manufacturing Co., Ltd.Search page: [IC-Timing Device Search Tool](#)

- 1) Select "Renesas Electronics" from the dropdown of IC manufacturers.
- 2) Select the group name from the dropdown of IC Part Numbers.
Ex.) IC Part Number: RX72N
- 3) Press the search button. The corresponding data is displayed.

■ NIHON DEMPA KOGYO CO., LTD.:Search page: [IC Matching Information](#)

- 1) Select "Renesas Electronics" in Supplier Name checkboxes.
- 2) Click the PDF icon in the row whose Families/Series is the group you want to know about.
Ex) Select RX660.
The corresponding data is displayed.

■ Seiko Instruments Inc.:Search page: [IC Matching Information](#)

- 1) Click the group name you want to know about. The corresponding data is displayed.

■ DAISHINKU CORP.Search page: [IC Manufacturer Information](#)

- 1) In the IC Manufacturer field, locate Renesas and verify the desired family/product group name.

The matching parameters of the oscillator circuit published on the website of the resonator manufacturers are the experimental results of some samples under certain conditions, and Renesas do not guarantee them. Optimal parameters may be different for each user's actual system. Renesas recommends that users contact the resonator manufacturers for a matching evaluation of their specific system to determine the oscillator circuit parameters required.

The operating conditions of the MCU described on their website are used to stabilize the oscillation of their resonator in the evaluation and are not the recommended conditions by Renesas. For the recommended operating conditions for MCU, refer to "Electrical Characteristics" in MCU User's Manual: Hardware.

4. Matching evaluation result

In this chapter, we present the matching evaluation results that Renesas commissioned multiple oscillator manufacturers to perform. The MCUs are categorized into groups as shown in Table4.1, and the subsequent chapters describe the drive capability settings for the main clock and sub-clock circuits, the characteristics of the oscillators (frequency, CL), the implementation details of the evaluation boards (Rd, CL1, CL2), and the evaluation results (negative resistance, recommended ESR, V_{oh}^1 , V_{ol}^1).

Note that these results are based on evaluation with a limited number of samples and are not guaranteed under all conditions.

Table4.1 matching evaluation Group

Group	RX	RA
1	RX65N, RX651, RX671, RX66N, RX72N and RX72M	RA4M2, RA4M3, RA4E1, RA4E2 ² , RA4T1 ² , RA6M1, RA6M2, RA6M3, RA6M4, RA6M5, RA6T1, RA6T2 ³ , RA6T3 ³ , RA6E1 and RA6E2 ²
2	RX26T ³ , RX660, RX66T ³ and RX72T ³	N/A
3	RX64M and RX71M	N/A
4	RX130, RX13T ³ , RX230, RX231, RX23E-A ³ , RX23E-B, RX23T ³ , RX23W, RX24T ³ and RX24U ³	RA2A1, RA4M1 and RA4W1
5	RX111, RX110 and RX113	N/A
6	RX140	N/A
7	N/A	RA2E1, RA2E3, RA2A2, RA2L1, RA2L2 and RA2T1
8	N/A	RA8M1, RA8D1, RA8T1, RA8E1 and RA8E2
9	N/A	RA0E1, RA0E2 and RA0L1
10	N/A	RA8P1, RA8M2, RA8D2 and RA8T2

1: V_{oh} , V_{ol} of the sub-clock cannot be measured when a probe is touched to the clock terminals, so there is no evaluation result.

2: 32-pin LQFP and QFN part numbers do not support their sub-clock oscillator function.

3: These groups do not include a sub-clock oscillator.

4.1 Matching evaluation result (Main clock circuit)

4.1.1 Group1

The matching evaluation results of Group 1 are shown below.

Table 4.1.1 Group 1, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting ⁴	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V _{oh}	V _{ol}
8MHz	8	8	0	8	8	-3,760	750	2.56	-0.04
8.1 to 16MHz	12	8	0	6	6	-2,150	430	2.48	0
8.1 to 16MHz	16	8	0	6	6	-1,120	220	2.44	0
16.1 to 20MHz	20	8	0	8	8	-1,020	200	2.52	0
16.1 to 20MHz	24	8	0	6	6	-1,320	260	2.48	-0.08
20.1 to 24MHz	24	6	680	4	4	-1,650	330	-	-
20.1 to 24MHz	24	8	0	6	6	-1,320	260	2.42	-0.04
20.1 to 24MHz	24	8	1000	8	8	-380	70	1.94	0.6
20 to 24MHz	24	8	0	0	0	-1,550	310	3.2	0.4

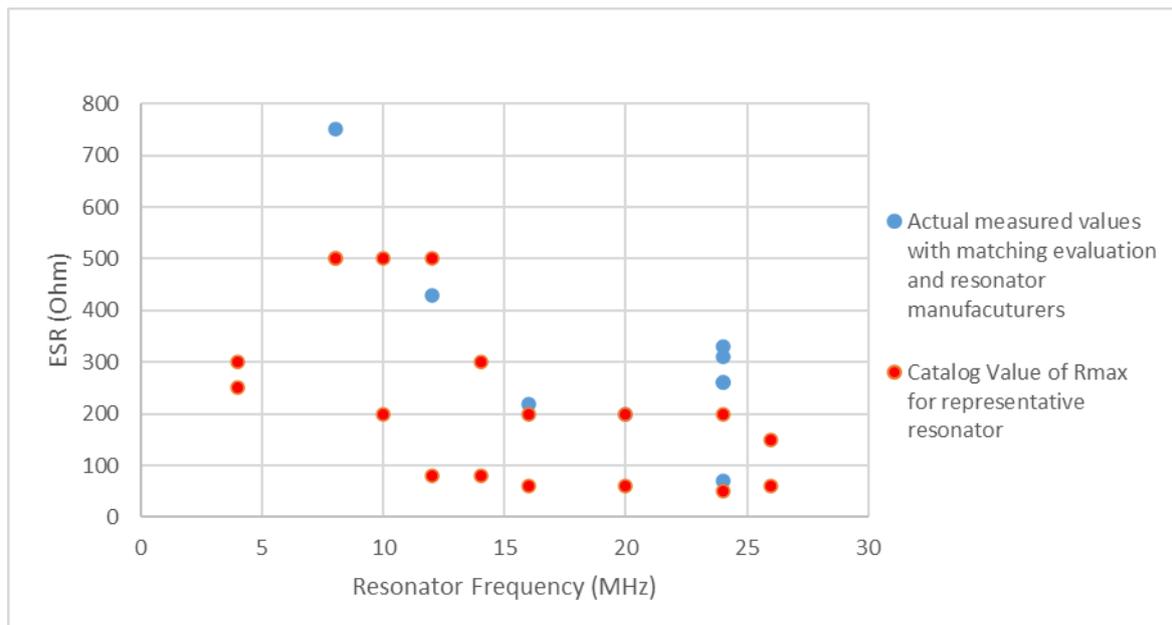


Figure 4.1.1 Group 1, Main clock: Resonator Frequency vs ESR max

4.1.2 Group2

The matching evaluation results of Group 2 are shown below.

Table 4.1.2 Group 2, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting ⁴	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V _{oh}	V _{ol}
8.1 to 16MHz	10	8	4700	12	12	-1,150	230	2.24	0.24
8.1 to 16MHz	12	8	4700	10	10	-830	160	2.14	0.32
8.1 to 16MHz	16	8	3900	9	9	-440	80	2	0.48
20.1 to 24MHz	20	8	3300	10	10	-320	60	1.98	0.52
20.1 to 24MHz	24	6	470	8	8	-1,850	370	-	-

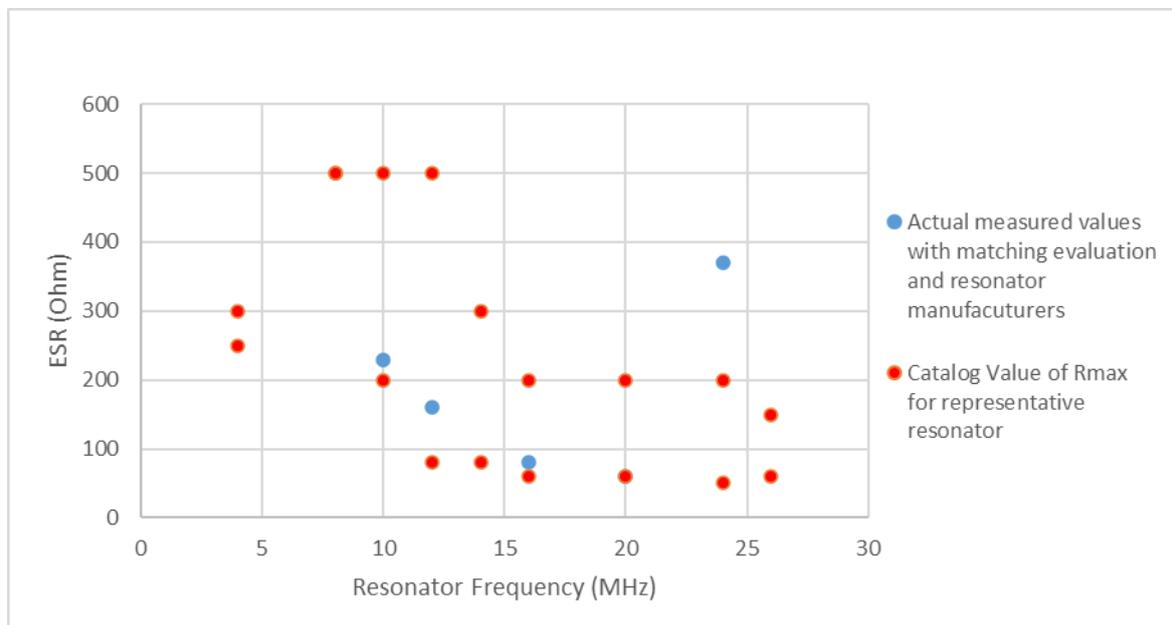


Figure 4.1.2 Group 2, Main clock: Resonator Frequency vs ESR max

4.1.3 Group3 and Group5

The matching evaluation results of Group 3 and Group5 are shown below.

Table 4.1.3 Group 3 and Group5, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting ⁴	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V _{oh}	V _{ol}
8MHz	8	8	0	8	8	-5,760	1,150	-	-
8.1 to 16MHz	16	8	1000	7	7	-1,520	300	-	-
16.1 to 20MHz	20	8	1000	7	7	-1,020	200	-	-
20.1 to 24MHz	24	8	1000	7	7	-860	170	-	-

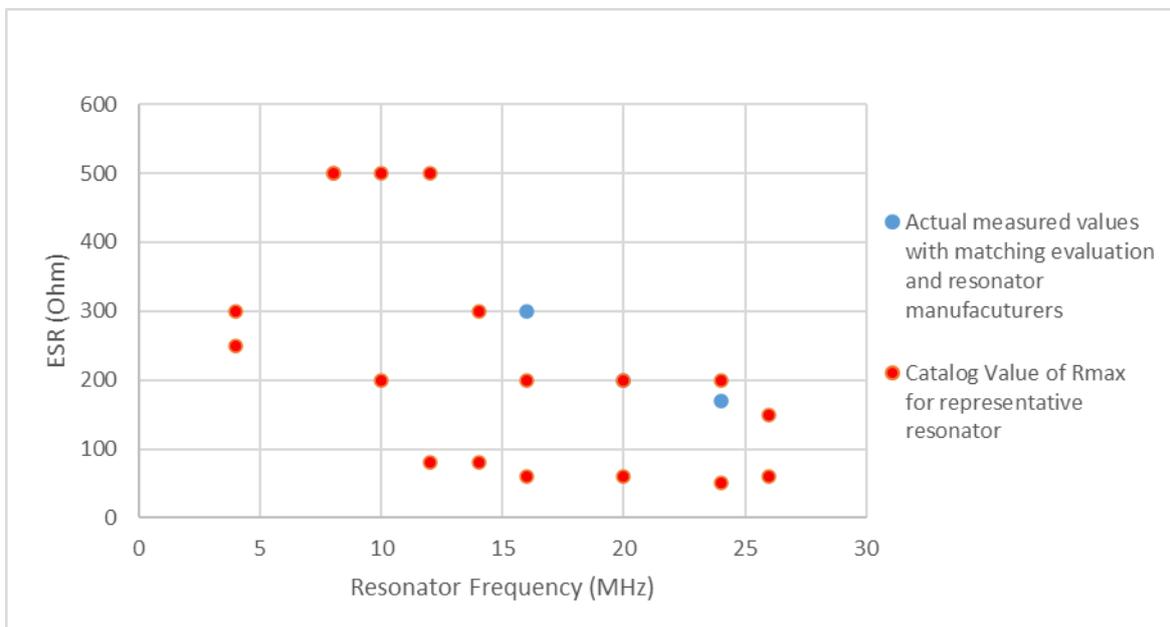


Figure 4.1.3 Group 3 and Group 5, Main clock: Resonator Frequency vs ESR max

4.1.4 Group4

The matching evaluation results of Group 4 are shown below.

Table 4.1.4 Group 4, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting ⁴	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V _{oh}	V _{ol}
1 to 8MHz	4	8	0	8	8	-2,500	500	-	-
1 to 10MHz	4	8	0	9	9	-2,900	580	-	-
1 to lower than 10MHz	4	8	0	8	8	-3,310	660	-	-
10 to 20MHz	10	8	0	6	6	-1,010	200	-	-
10 to 20MHz	12	8	0	9	9	-670	130	-	-
10 to 20MHz	16	8	0	9	9	-360	70	-	-

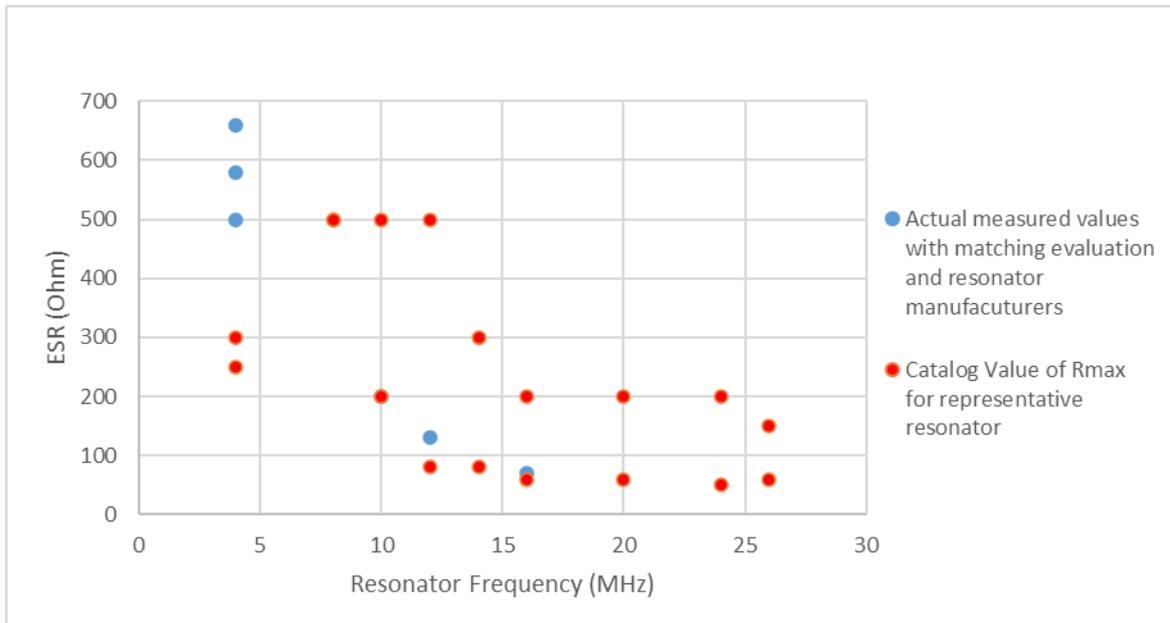


Figure 4.1.4 Group 4, Main clock: Resonator Frequency vs ESR max

4.1.5 Group6

The matching evaluation results of Group 6 are shown below.

Table 4.1.5 Group 6, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting ⁴	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V _{oh}	V _{ol}
1 to 10MHz	8	6	220	5	5	-4,660	930	-0.08	1.54
1 to 10MHz	8	6	330	5	5	-3,440	680	1.58	0.02
1 to 10MHz	8	8	0	8	8	-3,370	670	-	-
1 to 10MHz	10	8	0	8	8	-2,350	470	-	-
10 to 20MHz	10	8	0	8	8	-3,250	650	-	-
10 to 20MHz	12	8	0	8	8	-2,330	460	-	-
10 to 20MHz	16	8	0	9	9	-1,350	270	1.45	-0.01
10 to 20MHz	20	5	220	3	3	-1,700	340	-0.02	1.5
10 to 20MHz	20	5	330	5	5	-1,150	230	1.48	-0.04
10 to 20MHz	20	8	0	8	8	-900	180	-	-

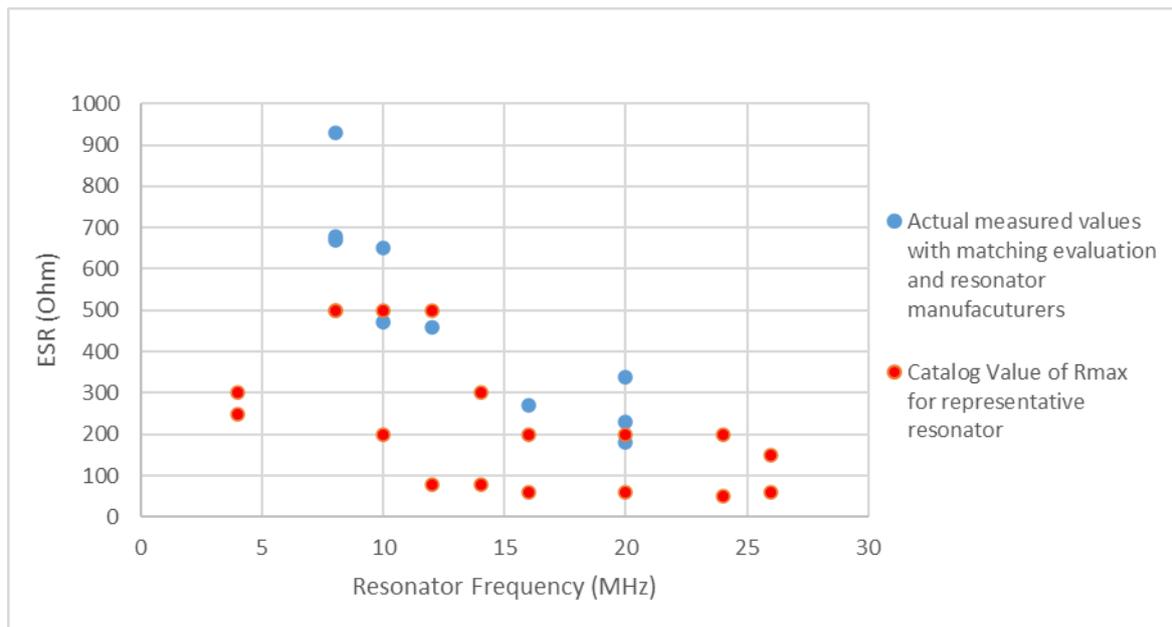


Figure 4.1.5 Group 6, Main clock: Resonator Frequency vs ESR max

4.1.6 Group7

The matching evaluation results of Group 7 are shown below.

Table 4.1.6 Group 7, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting ⁴	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V _{oh}	V _{ol}
1 to 10MHz	8	8	0	8	8	-2,860	570	1.52	0.04
1 to 10MHz	8	8	2200	3	4	-3,360	670	1.54	-0.04
10 to 20MHz	12	8	0	8	8	-2,060	410	1.58	-0.16
10 to 20MHz	16	8	0	8	8	-1,240	240	1.56	-0.09
10 to 20MHz	20	5	470	4	4	-1,360	270	1.53	-0.02
10 to 20MHz	20	8	0	12	12	-470	90	1.57	-0.09

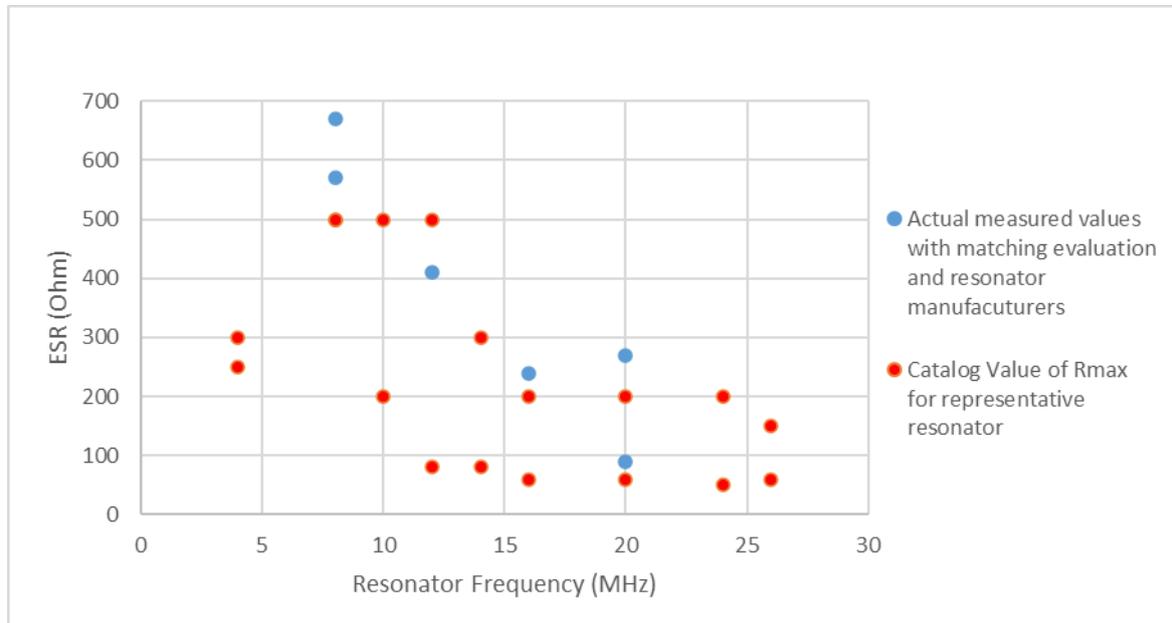


Figure 4.1.6 Group 7, Main clock: Resonator Frequency vs ESR max

4.1.7 Group8

The matching evaluation results of Group 8 are shown below.

Table 4.1.7 Group 8, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting ⁴	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V _{oh}	V _{ol}
8 to 24MHz	8	8	0	4	4	-10,270	2,050	-	-
8 to 24MHz	16	8	0	4	4	-2,730	540	-	-
8 to 24MHz	20	8	0	4	4	-3,020	600	-	-
8 to 24MHz	24	8	0	4	4	-3,620	720	-	-
8 to 48MHz	8	8	0	4	4	-8,970	1,790	-	-
8 to 48MHz	16	8	0	4	4	-2,330	460	-	-
8 to 48MHz	20	8	0	4	4	-2,220	440	-	-
8 to 48MHz	24	8	0	4	4	-1,820	360	-	-

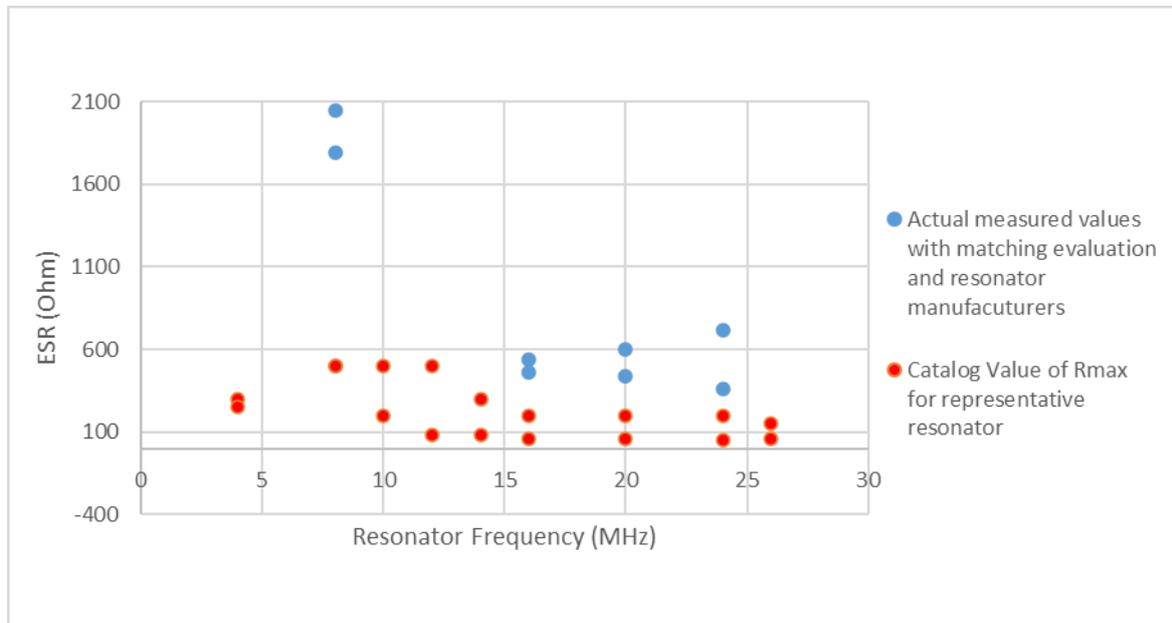


Figure 4.1.7 Group 8, Main clock: Resonator Frequency vs ESR max

4.1.8 Group9

The matching evaluation results of Group 9 are shown below.

Table 4.1.8 Group 9, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting ⁴	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V _{oh}	V _{ol}
1 to 10MHz	8	6	0	NM	NM	-3,270	650	-	-
1 to 10MHz	8	8	0	NM	NM	-3,000	600	1.61	-0.02
1 to 10MHz	10	8	0	1	1	-2,130	420	-	-
10 to 20MHz	12	8	0	4	4	-1,500	300	1.63	-0.09
10 to 20MHz	16	8	0	NM	NM	-910	180	1.64	-0.06
10 to 20MHz	20	8	0	4	4	-560	110	1.64	-0.02

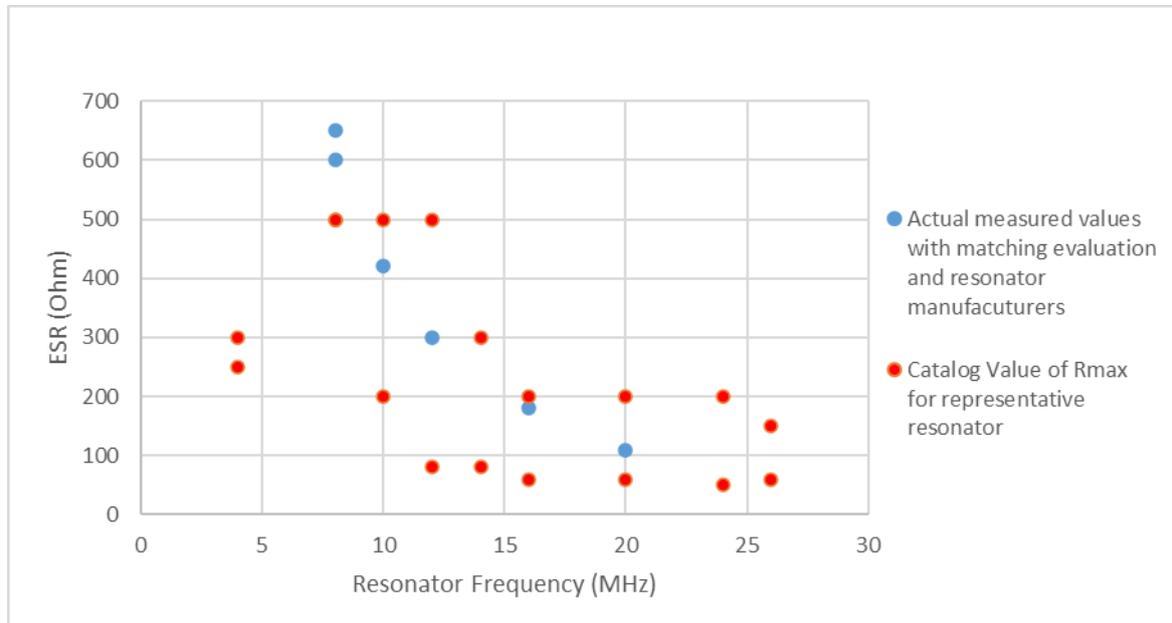


Figure 4.1.8 Group 9, Main clock: Resonator Frequency vs ESR max

4.1.9 Group10

The matching evaluation results of Group 10 are shown below.

Table 4.1.9 Group 10, Main clock: Results of the matching evaluation

Main Clock Oscillator Driving Setting ⁴	Resonator specification		Evaluation board implementation			Evaluation results			
	Frequency (MHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (Ohm)	Recommended ESR_max (Ohm)	V _{oh}	V _{ol}
8MHz	10	8	0	8	8	-4,600	920	0.80	0.02
8 to 24 MHz	12	8	0	7	7	-1,860	370	0.72	0.08
8 to 24 MHz	12	10	0	10	10	-820	160	1.1	0
8 to 24MHz	16	8	0	8	8	-1,770	350	0.72	0.11
8 to 24 MHz	16	5	0	5	5	-1,800	360	1.1	0
8 to 24MHz	20	8	0	8	8	-1,110	220	0.75	0.08
8 to 24 MHz	20	5	0	5	5	-1,200	240	-	-
8 to 24MHz	24	6	0	8	8	-1,050	210	-	-

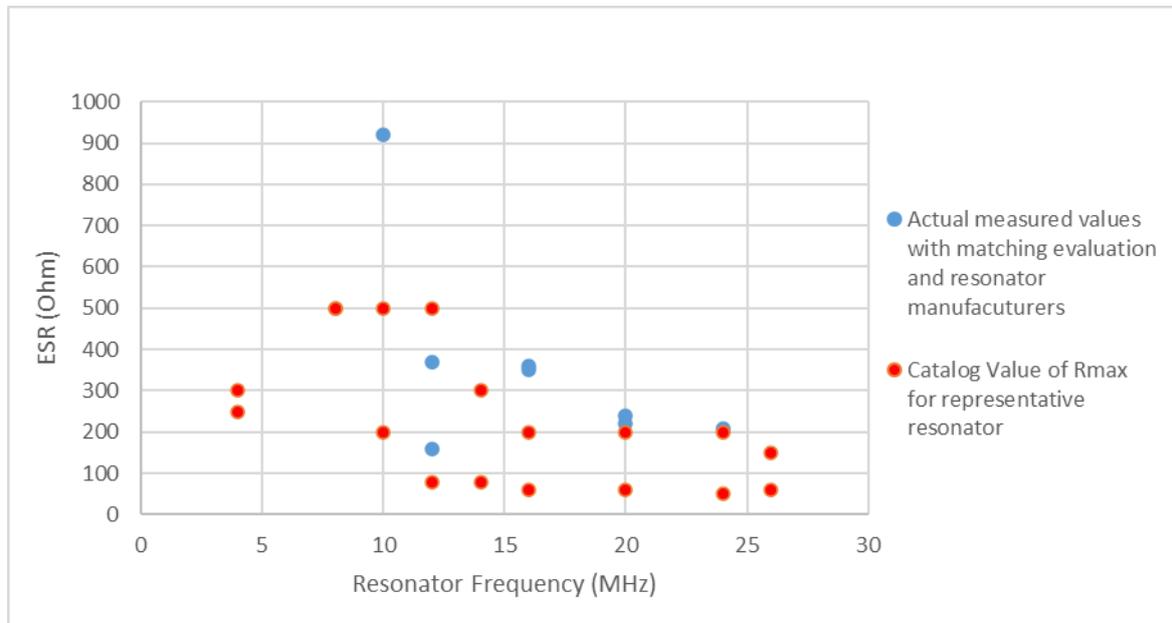


Figure 4.1.9 Group 10, Main clock: Resonator Frequency vs ESR max

4.2 Matching evaluation result (Sub clock circuit)

4.2.1 Group 1

The matching evaluation results of Group 1 are shown below.

Table 4.2.1 Group 1, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR _{max} (kOhm)
Low CL ⁶	32KHz	4	0	4.3	4.3	-510	100
Low CL ⁶	32KHz	4.4	0	6	5	-340	60
Low CL ⁶	32KHz	5	0	6	6	-370	70
Low CL ⁶	32KHz	6	0	8	8	-240	40
Standard CL ⁶	32KHz	7	0	12	12	-1,250	250
Standard CL ⁶	32KHz	9	0	15	15	-840	160
Standard CL ⁶	32KHz	12.5	0	24	24	-430	80

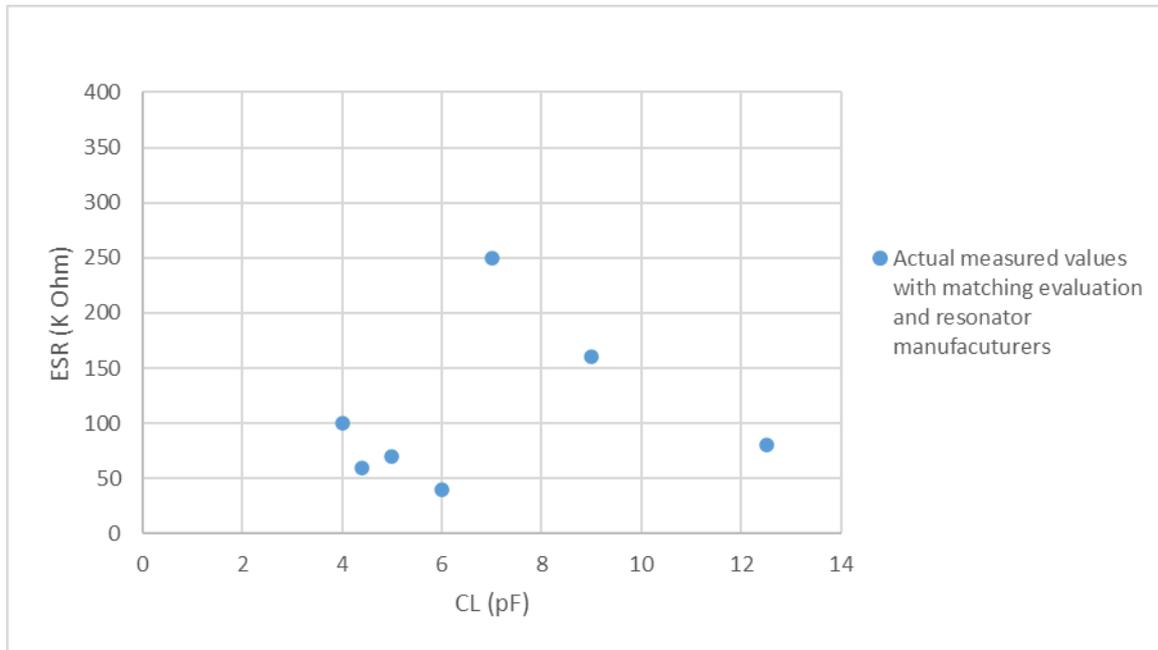


Figure 4.2.1 Group 1, Sub-clock: C_L vs ESR max

4.2.2 Group 2

The matching evaluation results of Group 2 are shown below.

Table 4.2.2 Group 2, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR _{max} (kOhm)
Standard CL ⁶	32KHz	7	0	10	10	-930	180
Standard CL ⁶	32KHz	9	0	15	15	-540	100
Standard CL ⁶	32KHz	12.5	0	18	22	-310	60

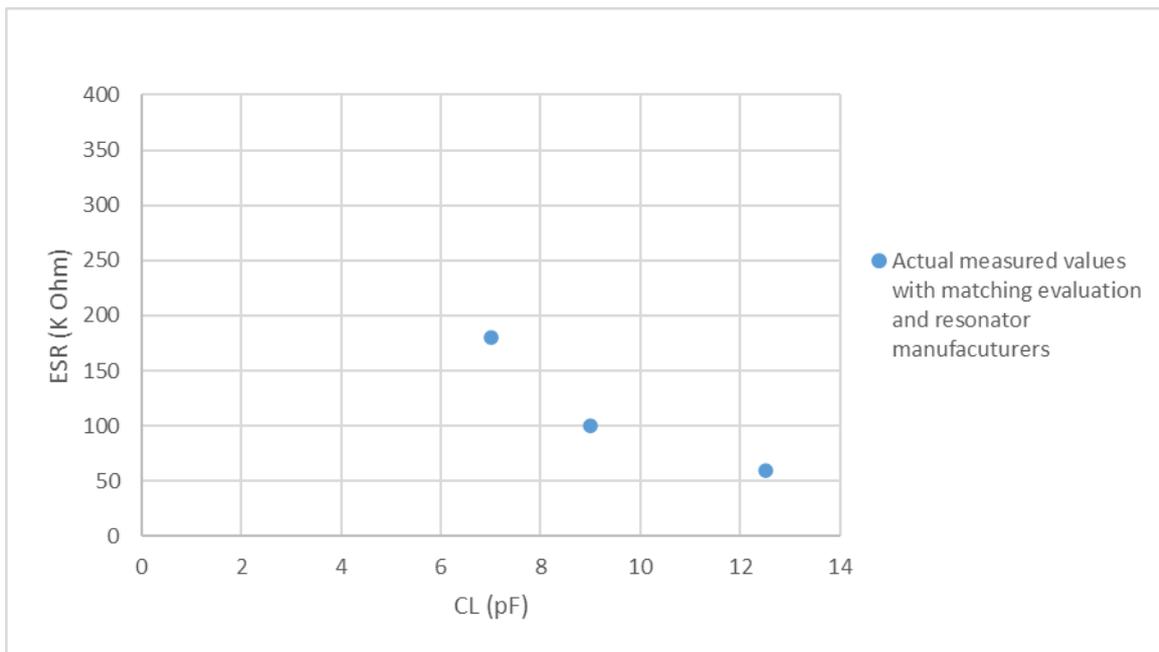


Figure 4.2.2 Group 2, Sub-clock: C_L vs ESR max

4.2.3 Group 3

The matching evaluation results of Group 3 are shown below.

Table 4.2.3 Group 3, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR_max (kOhm)
Low CL ⁶	32	4	0	2	3	-570	110
Low CL ⁶	32	3.7	0	3	3	-430	80
Standard CL ⁶	32	7	0	9	9	-1,000	200
Standard CL ⁶	32	12.5	0	22	22	-350	70

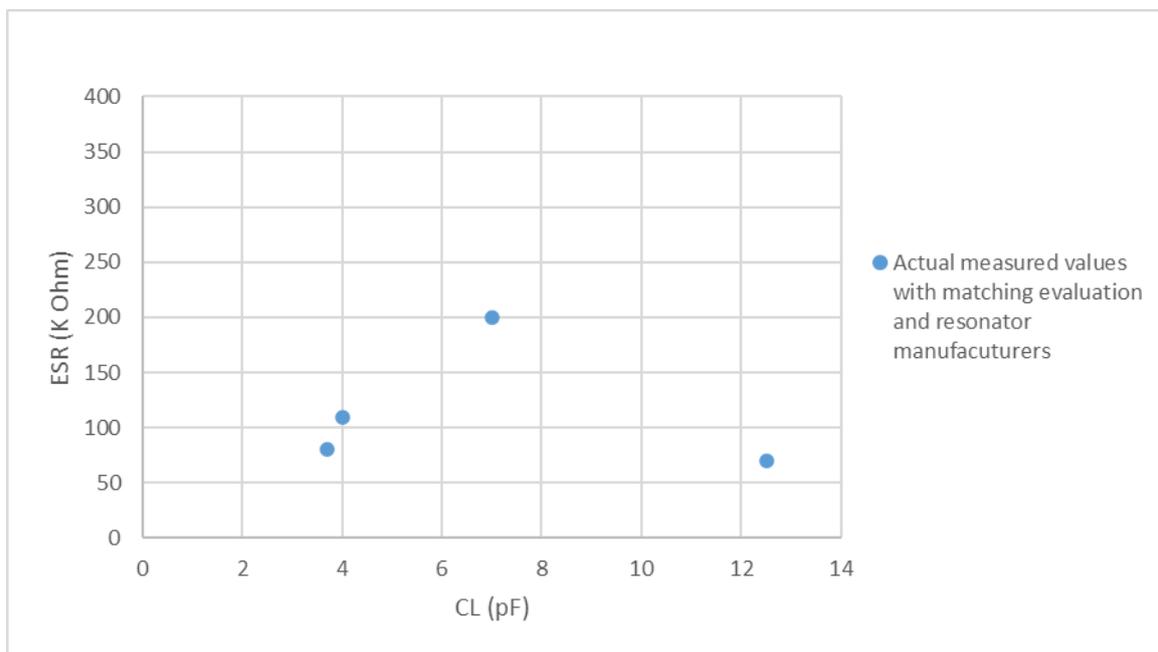


Figure 4.2.3 Group 3, Sub-clock: C_L vs ESR max

4.2.4 Group 4

The matching evaluation results of Group 4 are shown below.

Table 4.2.4 Group 4, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR_max (kOhm)
Low CL ⁶	32	4	0	5	5	-2,320	460
Low CL ⁶	32	6	0	9	9	-1,060	210

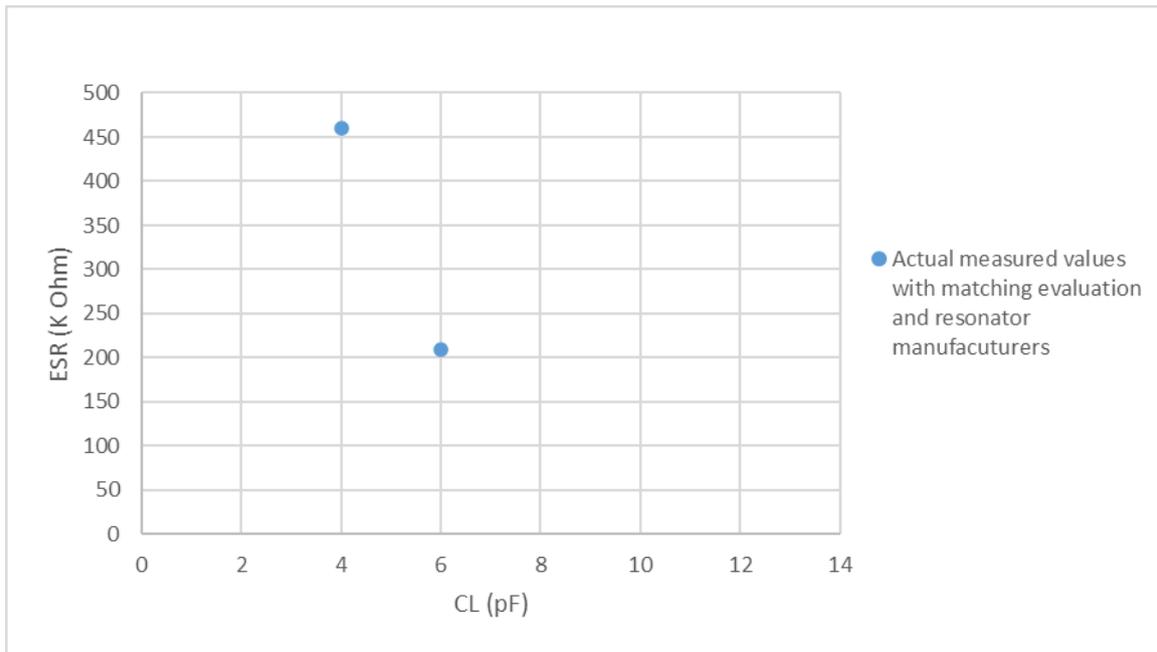


Figure 4.2.4 Group 4, Sub-clock: C_L vs ESR max

4.2.5 Group 5

The matching evaluation results of Group 5 are shown below.

Table 4.2.5 Group 5, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR_max (kOhm)
Low CL, high drive capacity ⁶	32	6	0	8	8	-740	140
Low CL, high drive capacity ⁶	32	7	0	10	12	-450	90
Low CL, low drive capacity ⁶	32	4.4	0	5	6	-600	120
Low CL, low drive capacity ⁶	32	6	0	9	9	-340	60
Low CL, low drive capacity ⁶	32	3.7	0	4	4	-860	170
Low CL, medium drive capacity ⁶	32	4.4	0	5	6	-1,050	210
Low CL, medium drive capacity ⁶	32	6	0	9	9	-550	110
Low CL, medium drive capacity ⁶	32	7	0	10	12	-320	60

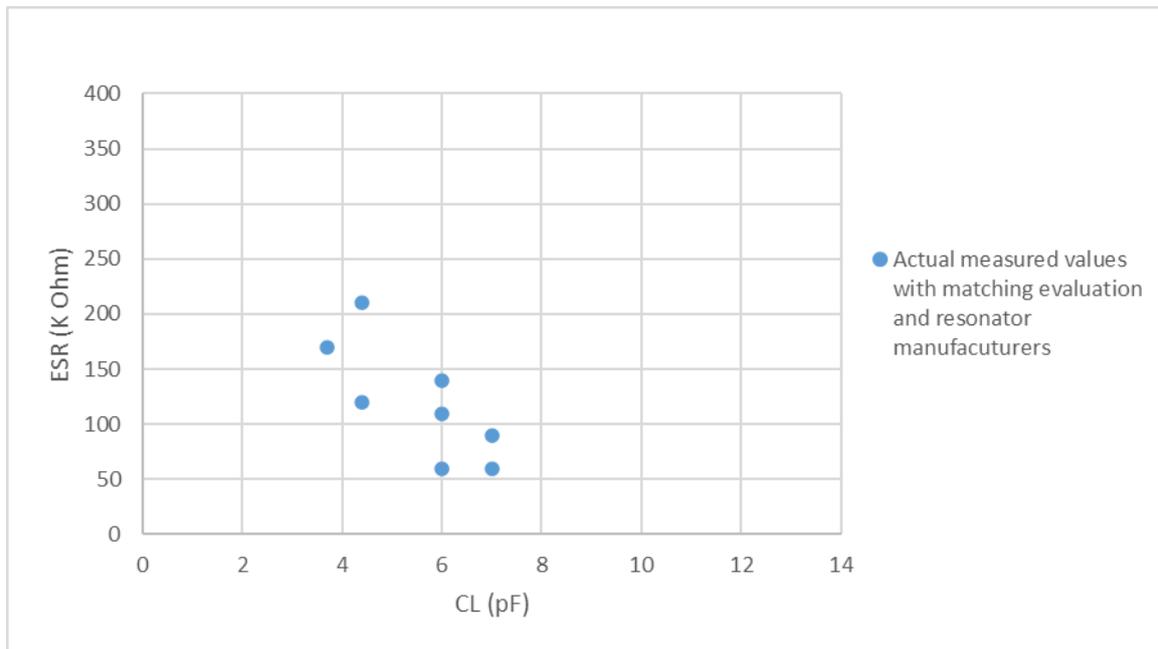


Figure 4.2.5 Group 5, Sub-clock: C_L vs ESR max

4.2.6 Group 6

The matching evaluation results of Group 6 are shown below.

Table 4.2.6 Group 6, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR _{max} (kOhm)
Standard CL ⁶	32	6	0	7	7	-1,340	260
Standard CL ⁶	32	9	0	16	15	-760	150
Standard CL ⁶	32	12.5	0	22	22	-420	80
Standard CL ⁶	32	7	0	9	10	-1,370	270
Standard CL ⁶	32	9	0	15	18	-580	110
Standard CL ⁶	32	12.5	0	22	22	-440	80
Low CL, high drive capacity ⁶	32	6	0	7	7	-610	120
Low CL, high drive capacity ⁶	32	7	0	10	10	-590	110
Low CL, high drive capacity ⁶	32	9	0	15	15	-350	70
Low CL, high drive capacity ⁶	32	6	0	7	8	-890	170
Low CL, high drive capacity ⁶	32	7	0	9	10	-490	90
Low CL, midium drive capacity ⁶	32	6	0	7	7	-300	60
Low CL, midium drive capacity ⁶	32	6	0	7	7	-410	80
Low CL, low drive capacity ⁶	32	4	0	3	3	-300	60
Low CL, low drive capacity ⁶	32	6	0	2	2	-290	50
Low CL, low drive capacity ⁶	32	3.7	0	2	3	-340	60
Low CL, low drive capacity ⁶	32	4	0	3	3	-360	70
Low CL, low drive capacity ⁶	32	3.7	0	3	2	-380	70

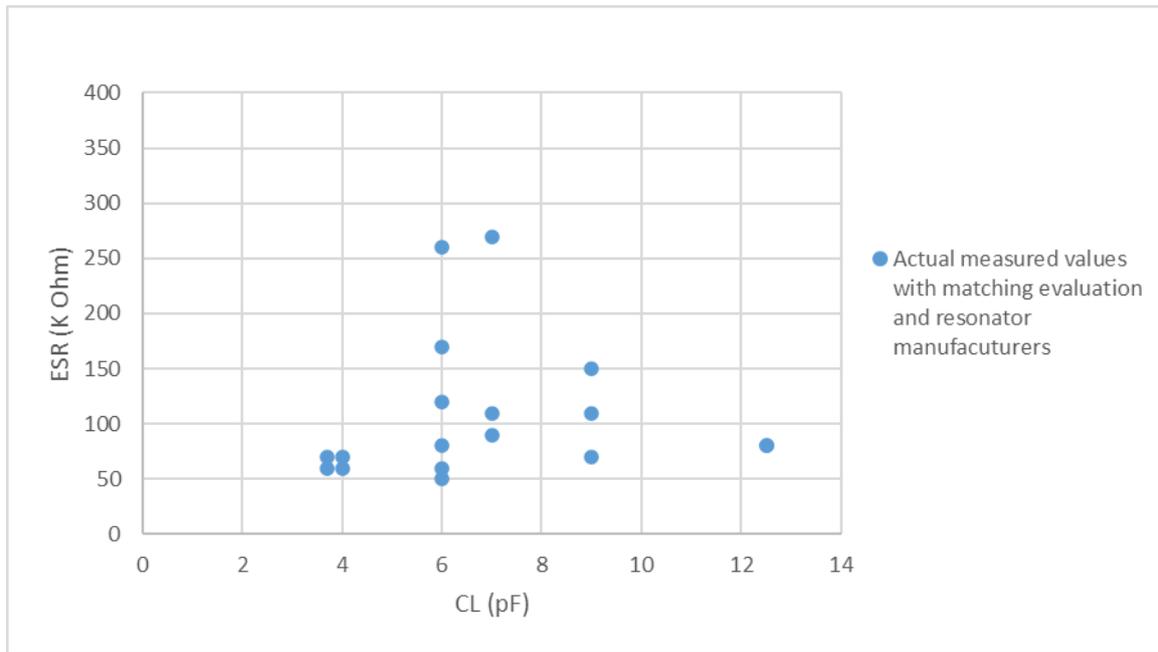


Figure 4.2.6 Group 6, Sub-clock: C_L vs ESR max

4.2.7 Group 7

The matching evaluation results of Group 7 are shown below.

Table 4.2.7 Group 7, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR _{max} (kOhm)
Standard CL ⁶	32	9	0	15	18	-620	120
Standard CL ⁶	32	12.5	0	22	22	-450	90
Standard CL ⁶	32	10	0	5	5	-2,080	410
LowCL1 ⁶	32	5	0	4	4	-1,130	220
LowCL1 ⁶	32	7	0	10	12	-660	130
LowCL1 ⁶	32	10	0	5	5	-950	190
LowCL2 ⁶	32	5	0	4	4	-450	90
LowCL2 ⁶	32	6	0	9	9	-380	70
LowCL2 ⁶	32	10	0	5	5	-390	70
LowCL3 ⁶	32	4	0	4	4	-300	60

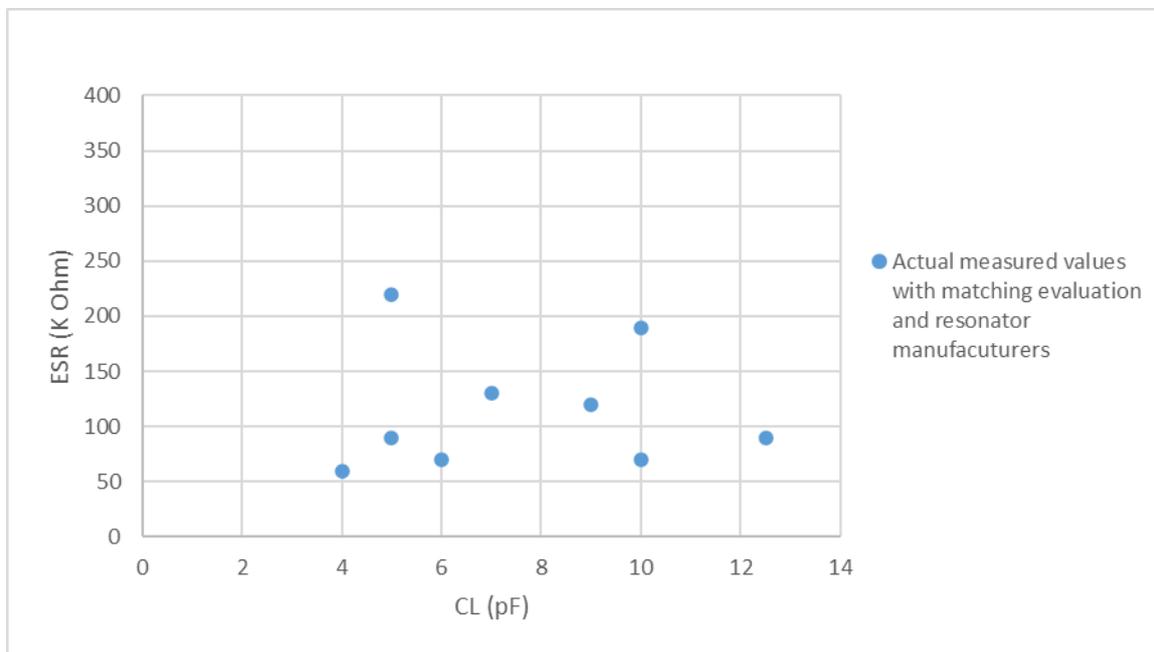


Figure 4.2.7 Group 7, Sub-clock: C_L vs ESR max

4.2.8 Group 8

The matching evaluation results of Group 8 are shown below.

Table 4.2.8 Group 8, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR_max (kOhm)
standard ⁶	32	9	0	9	9	-500	100
standard ⁶	32	12.5	0	22	18	-360	70

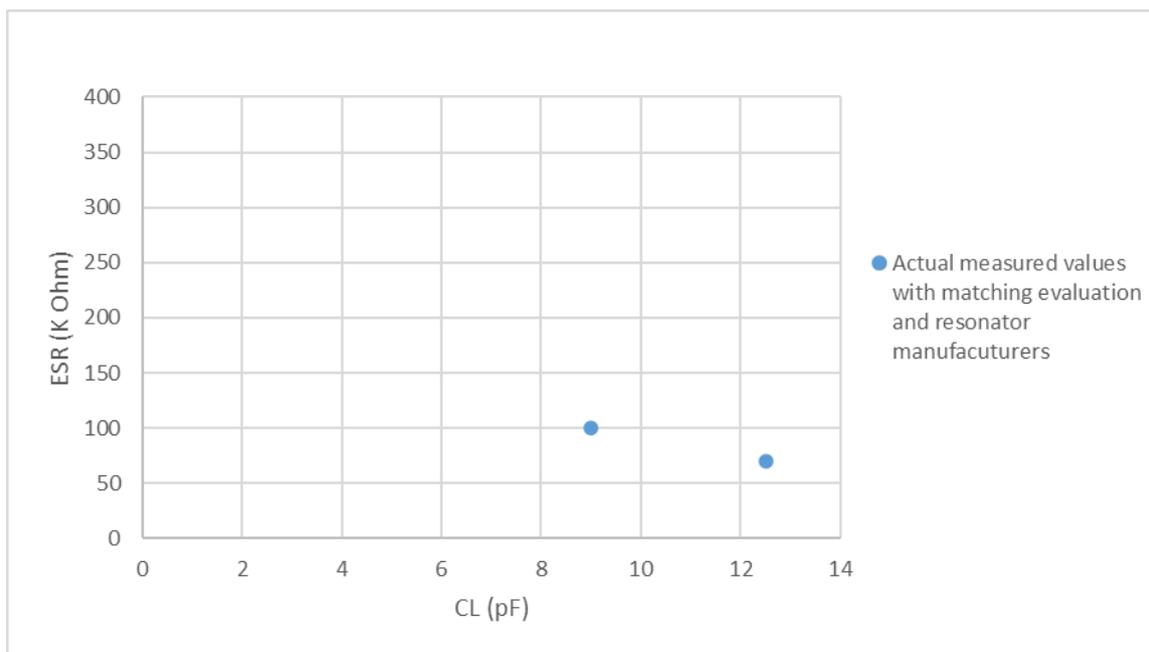


Figure 4.2.8 Group 8, Sub-clock: C_L vs ESR max

4.2.9 Group 9

The matching evaluation results of Group 9 are shown below.

Table 4.2.9 Group 9, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR _{max} (kOhm)
Standard CL ⁶	32	6	0	6	6	-1,090	210
LowCL1 ⁶	32	6	0	6	6	-690	130
LowCL2 ⁶	32	6	0	6	6	-470	90
LowCL3 ⁶	32	6	0	6	6	-590	110
Low Power Mode 3 ⁶	32	6	0	N.M	N.M	-690	130

N.M: Not Mount

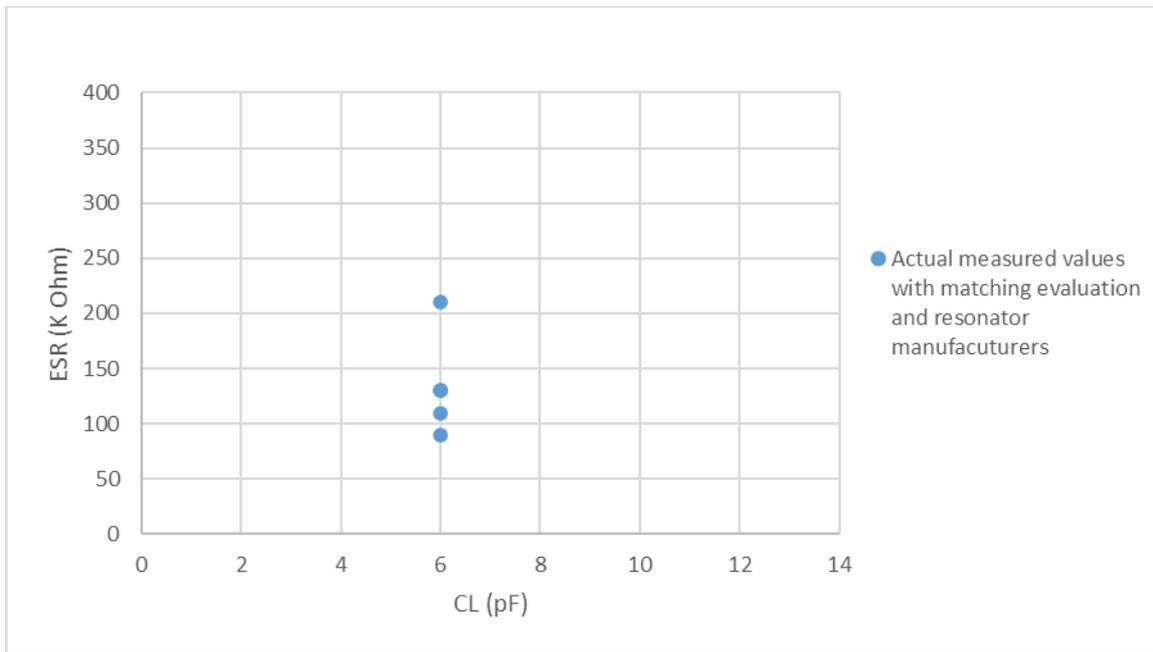


Figure 4.2.9 Group 9, Sub-clock: C_L vs ESR max

4.2.10 Group 10

The matching evaluation results of Group 10 are shown below.

Table 4.2.10 Group 10, Sub-clock: Results of the matching evaluation

Sub Clock Oscillator Driving Setting ⁵	Resonator specification		Evaluation board implementation			Evaluation results	
	Frequency (kHz)	C _L (pF)	R _d (Ohm)	C _{L1} (pF)	C _{L2} (pF)	Negative R (kOhm)	Recommended ESR _{max} (kOhm)
Standard CL ⁶	32	6	0	4	4	-1,740	340
LowCL1 ⁶	32	6	0	4	4	-940	180
LowCL2 ⁶	32	6	0	4	4	-600	120
LowCL3 ⁶	32	6	0	4	4	-270	50

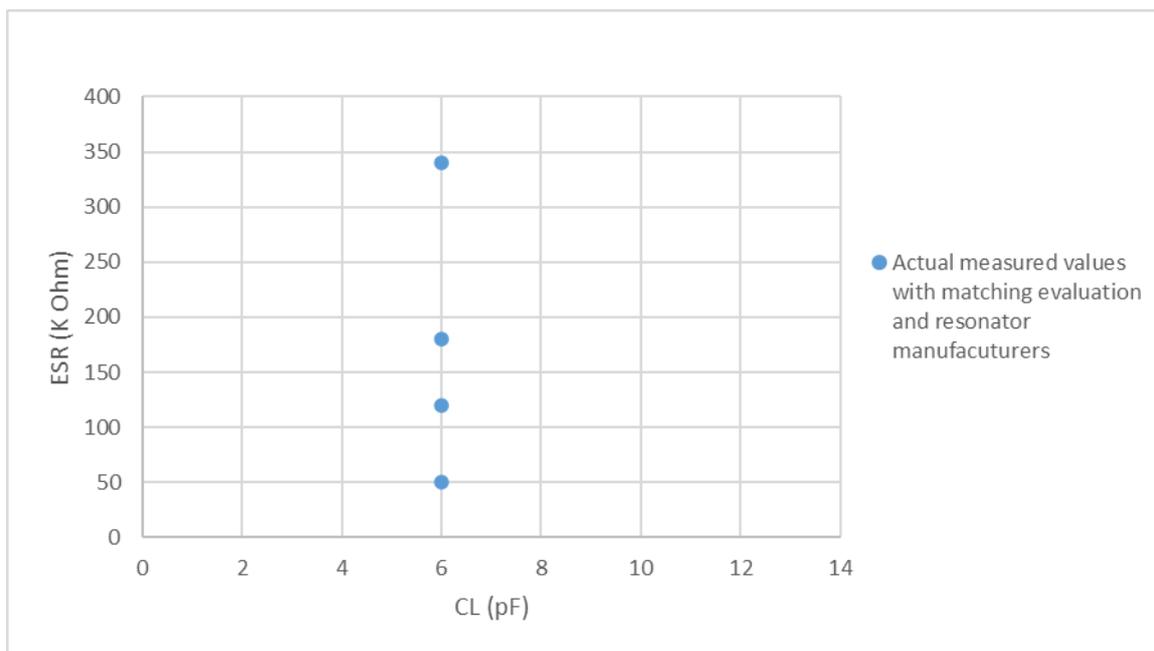


Figure 4.2.10 Group 10, Sub-clock: C_L vs ESR max

4: For the setting of the drive capability register of the main clock, refer to the "Clock Generation Circuit" chapter of the User's Manual: Hardware for both RX and RA.

Example:RX66N: MODRV2[1:0] = b11 (Drive capability 8 MHz)
 RA4E2: MODRV[1:0] = b11 (Drive capability 8 MHz)

5: Refer to the following chapter for setting of the sub-clock drive capability register.

RX: Real-time Clock in the User's Manual: Hardware
 RA: Chapter "Clock Generator" in the User's Manual: Hardware

Example:RX66N: RTCDV[2:0] = b110 (Standard C_L)
 RA4E2: then SODRV[1] = b0 (Normal C_L)

6: The magnitude relationship between the drive capacity settings is as follows.

Notations used in this application note	Notations used in RX Family User's Manual	Notations used in RA Family User's Manual	Drive capability
Standard C _L	Standard C _L	Normal mode	4 (highest)
Low C _L (High drive)	Low C _L (High drive)	Low power mode 1	3
Low C _L (Medium drive)	Low C _L (Medium drive)	Low power mode 2	2
Low C _L (Low drive)	Low C _L (Low drive)	Low power mode 3	1 (minimum)

5. Oscillator matching evaluation method and oscillator circuit parameter calculation method

This chapter describes how to evaluate external components. The oscillation stability of the resonator is determined by whether the negative resistance or transconductance is sufficiently large relative to the ESR of the oscillator.

5.1 How to measure the negative resistance

To measure the negative resistance of the oscillator circuit, insert a resistor in series with the resonator as shown in Figure 5.1.1 **Measurement method of the negative resistance**, and check the maximum resistance of the resistor at which the oscillation of MCU clock output can be maintained. Use the FET probe (low capacitance, high impedance) when observing the MCU clock output waveform with an oscilloscope. It is recommended that the resistance of the series resistor be approximately five times ESR (equivalent series resistance) of the resonator.

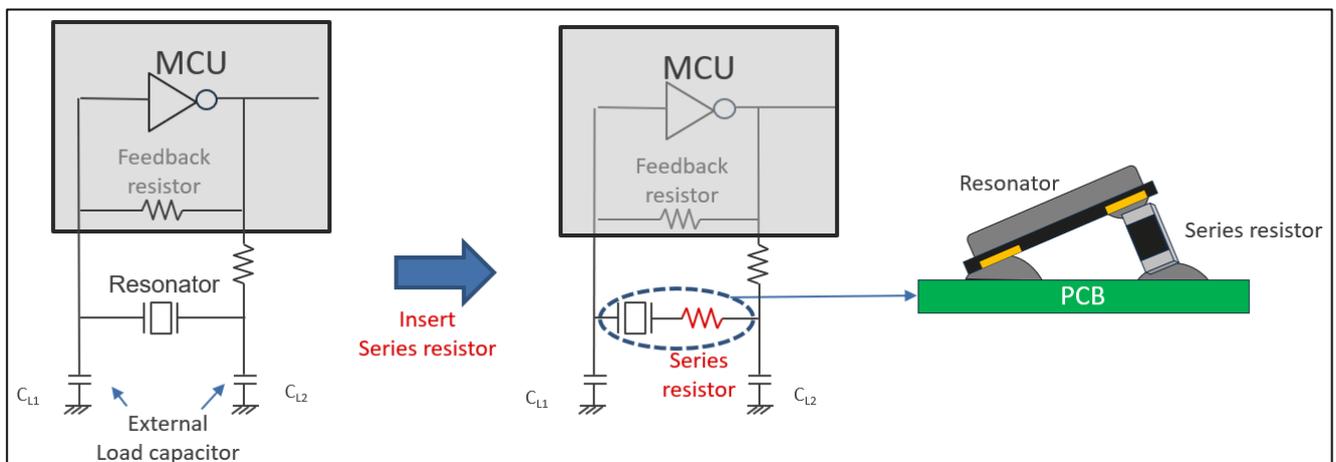


Figure 5.1.1 Measurement method of the negative resistance

5.2 Measurement method of oscillations' excitation power

The oscillations' excitation power (μW) is calculated from the oscillation current (I_{RMS}) measured by a current probe clamped to the resonator and the wire inserted between the circuit board as shown in Figure 5.2.1 Measurement method of the oscillations excitation power, and the equivalent series resistance of the oscillator (R_{load}).

■ Oscillations excitation power = $R_{\text{load}} * I_{\text{RMS}}^2$ (μW)

If the excitation power exceeds the specification of the resonator, consider the following measures.

- Add a damping resistor on the board.
- Decrease the oscillator drive capability of MCU.

See Note 6 in Chapter 4 for information of the MCU's oscillator drive capability.

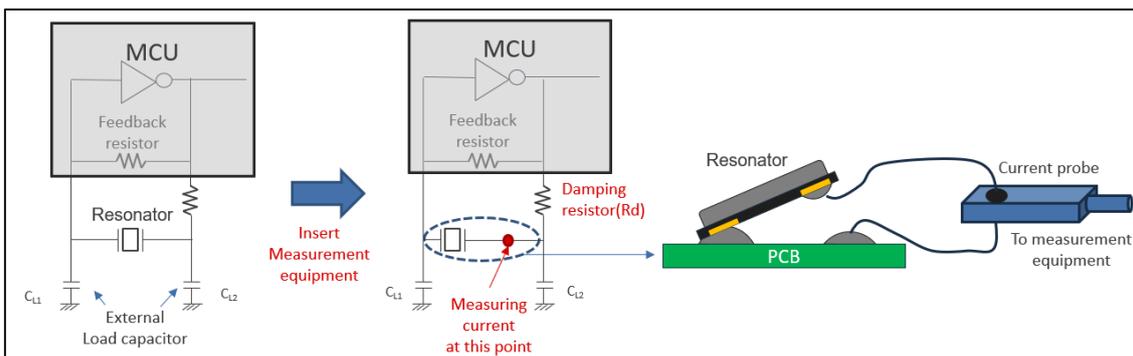


Figure 5.2.1 Measurement method of the oscillations excitation power

5.3 Measurement method of the oscillation amplitude voltage

Prepare a board with the selected external components according to Chapter 5.1 and Chapter 5.2. Connect a FET probe to XTAL/XCOU and VSS of the MCU as shown in Figure 5.3.1 Oscillation Amplitude Voltage Measurement Method to measure the oscillation amplitude voltage. If the measured voltage exceeds the absolute maximum rating of the MCU, consider the following measures.

- Add a damping resistor on the board.
 - Decrease the oscillator drive capability of the MCU.
- See Note 6 in Chapter 4 for information of the MCU’s oscillator drive capability.

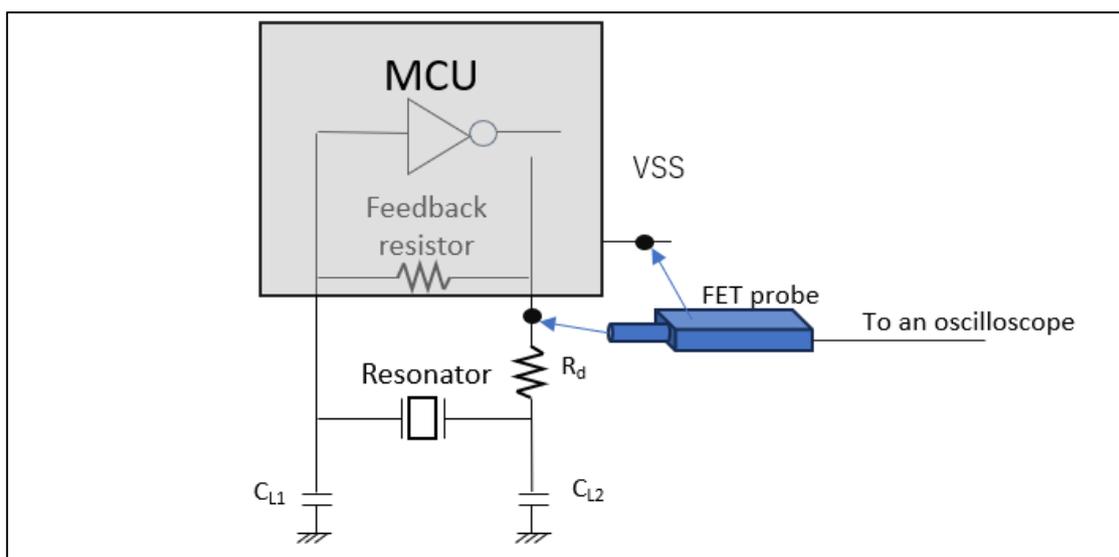


Figure 5.3.1 Oscillation Amplitude Voltage Measurement Method

5.4 How to determine the load capacitor values

In general, to determine the external load capacitance, adjust the capacitance in the actual experiment so that the oscillation frequency becomes the target value. If you want to estimate the external load capacitance without experimenting, follow the procedure below.

If you want to estimate the C_L of the load capacitor accurately, you must also consider the parasitic capacitance of the board, as shown in the Figure 5.4.1 Formula for the External Load Capacity (C_{L1} and C_{L2}) (Exact Version). However, in this application note, to simplify the calculation, we use the formula in the Figure 5.4.1 Formula for the External Load Capacity (C_{L1} and C_{L2}) (Simplified Version), where the parasitic capacitance value of the board is "zero". Other conditions are listed below.

- C_L : Use the resonator manufacturer's recommended value for the external load capacitor. For example, in this case we use $C_L = 8$ pF as a typical value.
- C_{L1} and C_{L2} : Assume them to the same value. ($C_{L1} = C_{L2}$)
- C_{ps} : The typical MCU pin-to-pin capacitance is 1 pF. Use the actual measured value if you want to calculate it accurately.

Substituting these values into the equation shown in Figure 5.4.1 Formula for the External Load Capacity (C_{L1} and C_{L2}) (Simplified version) gives capacitance of 14 pF for the external load capacitance, C_{L1} and C_{L2} .

■ $C_{L1} = C_{L2} = (C_L - C_{ps}) * 2 = (8 - 1) * 2 = 14$ pF

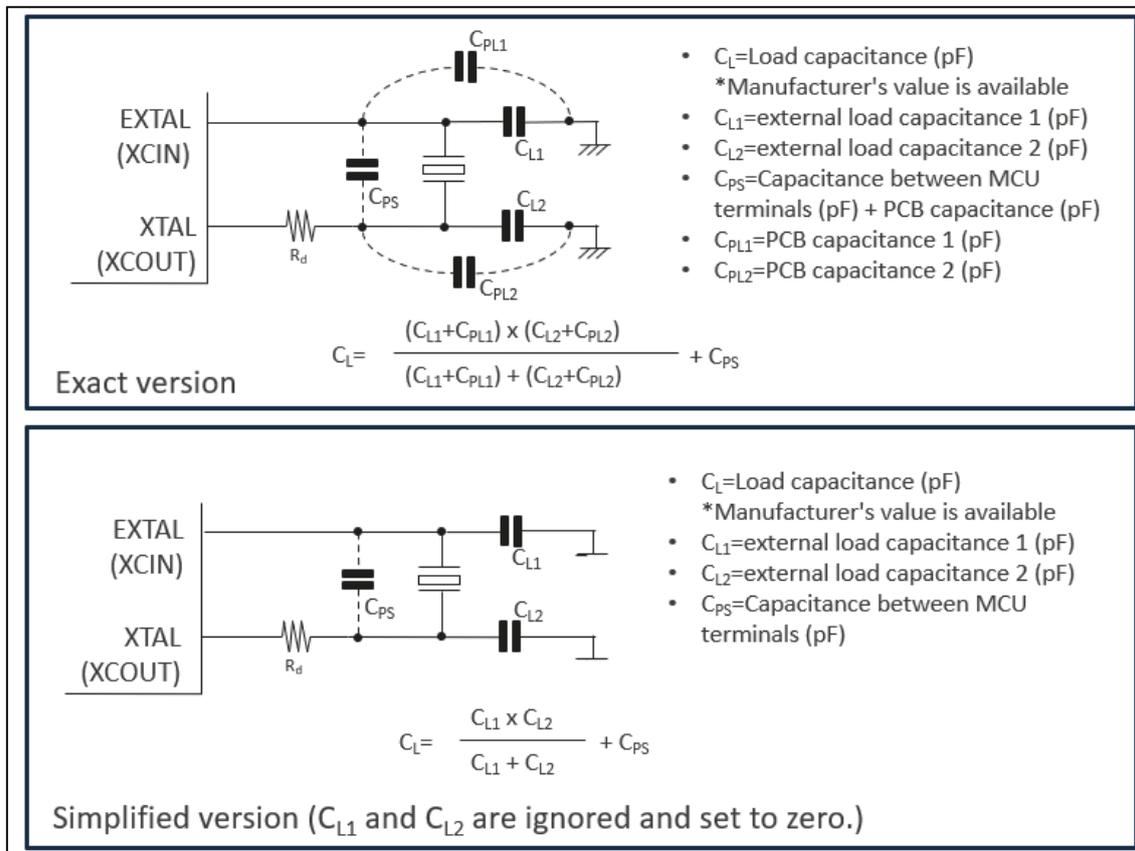


Figure 5.4.1 Formula for the External Load Capacity (C_{L1} and C_{L2})

5.5 Calculation method of transconductance

The transconductance (G_m) of the MCU oscillator can be calculated using the following equation. As R , C_{L1} , C_{L2} in this equation, use the matching evaluation results described in Chapter 4. The calculation result is a reference value and is not guaranteed.

- $G_m = |R| * (\omega^2 \times C_{L1} \times C_{L2})$ * When the resistance of the damping register (R_d) is 0 Ohm
 - R : Negative Resistance (Ohm)
 - ω : Angular frequency ($2\pi \times$ frequency (Hz)) (rad/sec)
 - C_{L1} , C_{L2} : External load capacitance (pF)

6. Board design recommendations

6.1 How to stabilize the oscillation

6.1.1 EXTAL/XCIN and XTAL/XCOU Routing

(1) through (6) below describe recommendations for the EXTAL/XCIN and XTAL/XCOU routing. Figure 6.1.1 Example of the EXTAL/XCIN and XTAL/XCOU Routing Pattern: LQFP Package through Figure 6.1.4 Pattern example when two external capacitors are difficult to place near MCU show examples of their traces.

- (1) Do not cross the EXTAL/XCIN and XTAL/XCOU wires with other signal wires.
- (2) Do not connect any testing terminals to the EXTAL/XCIN and XTAL/XCOU wires.
- (3) Make the EXTAL/XCIN and XTAL/XCOU wires width between 0.1 mm and 0.3 mm. The wires length from the MCU pins to the resonator pins should be within 10 mm as much as possible.
- (4) The trace connected to the EXTAL/XCIN pin, and the trace connected to the XTAL/XCOU pin should have as much space between them as possible (at least 0.3 mm).
- (5) Connect the two external load capacitors with the shortest routing distance and connect the routing to the ground pattern on the component surface (hereafter referred to as ground shield. See chapter 6.1.2 for details). If there is no space near the MCU of the PCB and the external load capacitors cannot be placed near the MCU as shown in Figure 6.1.1 to Figure 6.1.3 place them as shown in Figure 6.1.4.
- (6) To reduce the parasitic capacitance between the EXTAL/XCIN and XTAL/XCOU, add a ground trace between the resonator and the MCU.

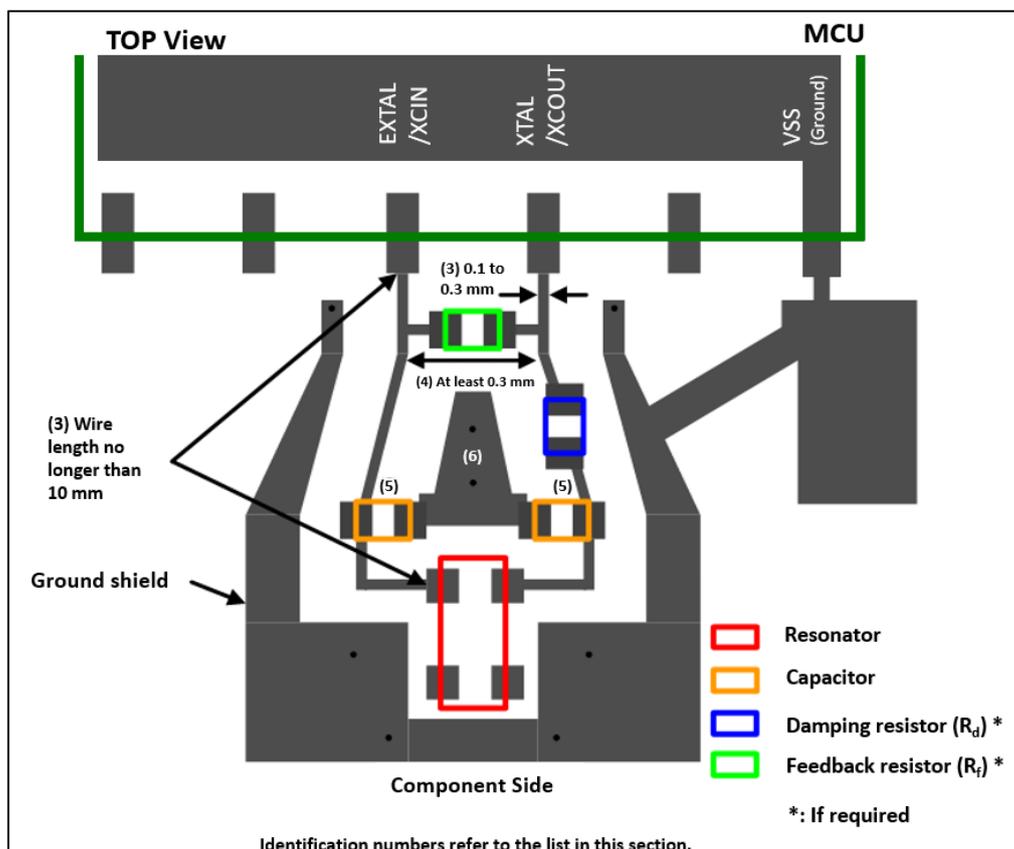


Figure 6.1.1 Example of the EXTAL/XCIN and XTAL/XCOU Routing Pattern: LQFP Package

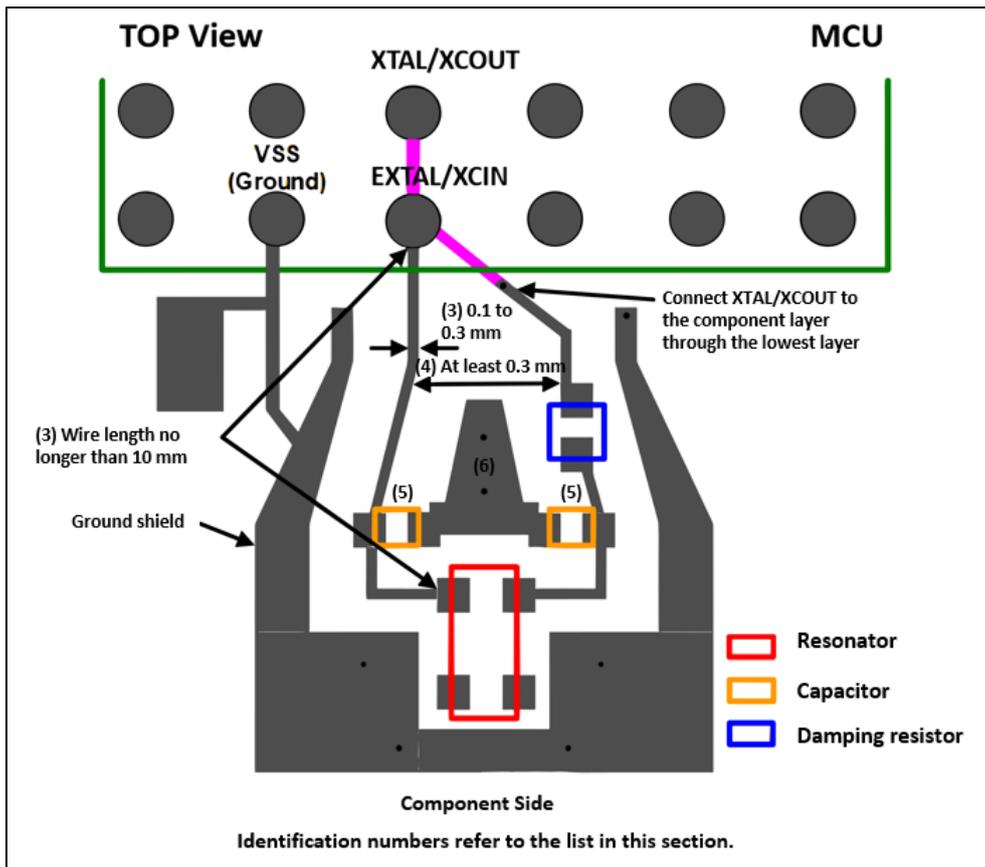


Figure 6.1.2 Example of the EXTAL/XCIN and XTAL/XCOUT Routing Pattern: LGA Package

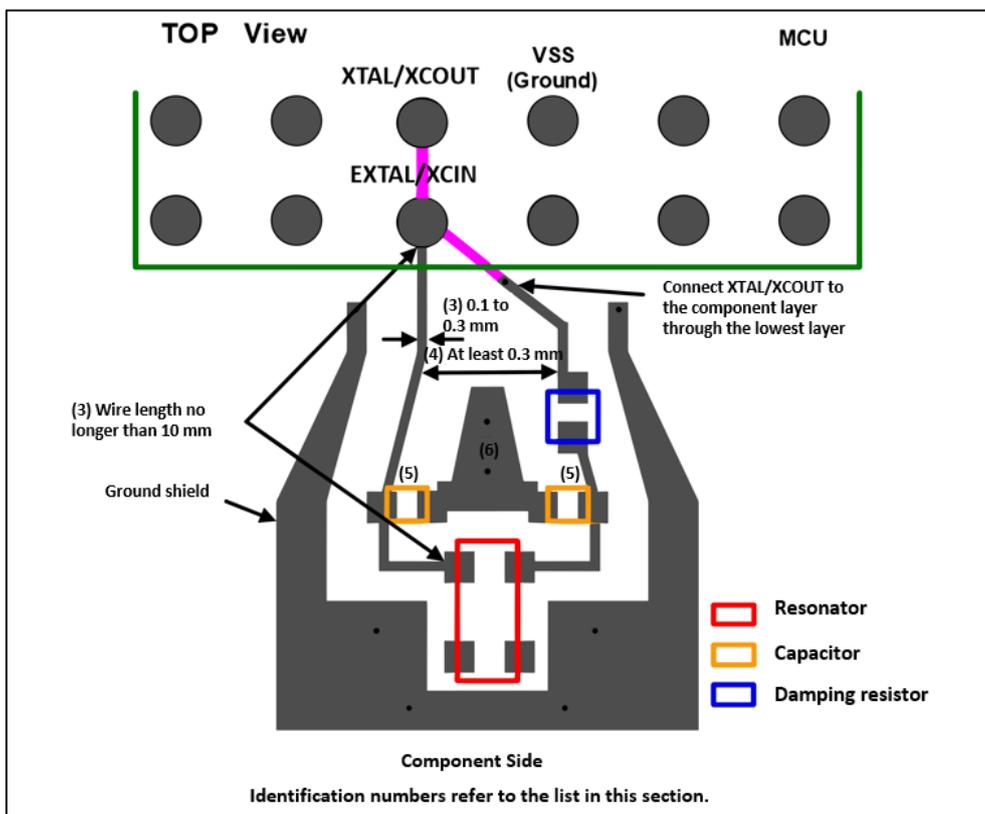


Figure 6.1.3 Example of the EXTAL/XCIN and XTAL/XCOUT Routing Pattern: BGA Package

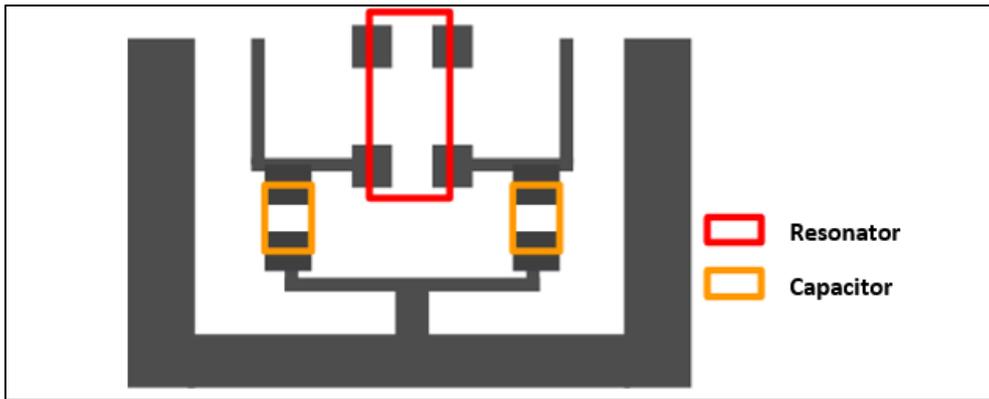


Figure 6.1.4 Pattern example when two external capacitors are difficult to place near MCU

6.1.2 Use a ground shield

Shield the resonator with a ground trace. (1) through (4) below describe the recommendations for the ground shield Figure 6.1.5 Example of the ground shield tracing: LQFP Package through Figure 6.1.7 Example of the ground shield tracing: BGA Package show trace examples for each package.

In addition, the ground shield of the main clock oscillator circuit and the sub-clock oscillator circuit should not be a continuous pattern as shown in Figure 6.1.8. If the ground shield of the main clock oscillator and the ground shield of the sub-clock oscillator are directly connected, the output of the main clock oscillator may propagate as noise to the ground shield of the sub-clock and affect the oscillation of the sub-clock.

- (1) Place the ground shield on the same layer as the resonator trace routing.
- (2) Make the ground shield trace width at least 0.3 mm and leave a gap of 0.3 to 2.0 mm between the ground shield and other traces.
- (3) Route the ground shield as close as possible to the VSS pin on the MCU and make sure that the trace width is at least 0.3 mm.
- (4) To prevent current from flowing through the ground shield, branch the ground shield and the ground on the board near the VSS pin on the board.

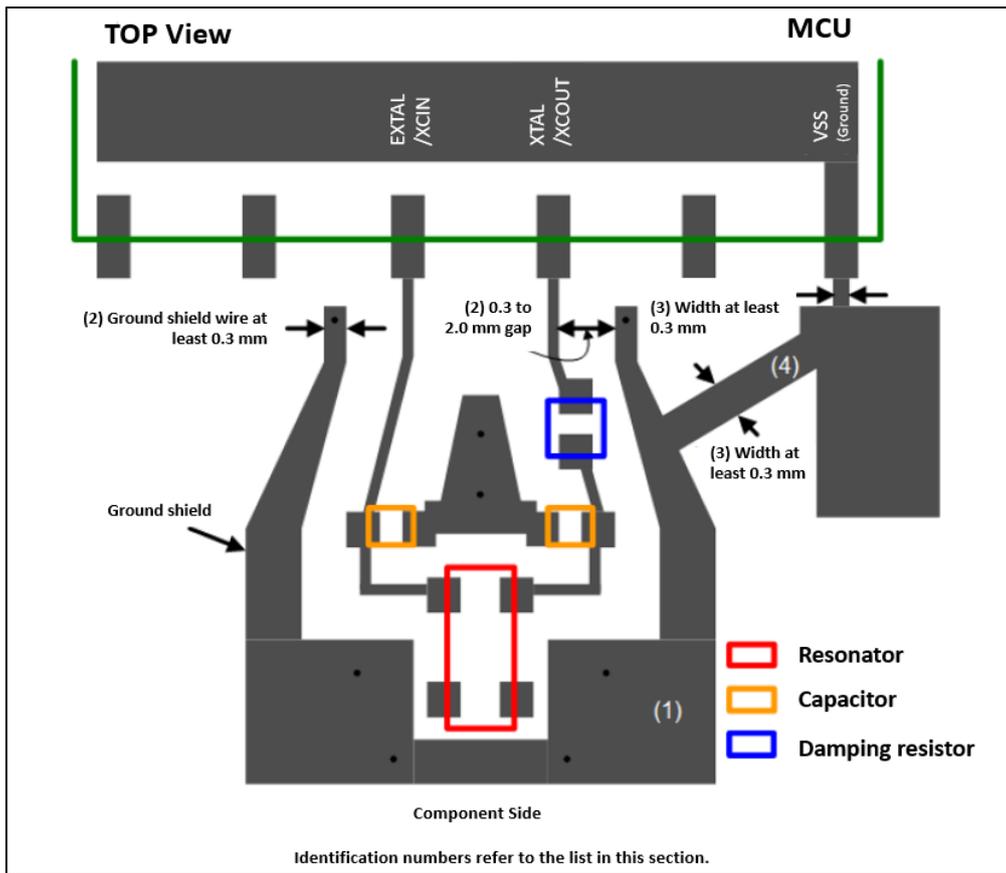


Figure 6.1.5 Example of the ground shield tracing: LQFP Package

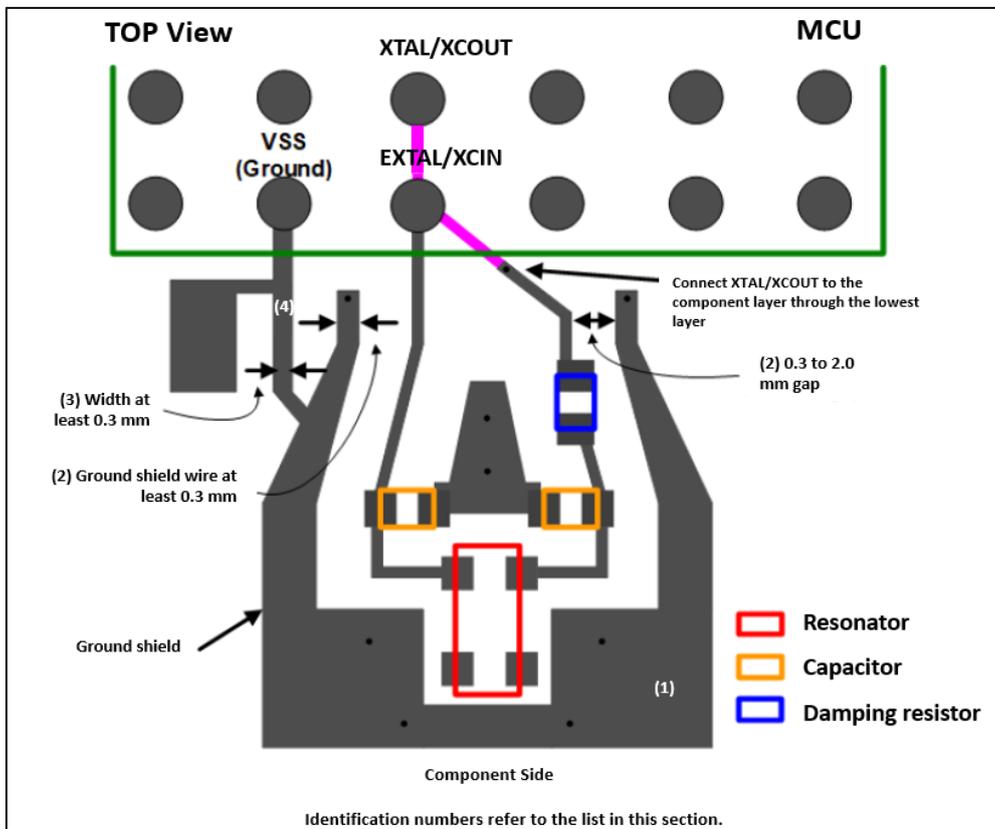


Figure 6.1.6 Example of the ground shield tracing: LGA Package

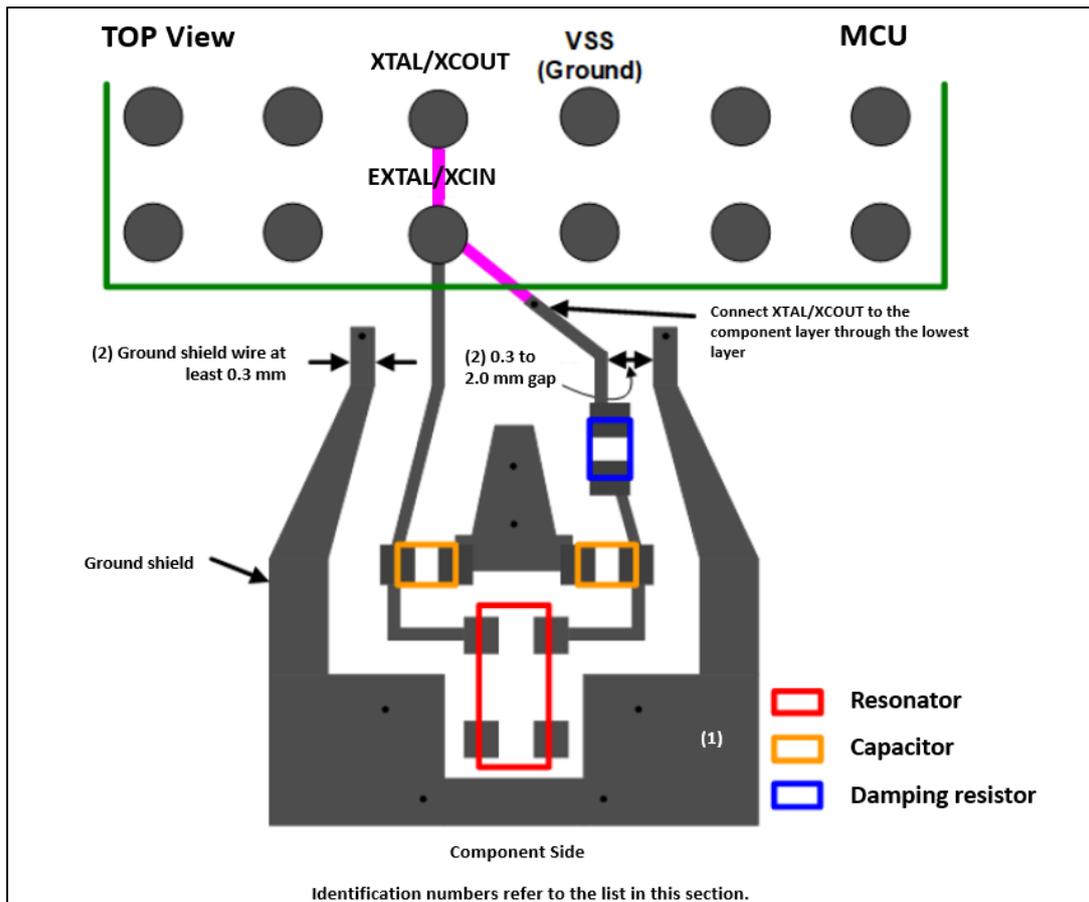


Figure 6.1.7 Example of the ground shield tracing: BGA Package

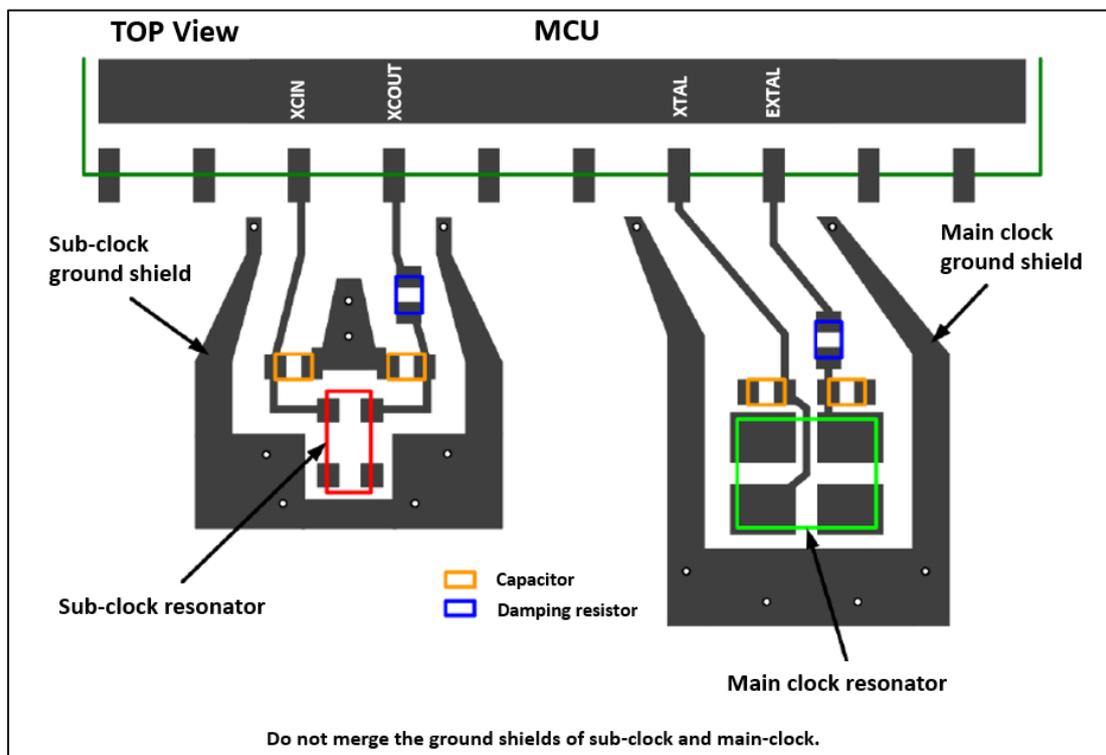


Figure 6.1.8 Example of the main clock and sub-clock ground shield configuration

6.1.3 Usage of a bottom-ground

6.1.3.1 Multilayer boards thicker than 1.2 mm

For multilayer boards thicker than 1.2 mm, place a ground pattern (hereafter referred to as bottom ground) on the solder surface of the resonator area (see Figure 6.1.9 through Figure 6.1.11).

The recommendations of the bottom ground are shown below. Figure 6.1.9 through Figure 6.1.11 show examples of patterns for each package.

- (1) Do not place power supply, ground, or signal line patterns in the middle layer of the resonator area. The parasitic capacitance and crosstalk between layers may affect stable oscillation.
- (2) Connect the ground shield termination on the component side to the bottom ground. If the termination is not connected to bottom ground and is an open end, there is a risk that the ground shield will become a noise source by acting as an antenna.
- (3) Make the bottom ground at least 0.1 mm larger than the ground shield.
 - Case of LQFP and LGA/BGA (whose VSS is placed in the outer column):
Connect the bottom ground only to the ground shield on the component side.
Do not connect the bottom ground directly to the VSS terminal, but connect it through the ground shield.
Do not connect any ground other than the VSS pin to the bottom ground and the ground shield.
 - Case of LQFP and LGA/BGA (whose VSS is placed in the inner column):
Connect the bottom ground directly to the VSS pin.
Do not connect any ground other than the VSS pin to the bottom ground and ground shield.

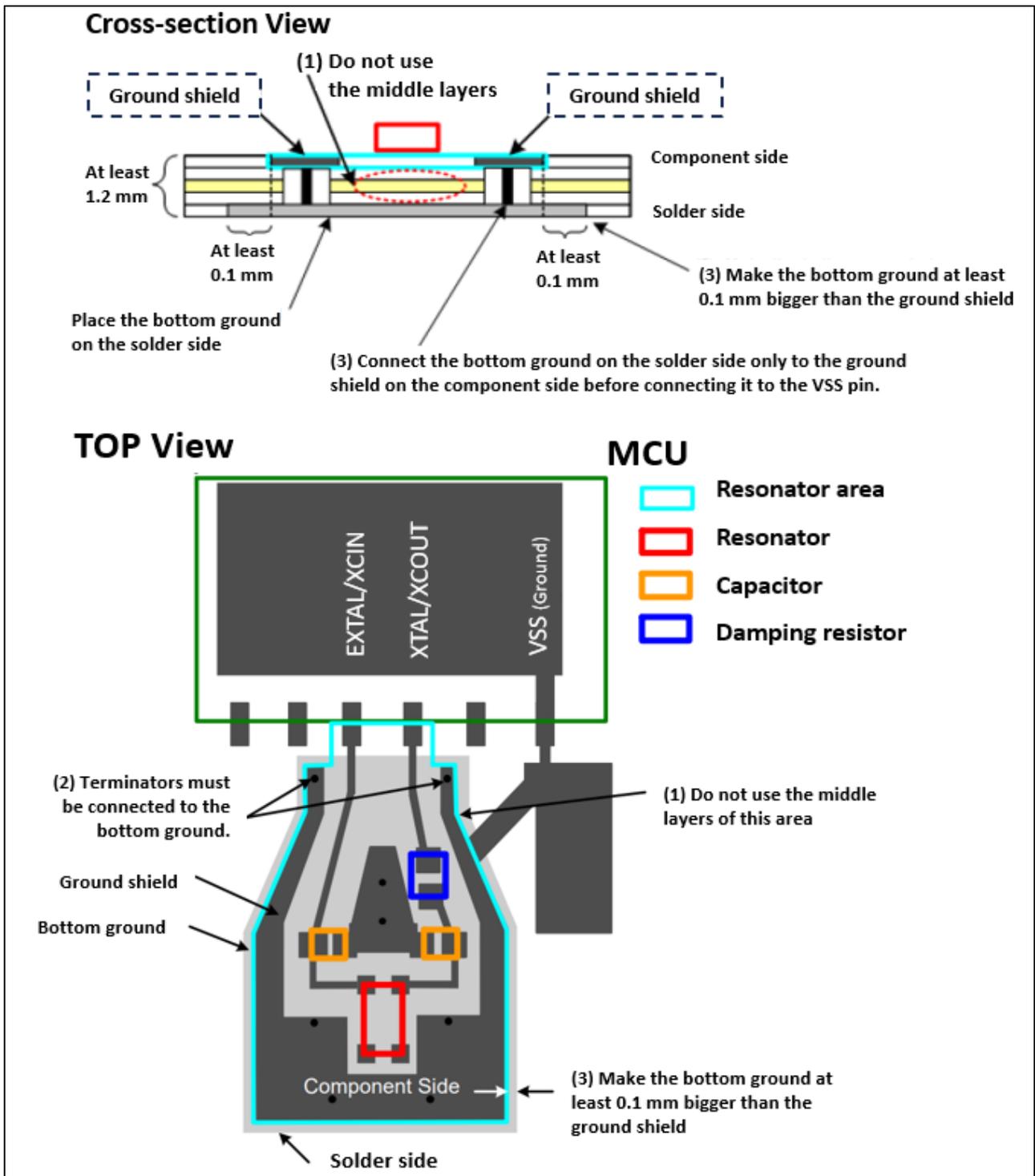


Figure 6.1.9 Routing example for a multilayer board thicker than 1.2 mm: LQFP Package

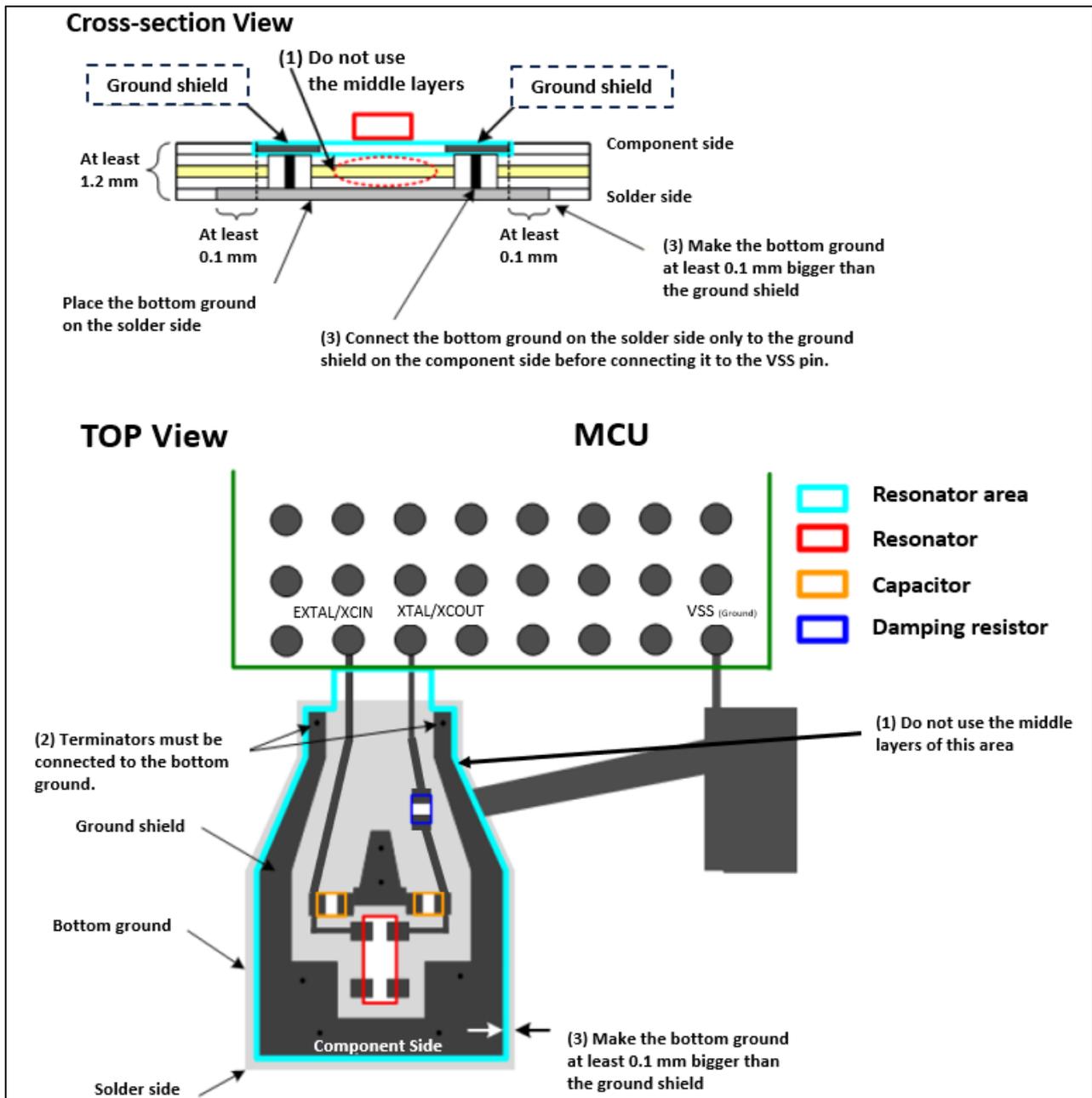


Figure 6.1.10 Routing example for a multilayered board thicker than 1.2 mm: LGA/BGA Package (VSS is placed in the outer column)

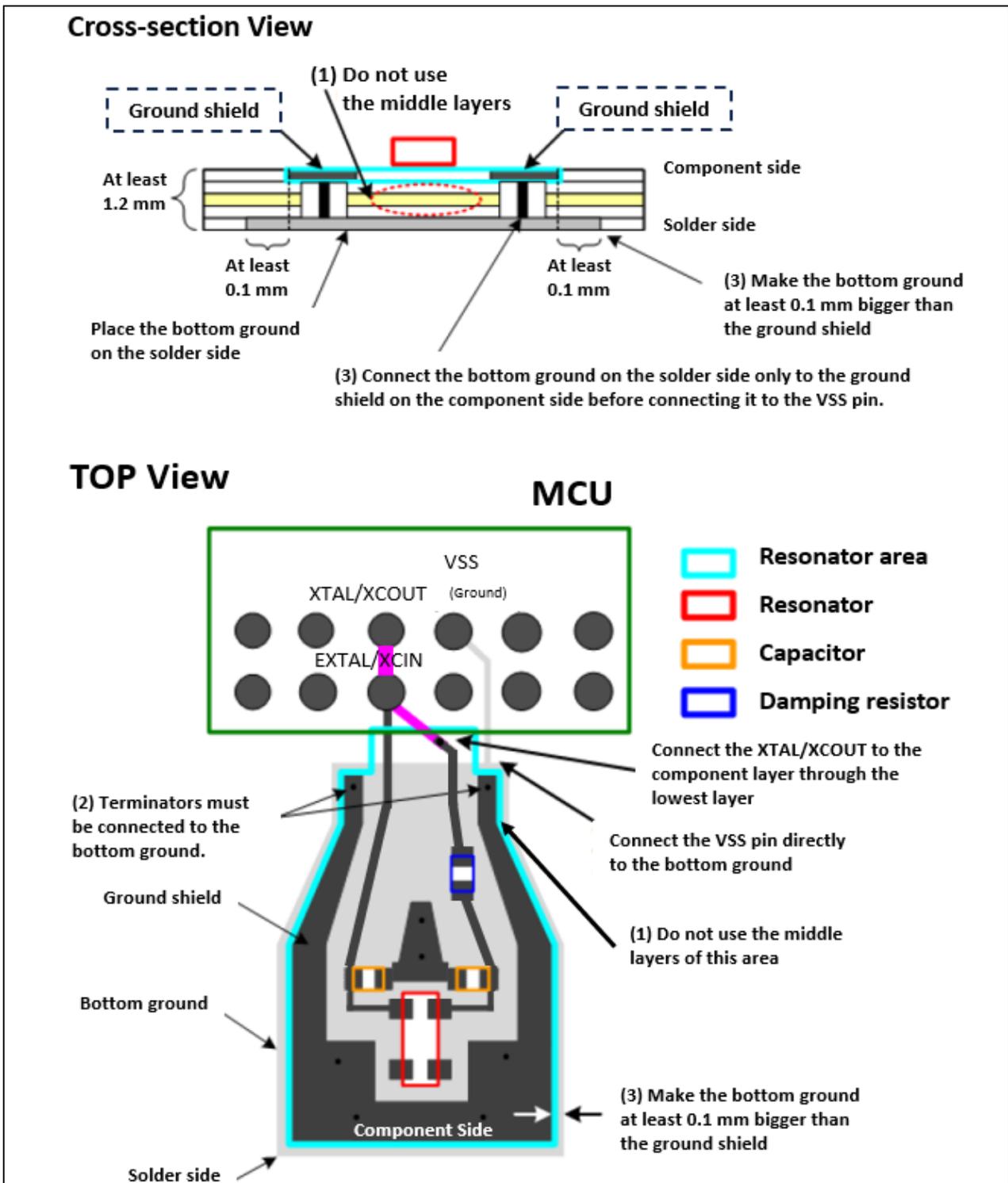


Figure 6.1.11 Routing example for a multilayered board thicker than 1.2 mm: LGA/BGA Package (VSS is placed in the inner column)

6.1.3.2 Multilayer boards thinner than 1.2 mm

The following are recommendations to consider when routing a multilayer board thinner than 1.2 mm. Figure 6.1.12 shows an example routing.

- (1) Do not place power supply, ground, and signal line patterns in the middle layer of the resonator area. Do not place power, ground, or signal line patterns on the solder surface as well. The parasitic capacitance and crosstalk between the layers may interfere with stable oscillation.

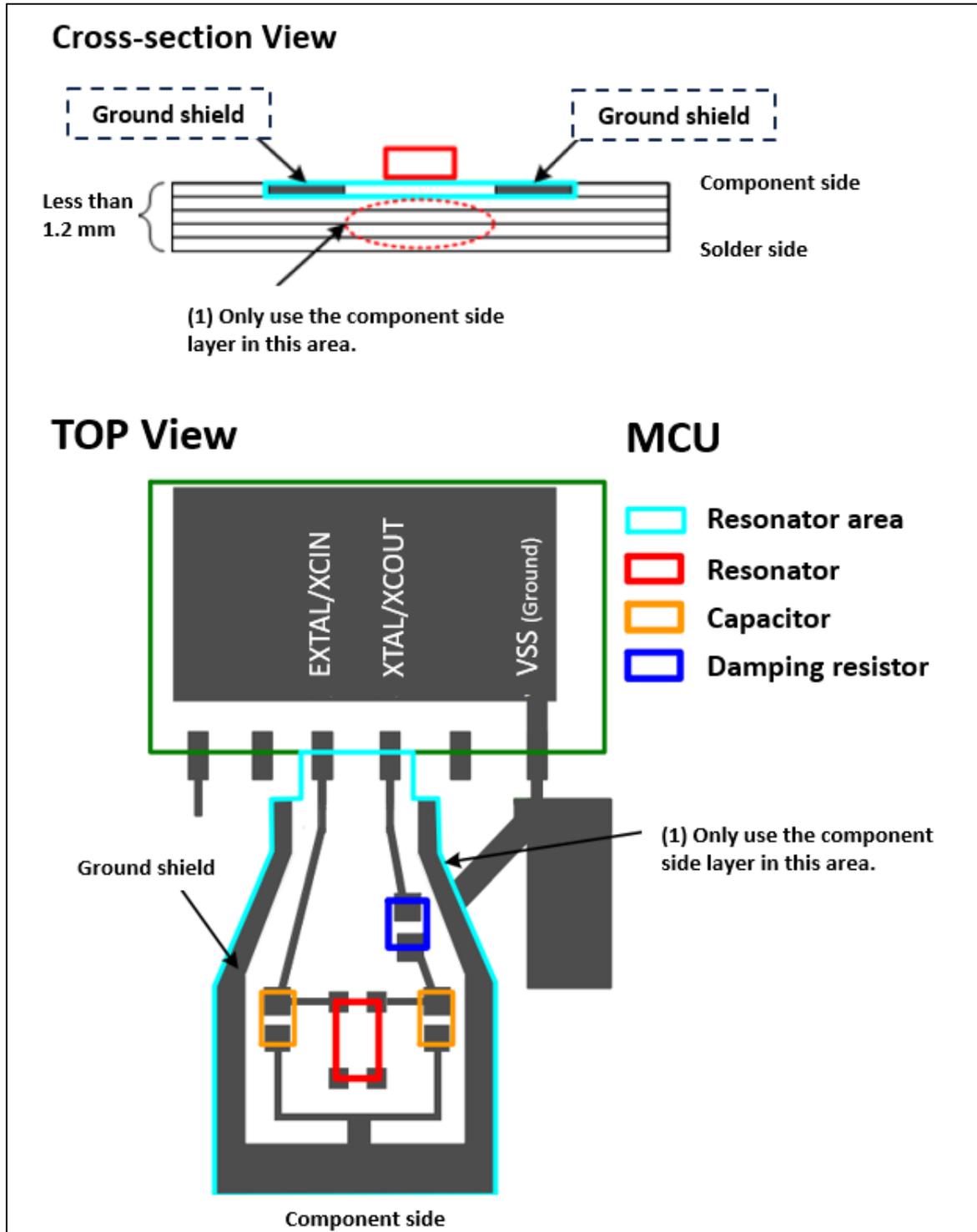


Figure 6.1.12 Routing Example When a Multilayered Board is less than 1.2 mm: LQFP Package

6.1.4 Other miscellaneous recommendations

The following are common recommendations for all packages. Figure 6.1.13 also shows an LQFP pattern as an example.

- (1) Do not place the EXTAL/XCIN and XTAL/XCOOUT wires near traces with large current variations.
- (2) Do not place the EXTAL/XCIN and XTAL/XCOOUT wires in parallel with other signal wires, such as those for adjacent pins.
- (3) Do not place the wires of the terminals adjacent to EXTAL/XCIN and XTAL/XCOOUT in parallel with the EXTAL/XCIN and XTAL/XCOOUT traces. Do not connect them directly to the outside of the MCU, but first route them through the bottom of the MCU and then bring them out from a location away from the EXTAL/XCIN and XTAL/XCOOUT pins.
- (4) Place the ground trace on the bottom side of the MCU and make this as large as possible.

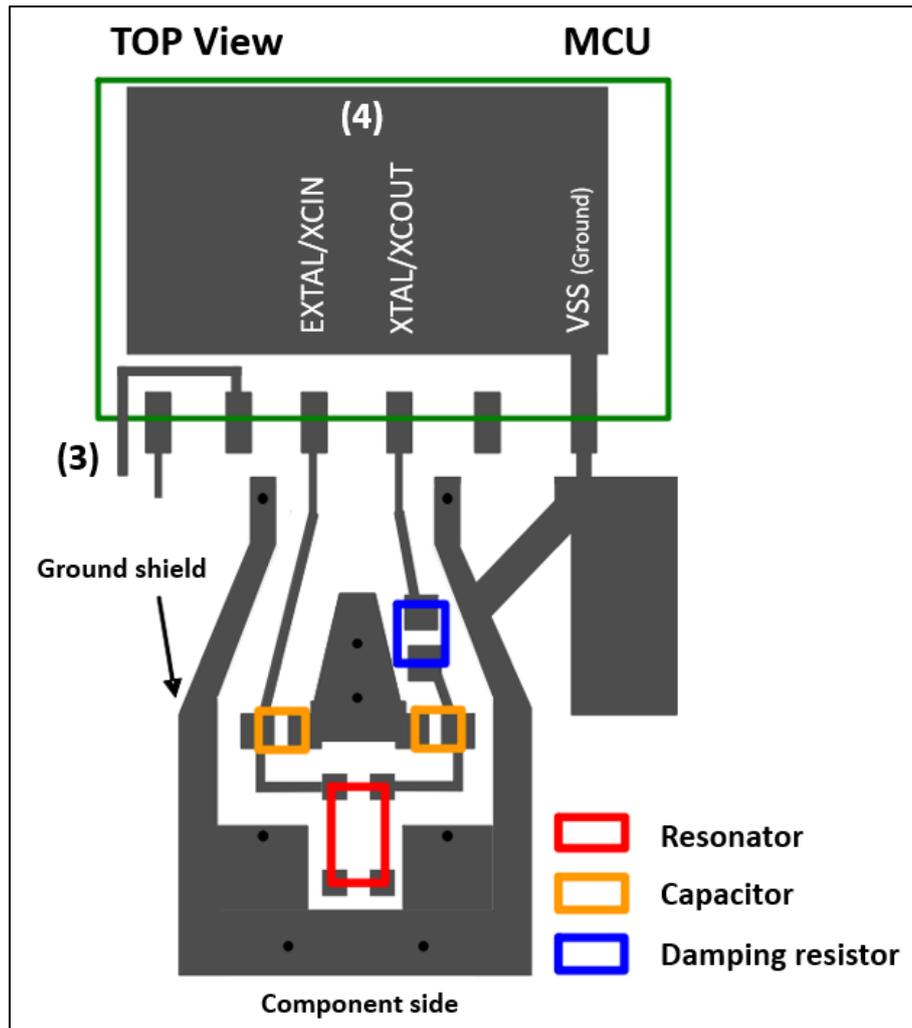


Figure 6.1.13 Example of Routing for Other Points: LQFP Package

6.2 Examples of patterns with a high risk of malfunction due to noise

Avoid the issues listed below in your PCB design as they may cause the resonator to oscillate incorrectly or may increase EMI. Figure 6.2.1 Example of a pattern with a high risk of malfunction due to noise shows some examples of incorrect patterns.

- (1) The EXTAL/XCIN and XTAL/XCOOUT wires cross other signal wires. The MCU may malfunction due to crosstalk.
- (2) Observation pins (test points) are attached to the EXTAL/XCIN and XTAL/XCOOUT wires. There is a risk of unstable oscillation due to impedance mismatch in the wiring and reflections in the oscillation waveform.

- (3) The EXTAL/XCIN and XTAL/XCOUT wires are long.
Parasitic capacitance or inductance can cause oscillation instability and loss of accuracy. It is also a source of EMI.
- (4) The ground shield does not cover the entire oscillation area, the wiring from the board ground is long or the wiring is thin.
The oscillating circuit is easily affected by noise.
There is a risk that the ground potential difference between the MCU and the external load capacitance may affect the accuracy of the oscillation frequency.
- (5) The ground shield is not isolated from the board ground immediately adjacent to the VSS terminal.
The operating current of the MCU flows to the ground shield and may cause the resonator to malfunction.
- (6) The power and ground patterns are located under the EXTAL/XCIN and XTAL/XCOUT wiring.
Oscillation in the resonator circuit may stop due to a lack of clock caused by parasitic capacitance, impedance and noise.
- (7) Wires with high current flow are routed near the EXTAL/XCIN and XTAL/XCOUT wiring.
There is a risk that the resonator circuit will stop oscillating due to the effects of crosstalk.
- (8) The distance between the EXTAL/XCIN and XTAL/XCOUT wiring, and the wiring of the adjacent terminals is close, and the parallel length is long.
There is a risk that the resonator circuit will stop oscillating due to the effects of crosstalk.
- (9) Intermediate layers in the resonator area are used.
If there are ground and/or power supply layers in the intermediate layer, there is a risk that parasitic capacitance will affect the oscillation characteristics.
If signal lines are present, there is a risk of crosstalk causing the resonator circuit or signal lines to malfunction.
- (10) The oscillation area is extremely close to the board edge.
Cause an increase in EMI radiated from the resonator circuit to the outside of the board.

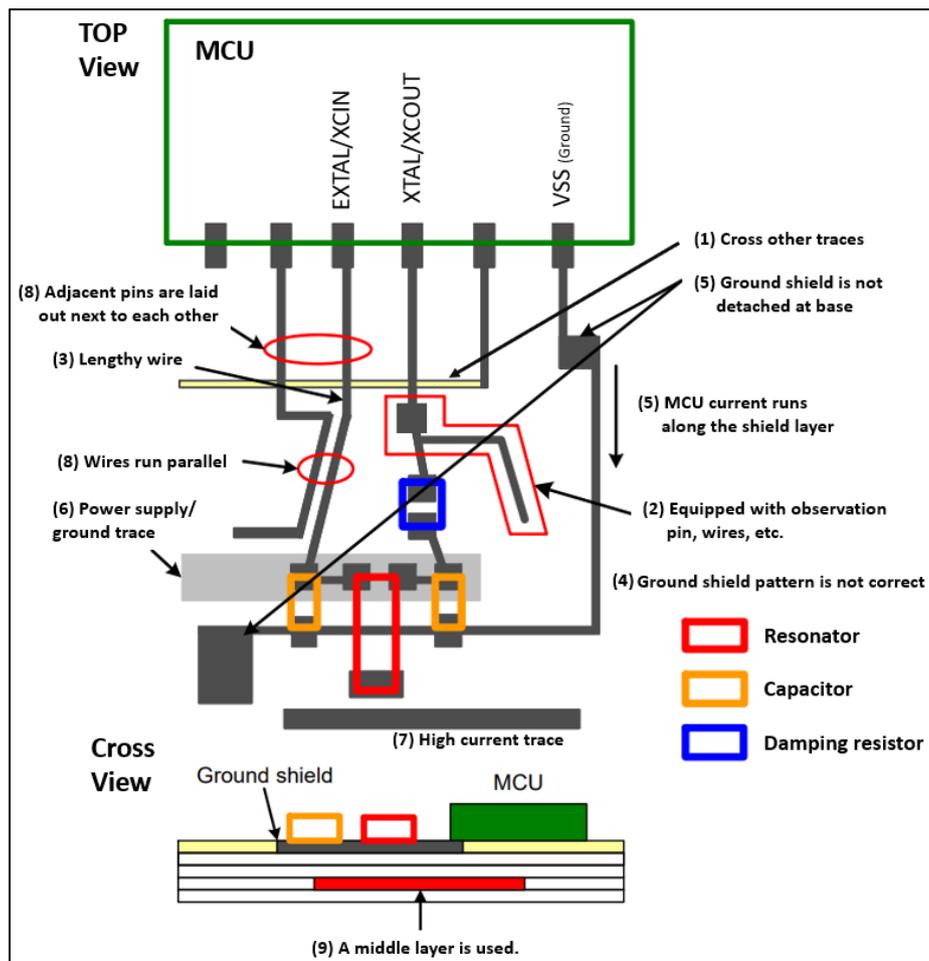


Figure 6.2.1 Example of a pattern with a high risk of malfunction due to noise

7. External Resonator Frequency Accuracy Measurement

As recommended by both resonator manufacturers and Renesas (in each MCU Hardware User's Manual), the correct implementation of the oscillator circuit includes 2 load capacitors (C_{L1} and C_{L2} in the diagram). Previous sections of this document cover capacitor selection. These capacitors directly influence the accuracy of the clock frequency. Loading capacitor values that are too high or too low can have a significant impact on the long-term accuracy of the clock, making the clock less reliable. The value of these capacitors is determined by a combination of the resonator device specification and the board layout, taking into account the stray capacitance of the PCB and the components in the clock path.

However, to correctly determine the accuracy of an oscillator circuit, the clock frequency must be measured on real hardware. Direct measurement of the oscillator circuit will almost definitely result in incorrect measurements. The typical value for the loading capacitors is in the range of 5 pF to 30 pF, and typical oscilloscope probe capacitance values are typically in the range of 5 pF to 15 pF. The additional capacitance of the probe is significant compared to the loading capacitor values and will skew the measurement, leading to incorrect results. The lowest value capacitance oscilloscope probes are still around 1.5 pF capacitance for very high precision probes, which would still potentially skew the measurement results.

The following is a suggested method for measuring clock frequency accuracy on MCU board products. This procedure eliminates potential measurement error due to capacitive loading added by the measurement probe.

7.1 Recommended Test Procedure

- One or more MCU boards for the device to be measured.
- Programming and emulation tools for the device to be measured.
- A frequency counter with at least 6-digit accuracy, with proper calibration

7.1.1 Test Method

1. Program the MCU to connect the clock crystal input for the sub-clock circuit to the CLKOUT pin of the MCU.
2. Connect the frequency counter to the CLKOUT pin of the MCU and an appropriate ground. DO NOT connect the frequency counter directly to the clock crystal circuit.
3. Configure the frequency counter to measure the frequency on the CLKOUT pin.
4. Allow the frequency counter to measure the frequency for several minutes. Record the measured frequency.

This procedure may be used for both sub-clock and main clock resonators. To see the effect of the loading capacitor values on clock crystal accuracy, the test can be repeated with different values for the loading capacitors. Select the values that provide the most accurate clock frequency for each clock.

It is also recommended to repeat the procedure on multiple boards of the same type to improve the validity of the measurements.

7.2 Frequency Accuracy Calculations

Frequency accuracy can be calculated using the following formulas:

f_m = measured frequency

f_s = ideal signal frequency

f_e = frequency error

f_a = frequency accuracy, typically expressed in parts per million (ppm) or parts per billion (ppb)

Frequency error can be expressed as

$$f_e = |f_s - f_m|$$

Frequency accuracy can be expressed as

$$f_a = \frac{f_e}{f_s} = \frac{|f_s - f_m|}{f_s}$$

To express frequency accuracy in parts per million:

$$f_{a(ppm)} = \frac{f_e}{f_s} \times 10^6$$

Frequency accuracy can also be expressed in deviation from actual time.

Deviation, in seconds per year, can be expressed as

$$\text{deviation} = 31,536,000 \text{ seconds per year} \times f_a$$

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb.06.24	-	First edition
1.01	May.17.24	-	Added Chapter 7 and updated some minor points
1.20	Dec.23.25	-	Updated the Group evaluation result: Added RA2E3, RA2A2, RA2L2, RA2T1, RA8M1, RA8D1, RA8T1, RA8E1, RA8E2, RA0E1, RA0E2, RA0L1, RA8P1, RA8M2, RA8D2 and RA8T2

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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