RH850/U2B Group

R01AN6292EJ0110
Rev.1.10

Estimation and Calculation of Chip Operating Temperature

Summary

This application note describes the chip temperature estimation and calculation method of RH850/U2B.

1. Power Consumption of Entire LSI

The total power consumption PD for this LSI can be calculated by the following Formula 1.1.

$$Pd = P_{SYSVCC} + P_{VCC} + P_{VDD} + P_{EMUVCC} + P_{EMUVDD} + P_{SVR} + P_{LVDS} + P_{DEBUG} + P_{GBETH} + P_{ADC} + P_{AFCVCC} + P_{IO} \quad \text{... Formula 1.1}$$

P_{SYSVCC} : SYSVCC Power Consumption

P_{VCC} : VCC and OSCVCC Power Consumption

P_{VDD} : VDD Power Consumption

P_{EMUVCC} : EMUVCC Power Consumption

P_{EMUVDD} : EMUVDD Power Consumption

P_{SVR} : SVR(Switching Voltage Regulator) Power Consumption

P_{LVDS} : LVDS Power Consumption

P_{DEBUG} : HSIF(debug) Power Consumption (J0VCC and J1VCC Power Consumption)

P_{GBETH} : Gigabit Ethernet Power Consumption(GETH0BVCC and GETH0PVCC Power Consumption)

P_{ADC} : AD Converter Power Consumption(A0VCC, A0VREFH, A1VCC, A1VREFH, A2VCC, A2VREFH, A3VCC, A3VREFH, ADSVCC, and ADSVREFH Power Consumption)

P_{AFCVCC} : AFCVCC Power Consumption

$P_{IO} = P_{IOCONST} + P_{IOINJ} + P_{IODO}$

$P_{IOCONST}$: I/O Buffer Constant Power Consumption (E0VCC, E1VCC and E2VCC Power Consumption)

P_{IOINJ} : I/O Buffer Injection Power

P_{IODO} : I/O Buffer Output Power (AC Operation)

1.1 SYSVCC Power Consumption

SYSVCC power consumption (P_{SYSVCC}) can be calculated by the following Formula 1.2.

Please refer to the user's manual for I_{SYSVCC_R}, or contact each sales department for calculation under your usage conditions.

$$P_{SYSVCC} = I_{SYSVCC\_R} \times SYSVCC \quad \text{...Formula 1.2}$$

1.2 VCC and OSCVCC Power Consumption

VCC and OSCVCC power consumption (P_{VCC}) can be calculated by the following Formula 1.3.

Please refer to the user's manual for I_{VCC_R}, or contact each sales department for calculation under your usage conditions.

$$Pvcc = I_{VCC\_R} \times VCC \quad \text{...Formura 1.3}$$

1.3 VDD Power Consumption

VDD power consumption (P_{VDD}) can be calculated by the following Formula 1.4.

Please refer to the user's manual for I_{ISOVDD_R}, or contact each sales department for calculation under your usage conditions.

$$P_{VDD} = I_{ISOVDD\_R} \times VDD \quad \text{...Formula 1.4}$$

I_{ISOVDD_R} : ISOVDD Current (A)

ISOVDD : VDD Voltage (V)

1.4 EMUVCC Power Consumption

EMUVCC power consumption (P_{EMUVCC}) can be calculated by the following Formula 1.5.

Please refer to the user's manual for I_{EMUVCC}, or contact each sales department for calculation under your usage conditions.

$$P_{EMUVCC} = I_{EMUVCC} \times EMUVCCC \quad \text{...Formula 1.5}$$

1.5 EMUVDD Power Consumption

EMUVDD power consumption (P_{EMUVDD}) can be calculated by the following Formula 1.6.

Please refer to the user's manual for I_{EMUVDD}, or contact each sales department for calculation under your usage conditions.

$$P_{EMUVDD} = I_{EMUVDD} \times EMUVDD \quad \text{... Formula 1.6}$$

1.6 SVR converter Power Consumption

SVR converter power consumption (P_{SVR}) can be calculated by the following Formula 1.7.
Please refer to the user's manual for I_{SVR} and I_{SVRA}, or contact each sales department for calculation under your usage conditions.

$$P_{SVR} = I_{SVR} \times SYSVCC + I_{SVRA} \times SVRAVCC + P_{SVRDR} \quad \text{... Formula 1.7}$$
$$P_{SVRDR} = f_{SVRSW} \times SVRDRVCC^2 \times (C_{iss\_}PMOSFET + C_{iss\_}NMOSFET)$$

f_{SVRSW} :SVR Switching Frequency
Ciss_PMOSFET: External Pch MOSFET input capacity for SVR
Ciss_NMOSFET: External Nch MOSFETinput capacity for SVR

1.7 LVDS Power Consumption

LVDS power consumption (P_{LVDS}) can be calculated by the following Formula 1.8.

Please refer to the user's manual for I_{LVDS}, or contact each sales department for calculation under your usage conditions.

$$P_{LVDVCC} = I_{LVDS} \times LVDVCC + I_{LVDS} \times EnVCC \ (n = 1 \sim 2) \quad \text{... Formula 1.8}$$

※For ILVDS, use the current value used for each power supply.

1.8 HSIF(debug) Power Consumption

HSIF(debug) power consumption (P_{DEBUG}) can be calculated by the following Formula 1.9.
Please refer to the user's manual for I_{DEBUG}, or contact each sales department for calculation under your usage conditions.

$$P_{DEBUG} = I_{DEBUG} \times J0VCC + \frac{|V_{OD}|^2}{R_{IN}} \quad \text{... Formula 1.9}$$

V_{OD} : Output Differential Voltage of the opposite device

Rin : Receiver differential input impedance

1.9 Gigabit Ethernet Power Consumption

Gigabit Ethernet power consumption (P_{GBETH}) can be calculated by the following Formula 1.10.

Please refer to the user's manual for I_{GBETH} and Rin, or contact each sales department for calculation under your usage conditions.

$$P_{GBETH} = I_{GBETH} \times GETH0BVCC + \frac{|V_{OD}|^2}{R_{IN}} \quad \text{...Formula 1.10}$$

V_{OD} : Output Differential Voltage of the opposite device

Rin : Receiver differential input impedance

1.10 ADC Power Consumption

This LSI AD converter power consumption of this LSI (P_{ADC}) can be calculated by the following Formula 1.11.

Please refer to the user's manual for I_{ADCn}, $I_{ADCnREF}$, I_{ADS}, and I_{ADSREF}, or contact each sales department for calculation under your usage conditions.

$$P_{ADC} = P_{ADCK0} + P_{ADCK1} + P_{ADCK2} + P_{ADCK3} + P_{ADS} \quad \text{...Formula 1.11}$$

$P_{ADCKn} = I_{ADCn} \times AnVCC + I_{ADCnREF} \times AnVREFH(n=0\sim3)$: SAR-AD module power consumption

$P_{ADS} = I_{ADS} \times ADSVCC + I_{ADSREF} \times ADSVREFH$: DSADC/CADC module power consumption

1.11 Fast Comparator and RD Converter Power Consumption

Fast comparator and RD converter power consumption (P_{AFCVCC}) can be calculated by the following Formula 1.12.

Please refer to the user's manual for I_{AFCVCC}, or contact each sales department for calculation under your usage conditions.

$$P_{AFCVCC} = I_{AFCVCC} \times AFCVCC \quad \text{...Formula 1.12}$$

1.12 I/O Buffer Power Consumption

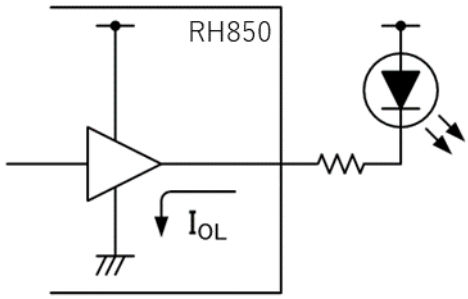
Add constant power consumption when DC current flows through the input, output, and input/output pins.

Ex. 1 When driving LED (When steady current flows)

$P_{IOCONST} = V_O \times I_{OL} \times A \times Buffer$

A: Rate the LED turns ON.

Buffer: Number of inputs/outputs/bidirectional buffer outputs.



1.13 I/O Buffer Injection Power

The I/O buffer injection power (P_{IOINJ}) of this LSI can be calculated by the following Formula 1.13.

$$P_{IOINJ} = \{Pinjdp \times Ninjdp + Pinjdm \times Ninjdm + Pinjap \times Ninjap + Pinjam \times Ninjam\} \ldots \text{Formula 1.13}$$

Pinjdp：Injection Power per Pin（Digital Pin, Positive Current Injection)

Ninjdp：Number Current Injected Pins (Digital Pin, Positive Current Injection）

Pinjdm：Injection Power per Pin （Digital Pin, Negative Current Injection）

Ninjdm：Number of Current Injected Pins（Digital Pin, Negative Current Injection）

Pinjap：Injection Power per Pin（Analog Pin, Positive Current Injection）

Ninjap：Number of Current Injected Pins（Analog Pin, Positive Current Injection）

Pinjam：Injection Power per Pin（Analog Pin, Negative Current Injection）

Ninjam：Number of Current Injected Pins（Analog Pin, Negative Current Injection）

1.14 I/O Buffer Output Power (AC Operation)

The I/O buffer output power (P_{IODO}) of this LSI can be calculated by the following Formula 1.14.

$$P_{IODO} = \Sigma (fo \times CL \times V^2) \ldots \text{Formula 1.14}$$

CL：Load Capacity

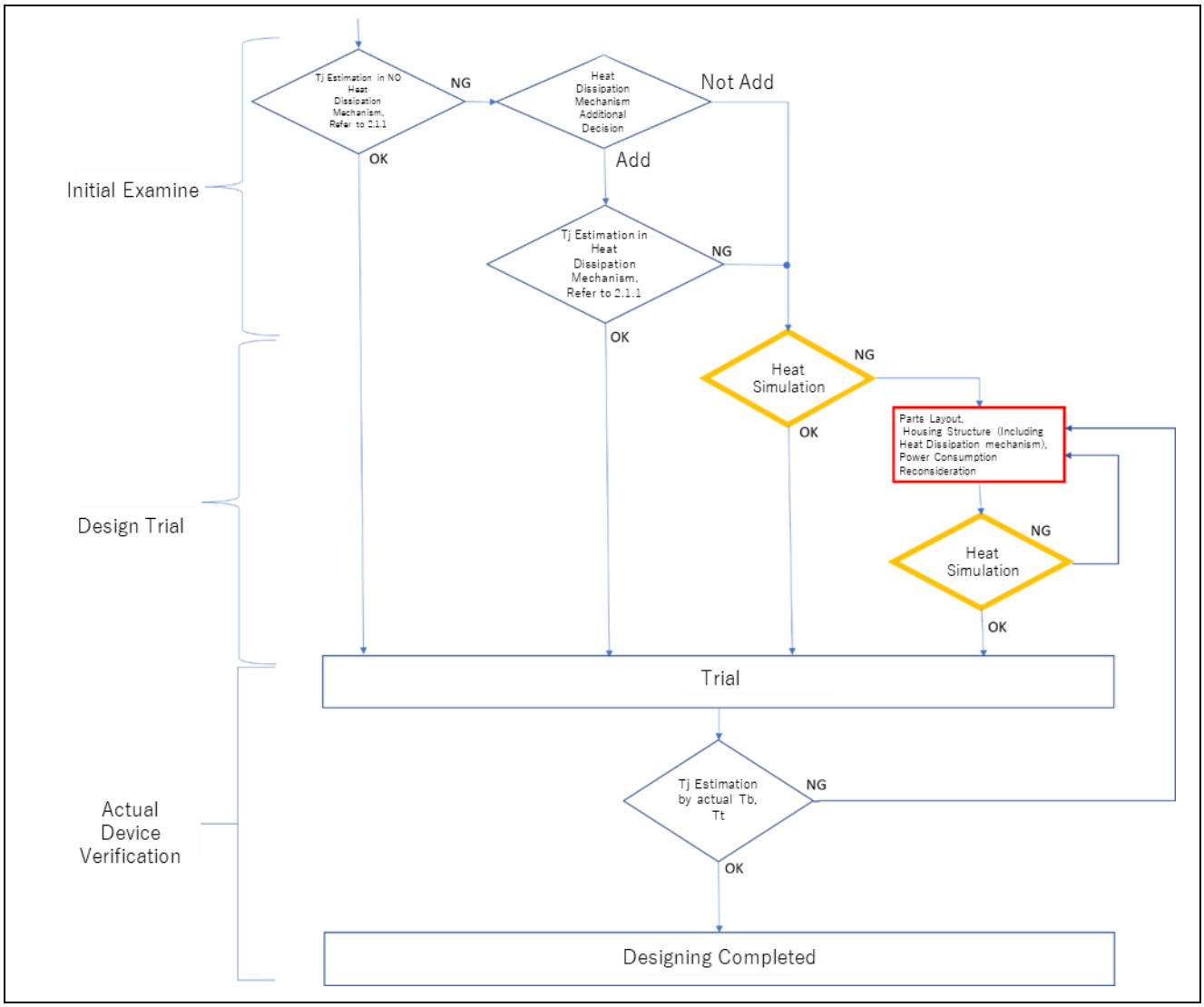
fo：Output Frequency

V：I/O Buffer Voltage

2. Chip Temperature (Tj) Estimation (Thermal Design Guide)

In the early stage of development, if the board temperature “Tb” and the package surface temperature “Tt” (Refer to 2.4.2 for definition) can be assumed from conventional products, estimate the chip temperature (Tj) using the values of Ψjb, Ψjt, etc. (see the user's manual for numerical values). As an initial consideration, this method is the most accurate method for Tj estimation. Estimate Tj with θja (see the user's manual for numerical values) when Tb or Tt cannot be assumed. If the estimated Tj is close to Tjmax (see the user's manual for the numerical value), estimate Tj by adding a heat dissipation mechanism or perform thermal simulation to estimate Tj in more detail.

If necessary, review the component layout, housing structure (including heat dissipation mechanism), and power consumption (IO buffer power, etc.) on the ECU board. Even if it is judged that there is a sufficient margin in the thermal simulation, measure Tb, Tt, etc. with a prototype. Estimate Tj using Ψjb, Ψjt, etc. from the measured Tb, Tt and power consumption, and confirm that it is below Tjmax.



2.1 Initial Consideration

2.1.1 Tj Estimation without Heat Dissipation Mechanism

Estimate Tj from formula 2.1 when Tb is estimated from conventional products, and from formula 2.2 using Tt when Tb cannot be estimated. When Tb and Tt cannot be estimated, estimate Tj from the formula 2.3 using Ta Tb. For XYΨjb, XYΨjt, and XY θ ja, apply the data closest to the assumed board among the data described in the user manual. If the estimated Tj is close to Tjmax, perform a thermal simulation or add a heat dissipation mechanism and consider Tj estimation.

(1)When estimate Tj from Tb

$$Tj = Tb + XY\psi jb \times Pd \quad \text{. . . Formula 2.1}$$

(2)When estimate Tj from Tt

$$Tj = Tt + XY\psi jt \times Pd \quad \text{. . . Formula 2.2}$$

(3)When estimate Tj form Ta

$$Tj = Ta + XY\theta ja \times Pd \quad \text{. . . Formula 2.3}$$

Caution：Refer to 2.1.3 for definition of each symbol.

The value of Ta changes greatly depending on where the measurement point is located. It is recommended to acquire Tb/Tt data and Tj estimation from Tb/Tt as much as possible because it may cause Tj estimation error.

2.1.2 Tj Estimation Mounted Heat Dissipation Mechanism only on top surface

Estimate Tj with Fig. 1 “ θ ja Thermal Resistance Net Model assuming” when there is a heat dissipation mechanism only on the upper surface. The ambient temperature (Ta) of the ECU is made uniform to model heat dissipation from the junction in the vertical direction. Relationship between Ta and Tj can be shown by the Formula 2.4 from Fig. 1. If θ ca cannot be inferred, Tt is inferred and Tj is estimated using Formula 2.5. Since θ ca changes depending on the usage environment, so it is necessary for the customer to calculate it.

$$\mathrm{Tj} = (\theta\mathrm{ca} + \theta\mathrm{jc}) \times \mathrm{Pt} + \mathrm{Ta} = (\theta\mathrm{ca} + \theta\mathrm{jc}) \times \left(1 - \frac{\Psi jb}{\theta jb}\right) \times Pd + Ta \ldots \text{Formula 2.4}$$

$$\mathrm{Tj} = \theta\mathrm{jc} \times \mathrm{Pt} + \mathrm{Tt} = \theta\mathrm{jc} \times \left(1 - \frac{\Psi jb}{\theta jb}\right) \times Pd + \mathrm{Tt} \ldots \text{Formula 2.5}$$

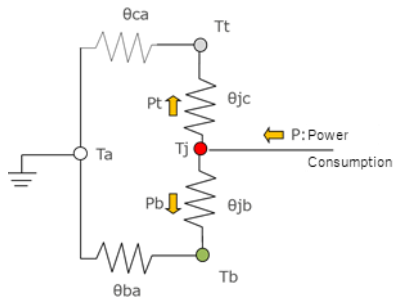


Fig. 1 θ ja Thermal Resistance Net Model

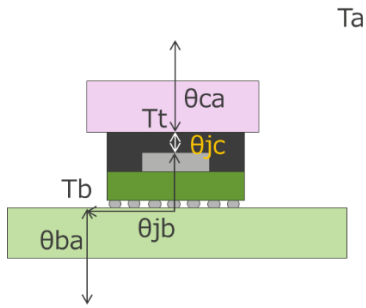


Fig. 2 Cross-section Image of Thermal Resistance Net

If Tt can be estimated from conventional products, etc., estimate Tj from Formula 2.6, and if θ ca can be estimated, estimate Tj from Formula 2.7. For XY Ψ jb and XY θ jb, apply the data described in the user manual that is closest to the assumed board. XY Ψ jb, If the estimated Tj is close to Tjmax, perform thermal simulation or add heat dissipation mechanism and consider the Tj estimation.

(1) When Tt is can be estimated

$$\mathrm{Tj} = \theta\mathrm{jc} \times \left(1 - \frac{XY\Psi jb}{XY\theta jb}\right) \times Pd + Tt \ldots \text{Formula 2.6}$$

(2) When θ ca is can be estimated

$$\mathrm{Tj} = (\theta\mathrm{ca} + \theta\mathrm{jc}) \times \left(1 - \frac{XY\Psi jb}{XY\theta jb}\right) \times Pd + Ta \ldots \text{Formula 2.7}$$

Caution：Refer to 2.1.3 for definition of each symbol.

2.1.3 Tj Estimation Mounted Heat Dissipation Mechanism only on top and bottom/bottom surface

Estimate Tj with Fig. 3 “ θ ja Thermal Resistance Net Model assuming” when there is a heat dissipation mechanism only on the upper and lower/ lower surface. The ambient temperature (Ta) of the ECU is made uniform to model heat dissipation from the junction in the vertical direction. Relationship between Ta and Tj can be shown by the Formula 2.8 from Fig. 3. If θ ca cannot be inferred, Tt is inferred and Tj is estimated using Formula 2.9. Since θ ca changes depending on the usage environment, so it is necessary for the customer to calculate it.

$$\mathrm{Tj} = (\theta\mathrm{ca} + \theta\mathrm{jc}) \times \mathrm{Pt} + \mathrm{Ta} = (\theta\mathrm{ca} + \theta\mathrm{jc}) \times \left(1 - \frac{\Psi jmb}{\theta jcbot}\right) \times Pd + Ta \ \ldots \text{Formula 2.8}$$

$$\mathrm{Tj} = \theta\mathrm{jc} \times \mathrm{Pt} + \mathrm{Tt} = \theta\mathrm{jc} \times \left(1 - \frac{\Psi jmb}{\theta jcbot}\right) \times Pd + \mathrm{Tt} \ \ldots \text{Formula 2.9}$$

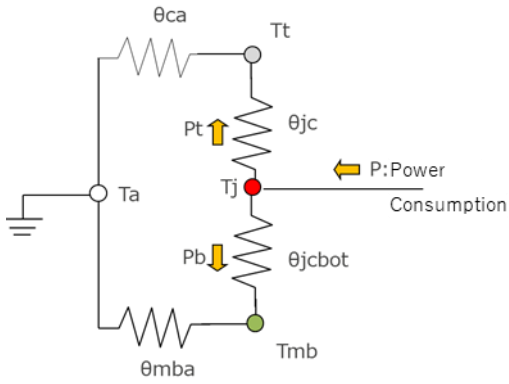


Fig. 3 θ ja Thermal Resistance Net Model

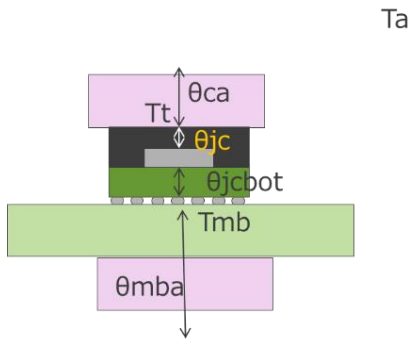


Fig. 4 Cross-section Image of Thermal Resistance Net

If Tt can be estimated from conventional products, etc., estimate Tj from Formula 2.10, and if θ ca can be estimated, estimate Tj from Formula 2.11. For XY Ψ jb and XY θ jb, apply the data described in the user manual that is closest to the assumed board. XY Ψ jb, If the estimated Tj is close to Tjmax, perform thermal simulation or add heat dissipation mechanism and consider the Tj estimation.

(1) When Tt is can be estimated

$$\mathrm{Tj} = \theta\mathrm{jc} \times \left(1 - \frac{XY\Psi jmb}{\theta jcbot}\right) \times Pd + Tt \ \ldots \text{Formula 2.10}$$

(2) When θ ca is can be estimated

$$\mathrm{Tj} = (\theta\mathrm{ca} + \theta\mathrm{jc}) \times \left(1 - \frac{XY\Psi jmb}{\theta jcbot}\right) \times Pd + Ta \ \ldots \text{Formula 2.11}$$

Tj : LSI Chip Junction Temperature

Ta : LSI PKG Ambient Temperature

Tb : Temperature described in “2.4.2 Measurement Point”

Tt : Temperature described in “2.4.2 Measurement Point”

Tmb : Temperature at the center of PKG on mounting board L1 surface

Pd : Power consumption of entire LSI calculated by Formula 1.1

Pt : Flowing power toward PKG top surface direction

Pb : Flowing power toward PKG under surface direction

θca : Tt and Ta Thermal Resistance (Value calculated by customer.)

θba : Tb and Ta Thermal Resistance (Value calculated by customer.)

θjb : LSI Package Thermal Resistance (Not used for heat estimation. Use XY θ jb close to your board.)

θmba : Tmb and Ta Thermal Resistance (Value calculated by customer.)

Ψjb : LSI Package Thermal Characteristics (Not used for heat estimation. Use XY Ψjb close to your board.)

Ψjmb : LSI Package Thermal Characteristics (Not used for heat estimation. Use XY Ψjmb close to your board.)

θjc : LSI Package Thermal Resistance (Refer to User’s Manual※.)

θjcbot : LSI Package Thermal Resistance (Refer to User’s Manual※.)

XYθja : LSI Package Thermal Resistance (Refer to User’s Manual※.)

XYθjb : LSI Package Thermal Resistance (Refer to User’s Manual※.)

XYψjb : LSI Package Thermal Characteristics (Refer to User’s Manual※.)

XYψjt : LSI Package Thermal Characteristics (Refer to User’s Manual※.)

XY Ψjmb : LSI Package Thermal Characteristics (Refer to User’s Manual※.)

※Reference : RH850/U2B User's Manual: Hardware, Thermal Characteristics Parameter

X : Number of Board Layer

Y : Board Size

Please refer to “2.4.4 Assumed Board” for the assumed board size.

2.2 Thermal Simulation

Perform thermal fluid simulation (computational fluid dynamics: CFD) for more accurate temperature prediction. We provide the package model for FloTHERM (DELPHI model). Please contact each sales department.

2.3 Actual Machine Verification (Tj Evaluation with Prototype)

2.3.1 Tj Evaluation with No Thermal Dissipation Mechanism

Measure Tb and power consumption and estimate Tj with Formula 2.12, or measure Tt and power consumption and estimate Tj with Formula 2.13. For XYΨjt, XYΨjb, and XYTb_inc, apply the conditions described in the user manual closest to the prototype. (The formula does not include measurement error. Please estimate in consideration of measurement error.)

(1) When estimate Tj from Tb

$$Tj = Tb\_typ + XY\psi jb \times Pdtyp + (XY\psi jb + XYTb\_inc) \times (Pd\_offset + Pd\_vothers) \quad \text{Formula 2.12}$$

(2) When estimate Tj from Tt

$$Tj = Tt\_typ + XY\psi jt \times (Pdtyp + Pd\_offset + Pd\_vothers) \quad \text{Formula 2.13}$$

$$Pd\_offset = Vm \times Id\_offset + I0 \times (Vm-V0) + Vm \times (dI/dV) \times (Vm-V0) \quad \text{Formula 2.14}$$

※When estimating the worst power from the power calculation tool, Pd_offset is as follows.

$$Pd\_offset = Pd\_max - Pdtyp$$

Caution：Refer to 2.3.3 for definition of each symbol.

2.3.2 Heat Dissipation Mechanism only on top surface

When heat dissipation mechanism only on the package top surface. [Assumptions: PKG top surface is in connect with the metal plate (Electrogalvanized Steel, Thickness 1mm) of the same size as the board via the thermal sheet (Thickness 1mm, 1W/mK) of the same size as the mold resin.]

Measure Tb and power consumption and estimate Tj with Formula 2.15, or measure Tt and power consumption and estimate Tj with Formula 2.16. For XYΨjb, XYTb_inc, and XY θ jb apply the conditions described in the user manual closest to the prototype. (The formula does not include measurement error. Please estimate in consideration of measurement error.)

(1) When estimate Tj form Tb

$$Tj = Tb\_typ + XY\Psi jb \times Pdtyp + (XY\Psi jb + XYTb\_inc) \times (Pd\_offset + Pd\_vothers) \ldots \text{Formula 2.15}$$

(2) When estimate Tj form Tt

$$Tj = Tt_{typ} + \theta jc \times \left(1 - \frac{XY\Psi jb}{XY\theta jb}\right) \times (Pdtyp + Pd_{offset} + Pd_{vothers}) \ldots \text{Formula 2.16}$$

Pd_offset = Vm × Id_offset + I0 × (Vm-V0) + Vm × (dI/dV) × (Vm-V0) . . . Formula 2.17

※When estimating the worst power from the power calculation tool, Pd_offset is as follows.

Pd_offset = Pd_max – Pdtyp

Caution：Refer to 2.3.3 for definition of each symbol.

2.3.3 Heat Dissipation Mechanism only on top and under/ under surface

When heat dissipation mechanism only on the package top and under or under surface. [Assumptions: PKG top surface is in connect with the metal plate (Electrogalvanized Steel, Thickness 1mm) of the same size as the board via the thermal sheet (Thickness 1mm, 1W/mK) of the same size as the mold resin.] Measure Tt and power consumption and estimate Tj with Formula 2.18. For XYΨjmb, apply the conditions described in the user manual closest to the prototype. (The formula does not include measurement error. Please estimate in consideration of measurement error.)

$$Tj = Tt_{typ} + \theta jc \times \left(1 - \frac{XY\Psi jmb}{\theta jcbot}\right) \times Pdtyp + \theta jc \times \left(1 - \frac{XY\Psi jmb}{\theta jcbot}\right) \times (Pd_{offset} + Pd_{vothers}) \ldots \text{Formula 2.18}$$

Pd_offset = Vm × Id_offset + I0 × (Vm-V0) + Vm × (dI/dV) × (Vm-V0) . . . Formula 2.19

※When estimating the worst power from the power calculation tool, Pd_offset is as follows.

Pd_offset = Pd_max – Pdtyp

Tj : LSI Chip Junction Temperature
Tb_typ : Tb actual measurement value when running application on actual ECU
Tt_typ : Tt actual measurement value when running application on actual ECU
Pdtyp : LSI power consumption considering VDD measurement value when running application on actual ECU
Pd_max : Worst VDD power estimated from power calculation tool
Pd_offset : Difference between Pdtyp and corner sample power consumption
Pd_vothers : Power consumption with power sources other than VDD (AnVCC, LVDVCC, etc.)
Id_offset : Difference between I0 and worst VDD current estimated by power calculation tool
dI/dV : VDD Dependency Coefficient of IDD
Vm : VDD Maximum Voltage (maximum voltage under customer's usage conditions)
V0 : VDD voltage during measurement
I0 : Measured VDD Current
θjc : LSI Package Thermal Resistance (Refer to User's Manual※.)
θjcbot : LSI Package Thermal Characteristics (Refer to User's Manual※.)
XYθjb : LSI Package Thermal Resistance (Refer to User's Manual※.)
XYψjb : LSI Package Thermal Characteristics (Refer to User's Manual※.)
XYψjt : LSI Package Thermal Characteristics (Refer to User's Manual※.)
XYψjmb : LSI Package Thermal Characteristics (Refer to User's Manual※.)
XYTb_inc : Tb Power Consumption Dependence (Refer to User's Manual※.)

※Reference : RH850/U2B User's Manual: Hardware, Thermal Characteristics Parameter
Tb is Tb_0 when MCU heat generation is 0W, and Tb is Tb_1 when MCU heat generation is 1W
XYTb_inc = Tb_1 – Tb_0
X : Number of Board Layer
Y : Board Size

Please refer to "2.4.4 Assumed Board" for the assumed board size.

2.4 Precautions for Tb／Tt Measurement

2.4.1 Measurement using Thermocouple

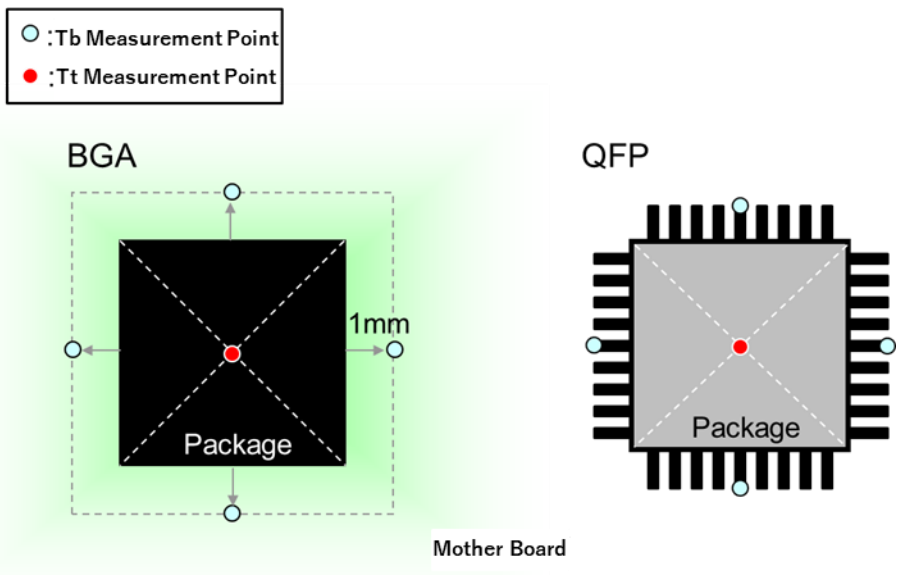
In order to measure the temperature, be careful about using thermocouple and the attaching method of the thermocouple to the object to be measured. The notes and recommendations are shown below.

- Use the thermocouple with the wire diameter as thin as possible. (For heat drawing suppression. Recommended: Diameter 100um or less)
- Recommend type K thermocouple. (Type T thermocouple has a large dissipation and may measure at a low temperature.)
- Recommend the heat resistance resin tape or heat resistant resin material for fixing the thermocouple.
- Securely fix the thermocouple to the measurement target. (Measurement error occur if there is a “float”.)

2.4.2 Measurement Point

BGA：Make sure the temperature is saturated and measure Tb on the board wiring 1mm outside the midpoint of each side of the package. When there is a temperature distribution due to the influence of peripheral parts, use the average value of the four measurement points as Tb. Tt is the center temperature of the package top surface.

QFP：Make sure the temperature is saturated and measure Tb on the lead foot pattern at the midpoint of each side of the package. When there is a temperature distribution due to the influence of peripheral parts, use the average value of the four measurement points as Tb. Tt is the center temperature of the package top surface.



2.4.3 Measurement using Thermography (Thermo Camera)

For measuring the temperature accurately, set the emissivity of the object to be measured in the thermography. The emissivity of the board surface is approximately 0.8-0.9, but the metal surface is generally small. (If the genus surface is measured at a setting of 0.8 to 0.9, it will be measured at a lower temperature than the actual temperature.) If the emissivity is unknown, perform surface treatment with a blackbody spray, etc., and set the emissivity of the blackbody spray to enable accurate measurement of the temperature.

Also, please note that correct measurement results will not be obtained if there is an object between the thermography and the measurement target (even if it is a translucent acrylic plate). In this case, thermography, measures the acrylic plate temperature.

Temperature measurement by thermography may be difficult depending on the arrangement of the measurement target, but it is an effective means to know the temperature distribution, so we recommend to use it together with a thermocouple.

2.4.4 Assumed Board

Compliant with JESD51-9 (4layers)

	Board Size(mm)		Area(mm2)
	X	Y	
Board	101.5	114.5	11621.75
Residual Copper Rate		Conductor Thickness	
50-95-95-50%		70-35-35-70 μm	

L Board (4layers)

	Board Size(mm)		Area(mm2)
	X	Y	
Board	90	160	14400
Residual Copper Rate		Conductor Thickness	
30-80-80-30%		35-35-35-35 μm	

3. Reference Page

Please refer below for the overview of the package thermal/power characteristics.

https://www.renesas.com/support/technical-resources/package/characteristic.html

Our Company's Website and Inquiry

- Website
  https://www.renesas.com/
- Inquiry
  https://www.renesas.com/contact/

Revision History

Rev.	Date	Description	
		Page	Summary
0.50	2021.11.08	-	Initial Edition (Perform changing from U2A.)
1.00	2024.12.11	-	Document number update (contents are not changed)
1.10	2025.04.04	12	Correction of typos (Tb, Tt description)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

- 1. Precaution against Electrostatic Discharge (ESD)

  A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

- 2. Processing at power-on

  The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

- 3. Input of signal during power-off state

  Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

- 4. Handling of unused pins

  Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

- 5. Clock signals

  After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

- 6. Voltage application waveform at input pin

  Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

- 7. Prohibition of access to reserved addresses

  Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

- 8. Differences between products

  Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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